Intel Unveils Second-Generation Neuromorphic Chip

October 5, 2021, Intel has unveiled its second-generation neuromorphic computing chip, Loihi 2, the first chip to be built on its Intel 4 process technology. Designed for research into cutting-edge neuromorphic neural networks, Loihi 2 brings a range of improvements. They include a new instruction set for neurons that provides more programmability, allowing spikes to have integer values beyond just 1 and 0, and the ability to scale into three-dimensional meshes of chips for larger systems.

Review

• Core FPGA building blocks:
  • Configurable Logic Blocks (CLBs)
  • Configurable Interconnect
    • Switch boxes

• Modern FPGA Designs:
  • BRAMs, DSPs, and AI Engines

• CMOS process is used for producing chips
  • Planar bulk process used up to 28nm node
  • finFET and FDSOI used below the 22nm node

Intel’s Loihi 2 second-generation neuromorphic processor. (Source: Intel)
MOS Transistors

- Symbol
  - N-type NMOS
  - P-type PMOS

- Devices are symmetrical
  - NMOS: Drain is at higher voltage
  - PMOS: Source is at higher voltage

- Gate oxide
- Contacts
- N+ diffusion
- P+ diffusion
Different Kinds of MOS Transistors

- **Planar bulk CMOS**
  - N-type NMOS
  - \( S \rightarrow G \rightarrow D \)
  - \( W/L \)

- **FinFET**
  - \( S \rightarrow G \rightarrow D \)
  - \( W \)
  - Finite Width = \( T_{Si} \)
  - \( H_{FIN} \)

FinFET widths are discrete (\( W = kW_{unit} \))

- \( k \) is an integer

- Lengths are quantized because of lithography
  - Also are quantized lower metal layers, contacts…

Transistor Dimensions are Quantized
Ohm’s Law

- Resistors

\[ V = IR \]

- Variable resistors

\[ R = \rho \frac{L}{TW} \]

- Physical resistors

In a planar process, the designer controls W and L.

Series and Parallel

- With two identical resistors, \( R \)

\[ R_{\text{series}} = 2R \]

Equivalent to doubling length

\[ R_{\text{parallel}} = \frac{R}{2} \]

Equivalent to doubling width
An n-Channel MOS Transistor

When \( V_{GS} < V_{Th} \), transistor is off

\[ V_D = 0V \quad V_G = 0V \quad V_S = 0V \]

Dielectric, Polysilicon gate, and substrate form a capacitor.

When \( V_{GS} \geq V_{Th} \), transistor is on

\[ V_D > 0 \quad V_G > V_{Th} \quad V_S = 0V \]

Small region near the surface turns from p-type to n-type.

Current is proportional to \( V_{DS} \).
An n-Channel MOS Transistor

$V_D > 0$  $V_{GS} > V_{Th}$  $V_S = 0V$

$V_{DG} < 0$  $V_G > V_{Th}$  $V_S = 0V$

$V_{DS} > V_{GS} - V_{Th}$

MOS Transistors

- NMOS Transistor I-V characteristics

Old transistor

~7nm transistor

Nearly linear

$I_{DS} \sim K(V_{GS}-V_{Th})$
Velocity Saturation

• Carrier velocity in the channel saturates

- Electric field, $E \text{ [V/\mu m]}$
- Carrier velocity $\text{[m/s]}$
- Velocity linearly proportional to $E$, $v = \mu E$
- Velocity saturated at $v \approx 10^5 \text{ m/s}$ (for fields $> 1 \text{V/m}$)

• All submicron transistors are velocity saturated
• Other effects (drain-induced barrier lowering) cause $I_{DS}$ to increase in saturation

Administrivia

• Homework 5 will be posted later this week, due next week
• No lab this week
  • Lab 6 (last) after the midterm
• Midterm 1 on October 7, 7-8:30pm
  • You will be assigned a classroom
  • One double-sided page of notes allowed
  • Material includes FPGAs
MOS Transistor as a Switch

V_{GS} controls the switch

(it also charges the channel capacitor)
ON/OFF Switch Model of MOS Transistor

\[ |V_{GS}| < |V_t| \]

\[ |V_{GS}| \geq |V_t| \]

A More Realistic Model

• It is a dimmer!
A Logic Perspective

NMOS Transistor

\[ V_{GS} > V_{Th} \]

\[ Y = B \text{ if } A = 1 \]

PMOS Transistor

\[ V_{GS} < V_{Th} \]

\[ Y = B \text{ if } A = 0 \]

AND and OR

- AND

\[ F = AB \]

\[ (F = AB + \overline{A} \cdot 0) \]

- OR

\[ F = A + B \]

\[ (F = A \cdot 1 + \overline{A}B) \]

- Keep in mind – single NMOS/PMOS transistors are imperfect switches!
  - Turns off when \(|V_{GS}| = |V_{Th}|\)
Peer Instruction

• Switch logic

• Which combination of inputs implements \( F = AB \)?

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