Intel to spin-off Programmable Solutions Group as standalone business eyeing IPO in 2-3 years

October 3, 2023. AnandTech. Intel this afternoon has announced that the company will be spinning off its programmable solutions group (PSG), to operate as a standalone business. The business unit, responsible for developing Intel's Agilex, Stratix, and other FPGA products, will become a standalone entity under Intel's corporate umbrella starting in Q1 of 2024, with the long-term goal of eventually selling off part of the group in an IPO in two to three years’ time.

Review

• Features of recent FPGAs

• CMOS process is used for producing chips
  • Planar bulk process used up to 28nm node
  • finFET used below the 22nm node
    • Also FDSOI, but we didn’t talk about it

• MOS transistor operation
MOS Transistor as a Switch
MOS Transistor as a Resistive Switch

- $|V_{GS}|$ controls the switch
  - (it also charges the channel capacitor)
ON/OFF Switch Model of MOS Transistor

$|V_{GS}| < |V_T|$  
$|V_{GS}| \geq |V_T|$

$R_{on}$
A More Realistic Model

• It is a dimmer!
A Logic Perspective

NMOS Transistor

\[ V_{\text{GS}} > V_{\text{Th}} \]

\[ Y = B \text{ if } A = 1 \]

PMOS Transistor

\[ V_{\text{GS}} < V_{\text{Th}} \]

\[ Y = B \text{ if } A = 0 \]
AND and OR

• AND

\[ F = AB \]  
\[ (F = AB + \bar{A} \cdot 0) \]

• OR

\[ F = A + B \]  
\[ (F = A \cdot 1 + \bar{A}B) \]

• Keep in mind – single NMOS/PMOS transistors are imperfect switches!
  • Turns off when \(|V_{GS}| = |V_{Th}|\)
Quiz

• Switch logic

• Which combination of stored inputs implements $F = AB$?

<table>
<thead>
<tr>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
</tr>
</thead>
<tbody>
<tr>
<td>a)</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>b)</td>
<td>0</td>
<td>X</td>
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<td>c)</td>
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<td>d)</td>
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<td>e)</td>
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<td>1</td>
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<tr>
<td>f)</td>
<td>None of the above</td>
<td></td>
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CMOS Inverter
CMOS Inverter

• Simple DC behavior
  • Schematic

\[ V_{DD} \]

\[ V_D \]

\[ V_{in} = V_{DD} \]
\[ V_{in} = 0 \]

\[ V_{OL} = 0 \]
\[ V_{OH} = V_{DD} \]
Voltage Transfer Characteristic (VTC)

\[ V_A = V_{GS,n} = V_{DD} - V_{SG,p} \]

\[ I_{DS,n} = I_{SD,p} \]

\[ V_{Out} = V_{DS,n} = V_{DD} - V_{SD,p} \]
Voltage Transfer Characteristic (VTC)

• Can we change switching point ($V_A$ for which $V_{out} = \frac{V_{DD}}{2}$)?
Digital Circuits

• One logic representation
  \[ \text{Out} = \overline{A} \]

  Truth table
<table>
<thead>
<tr>
<th>A</th>
<th>Out</th>
</tr>
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<tbody>
<tr>
<td>0</td>
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• Multiple libraries
  • Layouts
    • Number of metal ‘tracks’
    • More tracks, faster, but larger
    • Less tracks – more compact, but slower

• Transistor thresholds \( (V_{Th}) \)
  (for each track height):
  • Regular (RVT)
  • Low (LVT)
    • Faster, higher power
    • Slower, lower power
  • High (HVT)

• Multiple gate sizes within a library

  • Symbol
  • Schematic

  \[ V_{DD} \]

  INVX1

  \[ M_1 \]

  \[ M_2 \]

  \[ W_{p/L} \]

  \[ W_{n/L} \]

  INVX2

  \[ M_1 \]

  \[ M_2 \]

  \[ 2W_{p/L} \]

  \[ 2W_{n/L} \]

  INVX3, INVX4,…

• Layout
Administrivia

• Midterm 1: tonight 10/5, 7-8:30pm
• Scope: Up to lecture 11 (& lab 5)
  • One double-sided page of notes allowed
• Lab break this week, lab 6 after midterm
  • Lab sessions for checkoffs this week
• Homework 5 posted this week
CMOS Logic
Building Logic From Switches

\[ Y = X \text{ if } A \text{ OR } B \]
\[ Y = X \text{ if } A \text{ AND } B \]

(output undefined if condition not true)
Logic, Using Inverting Switches

Series

\[ Y = X \text{ if } \overline{A} \text{ AND } \overline{B} \]
\[ = \overline{A + B} \]

Parallel

\[ Y = X \text{ if } \overline{A} \text{ OR } \overline{B} \]
\[ = \overline{A \cdot B} \]

(output undefined if condition not true)
Static Complementary CMOS

PUN and PDN are dual logic networks
PUN and PDN functions are complementary
Complementary CMOS Logic Style

- PUN is the dual to PDN (can be shown using DeMorgan’s Theorems)
  \[
  \overline{A + B} = \overline{AB} \\
  \overline{AB} = \overline{A + B}
  \]

- Static CMOS gates are always inverting
  \[
  \text{AND} = \text{NAND} + \text{INV}
  \]
Example Gate: NAND

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Truth Table of a 2 input NAND gate

- **PDN:** $G = AB \Rightarrow$ Conduction to GND
- **PUN:** $F = \overline{A + B} = AB \Rightarrow$ Conduction to $V_{DD}$
- $G(In_1, In_2, In_3, \ldots) \equiv F(In_1, In_2, In_3, \ldots)$
Example Gate: NOR

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Truth Table of a 2 input NOR gate

\[
\text{OUT} = \overline{A + B}
\]
Complex CMOS Gate

\[ \text{OUT} = D + A \cdot (B + C) \]

- Note: In scaled processes max #inputs is 3-4
- Max stack height is 2 or 3
Stick Diagrams
Stick Diagrams

Contains no dimensions
Represents relative positions of transistors

Inverter

NAND2
Stick Diagrams

\[ X = C \cdot (A + B) \]
Two Versions of $C \cdot (A + B)$
Consistent Euler Path

\[ X = C \cdot (A + B) \]
$X = (A+B) \cdot (C+D)$
Example: $x = \overline{ab+cd}$

(a) Logic graphs for $(ab+cd)$

(b) Euler Paths \{a b c d\}

(c) stick diagram for ordering \{a b c d\}
Summary

• CMOS switching behavior
• Series and parallel connection of switches implements logic
• CMOS inverter VTC
  • Almost ideal
• CMOS logic
  • N and P networks duals of each other
• Stick diagrams
  • Links to layout