Problem 1: Not So Much Effort

Consider a NAND3 gate that drives one of the input of a NAND2 gate:

For this problem, assume you have a reference inverter with $W_P = W_N = 1$ and $R_P = R_n = R_{eq}$. This technology has $\gamma \equiv \frac{C_d}{C_g} = 1.5$.

(a) Assume PMOS has unit size (“1”). Draw the transistor-level schematic for the circuit above and size all the NMOS transistors such that the equivalent switching resistances are the same as a reference inverter.

(b) What is the Logical Effort of each gate? Show your steps.

$$LE_{\text{NAND3}} = \frac{C_y + 3C_y}{C_g + C_g} = \frac{4}{2} = 2$$
\[ LE_{NAND2} = \frac{C_g + 2C_g}{C_g + C_g} = \frac{3}{2} \]

(c) Now let the second NAND gate drive a load \( C_L \). Assume the PMOS of the reference inverter has gate capacitance \( C_g \). Write the delay from A to the output driving \( C_L \).

Total delay = Delay of NAND3 driving NAND2 + Delay of NAND2 driving \( C_L \)

\[ t_{loaded} = \ln(2) * R_{eq} * (3\gamma C_g + 3\gamma C_g + 3C_g) + \ln(2) * R_{eq} * (2\gamma C_g + 2\gamma C_g + C_L) \]

\[ = \ln(2) * R_{eq} * \left[ (6\gamma + 3 + 4\gamma)C_g + C_L \right] \]

\[ = \ln(2) * R_{eq} * C_g * \gamma * 2 * \frac{(6 + 4)}{2} + \ln(2) * R_{eq} * C_g * 2\left(\frac{\gamma}{3} \cdot \frac{4}{2} + \frac{C_L}{3C_g} \cdot \frac{3}{2}\right) \]

\[ = \ln(2) * R_{eq} * [18C_g + C_L] \]

**Problem 2: More Effort**

Consider the following multi-stage network. The two inverters in the last stage are identical.

![Multi-stage network diagram]

Again, assume you have a reference inverter with \( W_P = W_N = 1 \) and \( R_p = R_n = R_{eq} \). This technology has \( \gamma \equiv \frac{C_d}{C_g} = 1.5 \).

(a) The input capacitance of A is \( C_{in} \) and the load \( C_L = 48 * C_{in} \). Determine the path effort from A to the output load \( C_L \).

\[ G = \frac{3}{2} * \frac{3}{2} * 1 * 2 * 1 = \frac{9}{2} \]
\[ B = 1 * 1 * 1 * 1 * 2 = 2 \]
\[ F = 48 \]
\[ H = GBF = 432 \]

(b) Determine the optimum stage effort (SE) that results in minimum delay.

\[ SE_{opt} = \sqrt[5]{432} \approx 3.37 \]

(c) Express the minimum delay in terms of the intrinsic delay of the reference inverter, \( \tau_{inv} \).

\[ \tau_{min} = \frac{\tau_{inv}}{\gamma} * (5 * SE_{opt}) + \tau_{inv} \Sigma p \]
\[ = \tau_{inv} \left( 5 \cdot \frac{SE_{opt}}{\gamma} + \Sigma p \right) \]
\[
\tau_{inv} = \tau_{inv} \left( \frac{5 \sqrt[\gamma]{432}}{\gamma} + \left( \frac{4}{2} + \frac{4}{2} + 1 + \frac{6}{2} + 1 \right) \right) \\
\approx 20.2 \tau_{inv}
\]

Alternatively, if define \( \tau_{inv} = \ln 2 * R_{eq} * C_{in,inv} \) then the answer is
\[
\tau_{inv} \left( 5 * S E_{opt} + \sum p * \gamma \right) = \tau_{inv} \left( 5 * \sqrt[\gamma]{432} + \left( \frac{4}{2} + \frac{4}{2} + 1 + \frac{6}{2} + 1 \right) * 1.5 \right) \\
\approx 30.32 \tau_{inv}
\]

(d) Based on your answers above, find the optimum input capacitance of the gates of each stage on the critical path.

\[
E = 48C_{in} * 1 * \frac{2}{S E_{opt}} \approx 28.49 C_{in}
\]
\[
D = E * 2 * \frac{1}{S E_{opt}} \approx 16.91 C_{in}
\]
\[
C = D * 1 * \frac{1}{S E_{opt}} \approx 5.01 C_{in}
\]
\[
B = C * \frac{3}{2} * \frac{1}{S E_{opt}} \approx 2.23 C_{in}
\]

Sanity check:

\[
A = B * \frac{3}{2} * \frac{1}{S E_{opt}} \approx 1 C_{in}
\]