Problem 1: Fun with RC Delay

The value of each component in the RC network here is listed below:

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>100 fF ($= 100 \times 10^{-15} F$)</td>
<td>R1</td>
<td>1000 Ω</td>
</tr>
<tr>
<td>C2</td>
<td>50 fF</td>
<td>R2</td>
<td>1200 Ω</td>
</tr>
<tr>
<td>C3</td>
<td>60 fF</td>
<td>R3</td>
<td>1500 Ω</td>
</tr>
<tr>
<td>C4</td>
<td>20 fF</td>
<td>R4</td>
<td>1800 Ω</td>
</tr>
<tr>
<td>C5</td>
<td>30 fF</td>
<td>R5</td>
<td>2000 Ω</td>
</tr>
</tbody>
</table>

Find the RC delay constant $\tau$ from node A to node 4.

First we calculate $\tau$ of the net by viewing $s$ as the input and $i$ as the output:

$$\tau = \sum_n \left( R_n \sum_m C_m \right)$$

where $R_n$ are resistors on the PATH from $s$ to $i$, and $C_m$ is the downstream capacitors for each $R_n$ on the path from $s$ to $i$.

$$\tau = \sum_n \left( R_n \sum_m C_m \right) = 1000 \times (100 + 50 + 60 + 20 + 30) \times 10^{-15} + 1500 \times (60 + 20 + 30) \times 10^{-15} + 1800 \times 60 \times 10^{-15} = 5.33 \times 10^{-10} s$$

If the answer has an $\ln (2)$ factor, it will also be accepted. i.e. $3.69 \times 10^{-10} s$ is also ok.
Problem 2: Wires Aren’t Just Lines
Assume we use a minimum sized inverter ($C_{g,min} = 0.3fF$) to drive an inverter sized the twice of the first inverter (i.e. gate lengths are the same as the minimum inverter, but widths are doubled). The second inverter doesn’t have any external load but only its own parasitic capacitance. There is a long piece of wire in between those two inverters and its delay cannot be ignored.

The intrinsic delay the first inverter, $t_0 = \ln 2 \ast R_{eq,min} \gamma \ast 2C_{g,min}$ (notice this definition has $\gamma$) is 4ps. $\gamma = 1.5$ for this technology. The resistance and capacitance of this wire is $r = 0.05\Omega/\mu m$ and $c = 0.2fF/\mu m$, respectively. The length of the wire is $L = 1.2 \ast 10^4 \mu m$.

(a) What is the total delay, $t$, of this circuit (from input to the output)? Show your steps and write your final numerical answer.

The corrected way is to use the following Elmore delay model:
\begin{align*}
3 &= 4444 \times \left(2 \times 1.5 \times 0.3 \times 10^{-15} + 0.2 \times 10^{-15} \times \frac{1.2 \times 10^4}{2} \times 2 + 4 \times 0.3 \times 10^{-15} \right) + \ln 2 \times 0.05 \\
&\quad \times \frac{1.2 \times 10^4}{2} \times \left(0.2 \times 10^{-15} \times \frac{1.2 \times 10^4}{2} + 4 \times 0.3 \times 10^{-15} \right) + \frac{4444}{2} \times 4 \times 1.5 \times 0.3 \\
&\quad \times 10^{-15} \\
&= 4444 \times 2.4021 \times 10^{-12} + 207.944 \times 1.2012 \times 10^{-12} + 4 \times 10^{-12} \\
&\approx 1.093 \times 10^{-8} s \text{ or } 10.93 \text{ ns}
\end{align*}

If the answer is missing \( \ln(2) \), i.e. if the answer is \( 1.58 \times 10^{-8} s \), lose one point

(b) Now we are breaking up the wire into \( N \) equal segments and insert \( N \) identically sized inverters to achieve lower delay (there is no wire between the original first inverter and the inv1 we insert). If we cannot ignore the delay due to the inverters, what is the new total delay (in terms of \( N \) and the size of these inverters, \( S \), and parameters given above. No need to write the numerical values.)

Using the similar Elmore model like above, the answer will be:

\begin{align*}
t &= \ln 2 \times R_{eq,\text{min}} \left(2y C_{g,\text{min}} + 2 + S \times C_{g,\text{min}}\right) \\
+(N - 1) \times \ln 2 \left(\frac{R_{eq,\text{min}}}{S} \left(2y SC_{g,\text{min}} + \frac{c_{\text{wire}}}{N} + 2SC_{g,\text{min}}\right) + \frac{r_{\text{wire}}}{N} \left(c_{\text{wire}} + 2SC_{g,\text{min}}\right)\right) \\
+ \ln 2 \left(\frac{R_{eq,\text{min}}}{S} \left(2y SC_{g,\text{min}} + \frac{c_{\text{wire}}}{N} + 4C_{g,\text{min}}\right) + \frac{r_{\text{wire}}}{N} \left(c_{\text{wire}} + 4C_{g,\text{min}}\right)\right) \\
+ \ln 2 \left(2y SC_{g,\text{min}} + \frac{c_{\text{wire}}}{N} + 4C_{g,\text{min}}\right) + \frac{r_{\text{wire}}}{N} \left(c_{\text{wire}} + 4C_{g,\text{min}}\right) \\
+ \ln 2 \times \frac{R_{eq,\text{min}}}{2} \times 4y C_{g,\text{min}}
\end{align*}
(c) **Optional Part** (this subpart won’t be graded): People have found that, if the delay introduced by one inverter is equal to $\ln 2 \cdot R_{eq,min} \gamma 2C_{g, min}$, then the minimum delay of inverter+wire segments is achieved when the number of stage, $N$, satisfies the following equation:

$$\frac{L}{N} = \sqrt{\frac{2R_{eq,min}2C_{g, min}(1 + \gamma)}{rc}}$$

If we use this conclusion, what would be the $N_{optimum}$ for (b)?

(NOT GRADED)

$$N_{optimum} \approx \sqrt{\frac{rc l^2}{2R_{eq,min}2C_{g, min}(1 + \gamma)}}$$

$$= \sqrt{\frac{0.05 \cdot 0.2 \cdot 10^{-15} \cdot (1.2 \cdot 10^4)^2}{4 \cdot \frac{4444}{\ln 2} \cdot 0.3 \cdot 10^{-15}(1 + 1.5)}} \approx 9 \text{ segments}$$