EECS 151 Disc 5

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Contents

- MOS Transistors
- Switch Networks
- CMOS
- Layout
- Flip-flops
N-MOS and P-MOS

NMOS

PMOS
V-I Characteristics

Note: NMOS is stronger (more current) than PMOS. Wider is stronger.

PMOS works with negative voltages.
More SPICE Simulation

.param your_param 0
.step param your_param 1 9 2

Plots each case (your_param = 1,3,5,7,9) with different colors

Can be combined with .dc to plot multiple curves
Transmission Gate

NMOS is bad at passing 1; PMOS is bad at passing 0 (why?)

Transmission gate:
Tri-state Buffer

Transmission gates do not provide power, accumulating a load on the driver

Alternative: Tri-state buffers
- Pass input to output if enabled
- Oneway
- Use a new power supply (VDD, GND)
Barrel Shifter

Diagram showing the barrel shifter with inputs $x_0, x_1, x_2, x_3$ and outputs $y_0, y_1, y_2, y_3$. The decoder selects the appropriate shift count (shift 0, shift 1, shift 2, shift 3) for each input.
CMOS Logic

The majority of digital logic is implemented using CMOS.

- Pull-up networks: PMOS and VDD
- Pull-down networks: NMOS and GND
NAND2 Gate

Show why this is a NAND gate in two ways:

- By analyzing the PDN
- By analyzing the PUN
NOR2 Gate

Draw a CMOS NOR2 gate.
NOR2 Gate

Draw a CMOS NOR2 gate.
AND-OR-Invert (AOI) Gate

Draw a complex CMOS gate implementing a 2-1 AOI:

Y = (A + B C)’

(Hint: Complement the function for PDN)
AND-OR-Invert (AOI) Gate

\[ Y = (A + B \; C)' = A' \; (B' + C') \]

\[ Y' = A + B \; C \]
n-well: required for making PMOS devices

Vias: vertical connection between layers

Polysilicon: gate connection. Pins connected to the gate will connect to this layer

Diffusion region: represents the source/drain contact areas of the transistor

Metal Routing: metal wires in layout

Power Rails: VDD and VSS supply rails for the cell
Example
Transistor-Level Schematic

\[ X = A_1 \cdot A_2 + B_1 + C_1 + D_1 \]
Flip-Flops
Flip-Flops

clk=0

clk=1