
The Watt: Unit of power. A rate of energy (J/s). A gas pump hose delivers 6 MW.

120 KW: The power delivered by a Tesla Supercharger. Tesla Model S has a 306 MJ battery (good for 265 miles).

1 J = 1 W * s  
1 W = 1 J/s.

Chevy Bolt battery capacity: 66 KWhr = 237 MJ (good for 259 miles).
Energy and Power

Energy is the ability to do work (W).
Power is rate of expending energy.

Energy Efficiency: energy per operation

- **Handheld and portable** (battery operated):
  - Energy Efficiency - limits battery life
  - Power - limited by heat

- **Infrastructure and servers** (connected to power grid):
  - Energy Efficiency - dictates operation cost
  - Power - heat removal contributes to TCO

Remember: $P = IV$
Sad fact: Computers turn electrical energy into heat. Computation is a byproduct.

Energy and Performance

Air or water carries heat away, or chip melts.
1 Joule heats 1 gram of water 0.24 degree C

1 Joule of Heat Energy per Second

The Watt: Unit of power. The rate at which energy dissipated in the resistor.

The Joule: Unit of energy. Can also be expressed as Watt-Seconds. Burning 1 Watt for 100 seconds uses 100 Watt-Seconds of energy.

20 W rating: Maximum power the package is able to transfer to the air. Exceed rating and resistor burns.

This is how electric tea pots work ...
Old example: Cooling an iPod nano ...

Like resistor on last slide, iPod relies on passive transfer of heat from case to the air.

Why? Users don’t want fans in their pocket ...

To stay “cool to the touch” via passive cooling, power budget of 5 W.

If iPod nano used 5W all the time, its battery would last 15 minutes ...
Powering an iPod nano (2005 edition)

1.2 W-hour battery:
Can supply 1.2 watts of power for 1 hour.

1.2 W-hr / 5 W ≈ 15 minutes.

More W-hours require bigger battery and thus bigger “form factor” -- it wouldn’t be “nano” anymore :-).

Real specs for iPod nano:
14 hours for music,
4 hours for slide shows.

85 mW for music.
300 mW for slides.
Apple Watch

3.8 V, 0.78 Whr lithium-ion battery on 38mm model. Apple claims the 205 mAh battery should provide up to 18 hours of use (which translates to 6.5 hours of audio playback, 3 hours of talk time, or 72 hours of Power Reserve mode.)
A clever prism projects a layer over reality light.
2.1 Wh battery – 2.7x as much energy as Apple watch.

Battery life very usage dependent.

640 x 360 Liquid Crystal on Silicon (LCoS) prism projector.

1.76 ounces – 4X the weight of iPod Shuffle

Logic Board
4.7 inch iPhone 6: 1,810mAh battery @3.8V = 6.88 Wh

iPhone 5s: 1570mAh @3.8V = 6 Wh
The A8 is manufactured on a 20 nm process by TSMC. It contains 2 billion transistors. Its physical size is 89 mm^2. It has 1 GB of LPDDR3 RAM included in the package. It is dual core, and has a frequency of 1.38 GHz.

- Apple A8 APL1011 SoC + SK Hynix RAM as denoted by the markings H9CKNNN8KTMRWR-NTH (we presume it is 1 GB LPDDR3 RAM, the same as in the iPhone 6 Plus)
- Qualcomm MDM9625M LTE Modem
- Skyworks 77802-23 Low Band LTE PAD
- Avago A8020 High Band PAD
- Avago A8010 Ultra High Band PA + FBARs
- SkyWorks 77803-20 Mid Band LTE PAD
- InvenSense MP67B 6-axis Gyroscope and Accelerometer Combo
Iphone 12:

https://unitedlex.com/insights/apple-iphone-12-pro-max-teardown-report

<table>
<thead>
<tr>
<th>iPhone Model</th>
<th>Battery Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>iPhone 12 Mini</td>
<td>2,227 mAh</td>
</tr>
<tr>
<td>iPhone 12</td>
<td>2,815 mAh</td>
</tr>
<tr>
<td>iPhone 12 Pro</td>
<td>2,815 mAh</td>
</tr>
<tr>
<td>iPhone 12 Pro Max</td>
<td>3,687 mAh</td>
</tr>
<tr>
<td>iPhone 11</td>
<td>3,110 mAh</td>
</tr>
<tr>
<td>iPhone 11 Pro</td>
<td>3,046 mAh</td>
</tr>
<tr>
<td>iPhone 11 Pro Max</td>
<td>3,969 mAh</td>
</tr>
</tbody>
</table>

14.13 Wh @ 3.8V (Pro Max)
Performance: Must be “close enough” to desktop performance ... most people no longer used a desktop (even in 2006).

Size and Weight. Ideal: paper notebook.

Heat: No longer “laptops” -- top may get “warm”, bottom “hot”. Quiet fans OK.
Battery: Set by size and weight limits ...

Almost full 1 inch depth. Width and height set by available space, weight.

Battery rating: 55 W-hour.

At 2.3 GHz, Intel Core Duo CPU consumes 31 W running a heavy load - under 2 hours battery life! And, just for CPU!

At 1.0 GHz, CPU consumes 13 Watts. "Energy saver" option uses this mode ...

46x more energy than iPod nano battery. And iPod lets you listen to music for 14 hours!
50Wh is 180,000 Joules!
MacBook Air ... design the laptop like an iPod/iPhone
Non-removable, “form-fit” battery...

Mainboard: fills about 25% of the laptop

35 W-h battery: 63% of 2006 MacBook’s 55 W-h
MacBook Air: Full PC

- Thunderbolt I/O
- Platform Controller Hub
- Core i5 CPU/GPU

Up to 4GB DRAM
Machine rooms are expensive. Removing heat dictates how many servers to put in a machine room.

Electric bill adds up! Powering the servers + powering the air conditioners is a big part of TCO.

Reliability: running computers hot makes them fail more often.
Computations per W-h doubles every 1.6 years, going back to the first computer.

(Jonathan Koomey, Stanford).
CMOS Circuits and Energy
Switching Energy: Fundamental Physics

Every logic transition dissipates energy.

How can we limit switching energy?

1. Reduce # of clock transitions. But we have work to do ...
2. Reduce Vdd. But lowering Vdd limits the clock speed ...
3. Fewer circuits. But more transistors can do more work.
4. Reduce C per node. One reason why we scale processes.

Strong result: Independent of technology.
Chip-Level “Dynamic” Power

\[ P_{sw} = \frac{1}{2} \alpha C V_{dd}^2 F \]

- \( P_{sw} \): Power
- \( \alpha \): “activity factor”, average percentage of capacitance switching per cycle (~ number of nodes to switch)
- \( C \): Total chip capacitance to be switched
- \( V_{dd} \): Clock Frequency
- \( F \): Clock Frequency
Additional Dynamic Power - “short circuit current”

When gate switches, brief period when both pullup network and pulldown network could be on.

Worse when input is changing slowly compared to the output.
Another Factor: Leakage Currents

Even when a logic gate isn’t switching, it burns power.

\[ 0V = \text{V}_{\text{IN}} \]

I\text{Gate}: Ideal capacitors have zero DC current. But modern transistor gates are a few atoms thick, and are not ideal.

I\text{Sub}: Even when this nFet is off, it passes an I\text{off} leakage current.

We can engineer any I\text{off} we like, but a lower I\text{off} also results in a lower I\text{on}, and thus a lower maximum clock speed.

Intel’s 2006 processor designs, leakage vs switching power

A lot of work was done to get a ratio this good ... 50/50 is common.

Bill Holt, Intel, Hot Chips 17.
Engineering “On” Current at 25 nm ...

We can increase $I_{on}$ by raising $V_{dd}$ and/or lowering $V_t$.

$I_{ds} = 1.2$ mA = $I_{on}$

$L_{min} = 25$ nm

$I_{off} = 0$ ???

$0.25 = V_t$

$0.7 = V_{dd}$
Plot on a “Log” Scale to See “Off” Current

We can decrease $I_{off}$ by raising $V_t$ - but that lowers $I_{on}$.

$I_{off} \approx 10 \text{ nA}$

$1.2 \text{ mA} = I_{on}$

$0.25 = V_t$

$0.7 = V_{dd}$
Customize processes for product types ...

- $V_t$ is controlled by channel doping.
- Modern IC processes have 2 or 3 different $V_t$ values available.
- Standard cell libraries offer low $V_t$ and high $V_t$ versions of cells so that the tools can optimize on a per instance basis.
- (If high performance not needed then use high $V_t$ to reduce leakage).

Transistor channel is a raised fin.

Gate controls channel from sides and top.

Channel depth is fin width. 12-15nm for L=22nm.
The 20-nm node provides phenomenal benefits in terms of power as well as performance, but the cost is increasing marginally because of elaborate manufacturing to ensure silicon integrity.

Thanks in large part to remarkable research started by Cal Berkeley professor Chenming Hu under a DARPA contract, the 20-nm process will likely be the last hurrah for the planar transistor (at least as we know it today), as the industry moves to FETs built with fins.

**INS AND OUTS OF FINS**

In a planar transistor of today, electrical current flows from source to drain through a flat, 2D horizontal channel underneath the gate. The gate voltage controls current flow through the channel. As transistor size shrinks with the introduction of each new silicon process, the planar transistor cannot adequately stop the flow of current when it is in an "off" state, which results in leakage and heat.

In a FinFET MOSFET transistor, the gate wraps around the channel on three sides, giving the gate much better electrostatic control to stop the current when the transistor is in the "off" state. Superior gate control in turn allows designers to increase the current and switching speed and, thus, the performance of the IC.

Because the gate wraps around three sides of the fin-shaped channel, the FinFET is often called a 3D transistor (not to be confused with 3D ICs, like the Virtex-7 2000T, which Xilinx pioneered with its stacked-silicon technology).

In a three-dimensional transistor (see Figure 1b), gate control of the channel is on three sides rather than just one, as in conventional two-dimensional planar transistors (see Figure 1a). Even better channel control can be achieved with a thinner fin, or in the future with a gate-all-around structure where the channel will be enclosed by a gate on all sides.

The industry believes the 16-nm/14-nm FinFET process will enable a 50 percent performance increase at the same power as a device built at 28 nm. Alternatively, the FinFET device will consume 50 percent less power at the same performance. The performance-per-watt benefits added to the continued increases in capacity make FinFET processes extremely promising for devices at 16 or 14 nm and beyond.

That said, the cost and complexity of designing and manufacturing 3D transistors is going to be higher at least for the short term, as EDA companies figure out ways to adequately model the device characteristics of these new processes and augment their tools and flows to account for signal integrity, electromigration, width quantization, resistance and capacitance. This complexity makes designing ASICs and ASSPs even riskier and more expensive than before.

Xilinx, however, shields users from the manufacturing details. Customers can reap the benefits of increased performance per watt and Xilinx's Generation Ahead design flows to bring innovations based on the new UltraScale architecture to market faster.

**Figure 1** – The position of the gate differs in the two-dimensional traditional planar transistor (a) vs. the three-dimensional FinFET transistor (b).
Dynamic versus Leakage Power

Figure 1: The reduction of feature sizes from 45 to 7nm may induce drastic gains in power consumption and leakage power [Xie2015]

Total Power = \( P_{\text{switching}} + P_{\text{short-circuit}} + P_{\text{leakage}} \)

\[
I_{DS_{\text{Sub}}} = k \cdot e^{\frac{-q \cdot V_T}{a \cdot k_a \cdot T}}
\]
Some low-power design techniques

- Parallelism and pipelining
- Power-down idle transistors
- Slow down non-critical paths
- Thermal management
Trading Hardware for Power

via Parallelism and Pipelining ...
Gate delay roughly linear with Vdd

And so, we can transform this:

Block processes stereo audio. 1/2 of clocks for “left”, 1/2 for “right”.

Into this: Top block processes “left”, bottom “right”.

P ~ #blks × F × V_{dd}^2

P ~ \frac{1}{2} \times \frac{1}{2} \times \frac{1}{4} = \frac{1}{4}

CV^2 power only

THIS MAGIC TRICK BROUGHT TO YOU BY CORY HALL ...
### Summary of Power Consumption and Area

#### Power (normalized)

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple</td>
<td>1</td>
</tr>
<tr>
<td>Parallel</td>
<td>0.36</td>
</tr>
<tr>
<td>Pipelined</td>
<td>0.39</td>
</tr>
<tr>
<td>Pipelined-Parallel</td>
<td>0.2</td>
</tr>
</tbody>
</table>

#### Area (normalized)

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple</td>
<td>1</td>
</tr>
<tr>
<td>Parallel</td>
<td>3.4</td>
</tr>
<tr>
<td>Pipelined</td>
<td>1.3</td>
</tr>
<tr>
<td>Pipelined-Parallel</td>
<td>3.7</td>
</tr>
</tbody>
</table>

#### Voltage

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple</td>
<td>5V</td>
</tr>
<tr>
<td>Parallel</td>
<td>2.9V</td>
</tr>
<tr>
<td>Pipelined</td>
<td>2.9V</td>
</tr>
<tr>
<td>Pipelined-Parallel</td>
<td>2.0</td>
</tr>
</tbody>
</table>

---

From: **Minimizing Power Consumption in CMOS Circuits**

Anantha P. Chandrakasan  
Robert W. Brodersen
Example: Intel Graphics Pipeline IP

A 2.05 GVertices/s 151 mW Lighting Accelerator for 3D Graphics Vertex and Pixel Shading in 32 nm CMOS

Farhana Sheikh, Member, IEEE, Sanu K. Mathew, Member, IEEE, Mark A. Anders, Member, IEEE, Himanshu Kaul, Member, IEEE, Steven K. Hsu, Member, IEEE, Amit Agarwal, Member, IEEE, Ram K. Krishnamurthy, Fellow, IEEE, and Shekhar Borkar, Fellow, IEEE
A 2.05 GVertices/s 151 mW Lighting Accelerator for 3D Graphics Vertex and Pixel Shading in 32 nm CMOS

Farhana Sheikh, Member, IEEE, Sanu K. Mathew, Member, IEEE, Mark A. Anders, Member, IEEE, Himanshu Kaul, Member, IEEE, Steven K. Hsu, Member, IEEE, Amit Agarwal, Member, IEEE, Ram K. Krishnamurthy, Fellow, IEEE, and Shekhar Borkar, Fellow, IEEE
Voltage Scaling

\[ P_{sw} = \frac{1}{2} \alpha C V_{dd}^2 F \]

Reducing \( F \), reduces power, but our computation now takes longer, and total energy does not change.

Reducing both \( F \) and \( V_{dd} \), reduces power but also improves energy efficiency (total energy for computation is less).

Parallelism gives us a way to make up for lower performance from voltage scaling.
Multiple Cores for Low Power

Trade hardware for power, on a large scale ...
Cell: The PS3 chip
Cell (PS3 Chip): 1 CPU + 8 “SPUs”

- L2 Cache
  - 512 KB

- 8 Synergistic Processing Units (SPUs)

- PowerPC
A “Schmoo” plot for a Cell SPU ...

The lower Vdd, the less dynamic energy consumption.

\[ E_{0\rightarrow1} = \frac{1}{2} CV_{dd}^2 \]

The lower Vdd, the longer the maximum clock period, the slower the clock frequency.

\[ E_{1\rightarrow0} = \frac{1}{2} CV_{dd}^2 \]

\[ Freq (GHz) \]

\[ Vdd (Volts) \]

Failed
Clock speed alone doesn’t help E/op ...

But, lowering clock frequency while keeping voltage constant spreads the same amount of work over a longer time, so chip stays cooler ...

\[ E_{0\rightarrow 1} = \frac{1}{2} C V_{dd}^2 \quad E_{1\rightarrow 0} = \frac{1}{2} C V_{dd}^2 \]
Scaling $V$ and $f$ does lower energy/op.

<table>
<thead>
<tr>
<th>$V_{dd}$ (Volts)</th>
<th>0.9</th>
<th>1.0</th>
<th>1.1</th>
<th>1.2</th>
<th>1.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 W</td>
<td>25C</td>
<td>26C</td>
<td>26C</td>
<td>26C</td>
<td>27C</td>
</tr>
<tr>
<td>2.2 GHz performance</td>
<td>26C</td>
<td>26C</td>
<td>27C</td>
<td>27C</td>
<td>27C</td>
</tr>
<tr>
<td>7 W</td>
<td>48C</td>
<td>49C</td>
<td>50C</td>
<td>50C</td>
<td>51C</td>
</tr>
<tr>
<td>2.2 GHz performance</td>
<td>49C</td>
<td>50C</td>
<td>52C</td>
<td>53C</td>
<td>54C</td>
</tr>
</tbody>
</table>

If a program that needs a 4.4 GHz CPU can be recoded to use two 2.2 GHz CPUs ... big win.

- 1 W to get 2.2 GHz performance, 26 C die temp.
- 7 W to reliably get 4.4 GHz performance, 47 C die temp.
Dynamic Voltage/Frequency Scaling (DVFS)

Many modern processors have controls for dynamically changing operating frequency and voltage.

Intel power states

- BIO/OS software can adjust frequency to reduce heat and/or improve power efficiency with high performance not needed.
- Adjusting both voltage and frequency helps improve energy efficiency and allows higher frequency for a given power level.
Powering down idle circuits
Add “sleep” transistors to logic ...

Example: Floating point unit logic.

When running fixed-point instructions, put logic “to sleep”.

+++ When “asleep”, leakage power is dramatically reduced.

--- Presence of sleep transistors slows down the clock rate when the logic block is in use.
Intel example: Sleeping cache blocks

SRAM Cache Block

NMOS Sleep Transistor

\[ V_{DD} \]

\[ V_{SS} \]

70 Mbit SRAM leakage current map

Without sleep transistor

With sleep transistor

Accessed block

>3x SRAM leakage reduction on inactive blocks

A tiny current supplied in “sleep” maintains SRAM state.

CPU Power Management

The 32nm CPU in the Intel® Atom™ Processor Z2480 is a process-shrink of the original 45nm Atom™ micro-architecture [5]. The 32nm CPU doubled the size of the Gshare branch predictor to 8K entries and optimized memory copy performance. Additional low-power enhancements include operating the CPU at lower minimum voltage, reducing active power of the CPU PLL, separating voltage rails for CPU and the L2 cache, and enabling full power-gating of the CPU in the C6 standby mode. This section highlights the results of these low-power optimizations, and how they apply to smartphone use cases.

As shown in Figure 5, the Intel® Atom™ CPU provides a wide dynamic performance/power operating range. On Medfield, fine-grained active CPU power management is accomplished through dynamic frequency voltage scaling that is controlled by Enhanced Intel® SpeedStep® Technology [7], also known as CPU P-states. The dynamic range of the CPU ranges from 600MHz @ ~175mW to a sustained high frequency mode (HFM) of 1.3GHz @ ~500mW. For bursty workloads (e.g., interactive use of a web browser) the CPU can burst up to 2.0GHz @ ~1,200mW for short periods of time.

As long as thermal headroom allows, the CPU can run in burst mode until thermal monitors in the platform, the SoC, or the CPU indicate that thermal design power limits have been reached. When this occurs, a combination of firmware and software throttle the CPU back into a lower P-state. Additionally, CPU w/512KB L2$
Intel Medfield

Switches 45 power “islands.”

Fine-grained control of leakage power, to track user activity.

“Race to idle” strategy -- finish tasks quickly, to get to power down.

![Image of smartphone reference design]
Playing a game ...

Active system looks like this
Watching a video ...

Active system looks like this

- Security Engine
- Power Manager
- Low Power Audio
- Storage
- CPU w/512KB L2$
- 2D/3D Graphics
- Video Encode/Decode (1080p30)
- Image Signal Processor
- Display Controller (3 pipes)

CPU is now off!
Looking at phone screen, not doing anything ...

S0i1 – low activity

CPU w/512KB L2$

Storage

Security Engine

Power Manager

Low Power Audio

2D/3D Graphics

Image Signal Processor

Video Encode/Decode (1080p30)

Display Controller (3 pipes)

Digital Object Indentifier 10.1109/MM.2013.22
0272-1732/$26.00 2013 IEEE

This article has been accepted for publication in IEEE Micro but has not yet been fully edited. Some content may change prior to final publication.
Phone in your pocket, waiting for a call ...

**Figure 8 – S0i1 System State with power consumption in the mW range**

**Figure 9 – S0i3 System State with power consumption in the uW range**

Standby State – just waiting for wakes
Slow down “slack paths”
Fact: Most logic on a chip is “too fast”

The critical path

Most logic paths have hundreds of picoseconds to spare.

Use several supply voltages on a chip ...

Why use multi-Vdd? We can reduce dynamic power by using low-power Vdd for logic off the critical path.

In practice, instead of multi-Vdd design ...
In a multi-Vt process, we can reduce leakage power on the off critical path logic by using high-Vth transistors.
Thermal Management
Keep chip cool to minimize leakage power

A recipe for thermal runaway

<table>
<thead>
<tr>
<th>Junction Temperature (T_J °C)</th>
<th>Normalized Static Power or I_{CCINTQ} Typical</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>1.00</td>
</tr>
<tr>
<td>50</td>
<td>1.46</td>
</tr>
<tr>
<td>85</td>
<td>2.50</td>
</tr>
<tr>
<td>100</td>
<td>3.14</td>
</tr>
</tbody>
</table>

Figure 3: \( I_{CCINTQ} \) vs. Junction Temperature with Increase Relative to 25°C

Optimizing Designs for Power Consumption through Changes to the FPGA Environment
Intel realtime temp monitoring

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPUID</td>
<td>306C3</td>
</tr>
<tr>
<td>Frequency</td>
<td>3591.683 MHz</td>
</tr>
<tr>
<td>Threads</td>
<td>8</td>
</tr>
<tr>
<td>Load</td>
<td>12.9%</td>
</tr>
<tr>
<td>GPU Temperature</td>
<td>36°C</td>
</tr>
<tr>
<td>CPU Temperature</td>
<td>45°C</td>
</tr>
<tr>
<td>Temperature (°C)</td>
<td>45°C, 45°C, 49°C, 62°C, 62°C</td>
</tr>
<tr>
<td>Package Temperature (°C)</td>
<td>55°C</td>
</tr>
<tr>
<td>Distance to TJ Max</td>
<td>55°C, 55°C, 51°C, 38°C, 38°C</td>
</tr>
<tr>
<td>Minimum Temperature</td>
<td>39°C, 38°C</td>
</tr>
<tr>
<td>Minimum Time</td>
<td>14:57:03, 14:57:49</td>
</tr>
<tr>
<td>Maximum Temperature</td>
<td>61°C, 62°C</td>
</tr>
<tr>
<td>Thermal Status</td>
<td>OK, OK, OK, OK, OK</td>
</tr>
</tbody>
</table>

Intel® Turbo Boost Technology

Intel® Core™ i7 processor 2.40 GHz

Intel® Core™ i7-4700MQ

CPUID 306C3
Threads 8
Temperature (°C) 45°C, 45°C, 49°C, 62°C, 62°C
Package Temperature 55°C
Distance to TJ Max 55°C, 55°C, 51°C, 38°C, 38°C
Minimum Temperature 39°C, 38°C
Minimum Time 14:57:03, 14:57:49
Maximum Temperature 61°C, 62°C
Thermal Status OK, OK, OK, OK, OK

Sensor Test  Testing...  C States  Cancel  Options