Lecture 25:
Clocks, Packaging, and Power Distribution
Announcements

- Homework assignment 10 posted - due next Monday.
- HW 11 - final problem set - posted end of this week.
- Final project checkoffs will be Thursday of next week (RRR).
- Final reports will be due Monday at midnight of exam week.
- Apple has generously offered to offer prizes for the best projects this semester:
  - The top ASIC project (2 students), & the top 3 FPGA projects (6 students)
  - The student can choose either an Apple Watch (SE GPS, 40mm) or Airpod Pro.
# Announcements

- **End game:**

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Outline

- Clock non-idealities
- Clock Distribution
- Chip packaging
- Power Distribution
Synchronous Timing
- Review
Synchronous Timing

CLK

In

R₁

Cᵢₙ

Combinational Logic

Cₒᵤₜ

R₂

Out
Register Timing Parameters

Output delays can be different for rising and falling data transitions
Timing Constraints

The diagram illustrates a timing analysis of a circuit with inputs and outputs labeled as follows:

- **In**: Input signal
- **CLK**: Clock signal
- **R1**: First register
  - $D$: Data input
  - $Q$: Output
- **R2**: Second register
  - $D$: Data input
  - $Q$: Output
- **Combinational Logic**: The part of the circuit that performs the logic operations

Key timing constraints are as follows:

- $t_{clk-q\_max}$
- $t_{clk-q\_min}$
- $t_{setup}$
- $t_{hold}$
- $t_{logic\_max}$
- $t_{logic\_min}$

The timing constraints are represented by:

- $t_{CLK_1}$
- $t_{CLK_2}$

These constraints ensure proper operation and timing correctness in the circuit.
Timing Constraints

Cycle time: $T_{Clk} > t_{clk-q,max} + t_{logic,max} + t_{setup}$

Race margin: $t_{hold} < t_{clk-q,min} + t_{logic,min}$
Clock Nonidealities
Clock Nonidealities

- **Clock skew**: $t_{SK}$
  - Time difference between the arrival time of the clock signal at sink two different receivers

- **Clock jitter**
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
  - Cycle-to-cycle (short-term) $t_{JS}$
  - Long term $t_{JL}$

- **Variation of the pulse width**
  - Important for level sensitive clocking
Clock Uncertainties

Sources of clock uncertainty

1. Clock Generation
2. Device Variation
3. Interconnect
4. Power Supply
5. Temperature
6. Capacitive Load
7. Coupling to Adjacent Lines
Clock Skew and Jitter

- Both skew and jitter affect the effective cycle time and the race margin
Positive Skew

Launching edge arrives before the receiving edge
Negative Skew

Receiving edge arrives before the launching edge
Timing Constraints

Minimum cycle time:
\[ T_{\text{clk}} + \delta = t_{\text{clk-q, max}} + t_{\text{setup}} + t_{\text{logic, max}} \]

Skew may be negative or positive
Timing Constraints

Hold time constraint:
\[ t_{\text{clk-q,min}} + t_{\text{logic,min}} > t_{\text{hold}} + \delta \]

Skew may be negative or positive
Jitter Contributes to Critical Path

Latest point of launching

$\text{Clk1}$

$\text{Clk2}$

$t_{JS1}$

$t_{clk-Q,max}$

$t_{logic,max}$

$T_{CLK}$

$t_{setup}$

$t_{JS2} - \delta$

Earliest arrival of next cycle
Clock Constraints in Edge-Triggered Systems

If launching edge is late and receiving edge is early, the data will not be too late if:

\[ t_{clk-q,\text{max}} + t_{\text{logic, max}} + t_{\text{setup}} < T_{CLK} - t_{JS,1} - t_{JS,2} + \delta \]

Minimum cycle time is determined by the maximum delays through the logic

\[ t_{clk-q,\text{max}} + t_{\text{logic, max}} + t_{\text{setup}} - \delta + 2t_{JS} < T_{CLK} \]

Skew can be either positive or negative

Jitter \( t_{JS} \) usually expressed as peak-to-peak or \( n \times \text{RMS} \) value
Datapath with Feedback

Negative skew

Positive skew
Clock distribution

In

Out
Clock Distribution
Clock Distribution

- Single clock generally used to synchronize all logic on the same chip (or region of chip)
  - Need to distribute clock over the entire region
  - While maintaining low skew/jitter
  - And without burning too much power
What’s wrong with just routing wires to every point that needs a clock?
H-Tree

Equal wire length/number of buffers to get to every location
More realistic ASIC H-tree

[Restle98]
Chip Packaging
Chip Packaging

- Bond wires (~25μm) sometimes used to connect the package to the chip
- Pads are arranged in a frame around the chip
- Pads are relatively large
  - ~100μm in 0.25μm technology, with 100μm pitch
  - 60μm x 80μm at 80μm pitch in 45nm
- Many chips are ‘pad limited’
Pad Frame

Layout

Die Photo
Chip Packaging

- Newer alternative is ‘flip-chip’:
  - Pads are distributed around the chip
  - The solder balls are placed on pads
  - The chip is ‘flipped’ onto the package
  - Pads still large
    - But can have many more of them
Bonding Pad Design

Bonding Pad

$V_{DD}$

Out

In

GND

GND

Out

100 µm

$100 \mu m$
ESD Protection

- When a chip is connected to a board or otherwise handled, there is unknown (potentially large) static voltage difference (a few kV)
- Equalizing potentials requires (large) charge flow through the pads
- Diodes sink this charge into the substrate – need guard rings to pick it up.

*The Design and Analysis of VLSI Circuits, Glasser and Dobberpuhl*
Pads + ESD Protection

Diode

PAD

$V_{DD}$

$D1$

$D2$

$R$

$X$

$C$
When Things Go Bad

[Maxim]
Power Distribution
Power Supply Distribution Issues

- IR drops
  - Voltage drops due to resistance in power wires
    - Slower circuits, false switching
  - Metal Migration (electromigration)
    - chip failures
- Inductive Effects
  - bounce and oscillations on power nodes

All effects are helped by shorter thicker wires. Modern processes have special thick metal layers dedicated to power distribution. Area pads help keep connections to package short and distance from pad to circuit short.
Power Delivery

- Achieving good reliable power delivery requires a lot of resources:
  - ~70% of package pins just for power
  - Top 2-3 (thick) metal layers

All effects are helped by shorter thicker wires. Modern processes have special thick metal layers dedicated to power distribution. Area pads help keep connections to package short and distance from pad to circuit short.
Electromigration

- If current density is too high - wires melts

- “On-chip wires: current limited to \( \sim 1 \text{mA/\mu m} \) for 5-7 year lifetime
Power Supply Impedance (Z)

- Two principal elements increase Z:
  - Resistance of supply lines ($V = IR$ drop)
  - Inductance of supply lines ($V = L \cdot \text{di}/\text{dt}$ drop)
Power Supply Impedance

- IR voltage drop
- Slower circuit operation because of series resistance with transistors:

\[ \tau = (R_w + R_p) C_L \]

- IR drops generate “noise”:

![Circuit Diagram]
Typical target for supply impedance is to get 5-10% voltage variation of nominal supply (e.g., 100mV for 1V supply)

- In traditional scaling $V_{dd}$ drops while power stays constant.
- This forced drastic drop in required supply impedance:
  - $V_{dd} \downarrow$, $I_{dd} \uparrow \rightarrow |Z_{\text{required}}| \downarrow \downarrow$

Extreme example:
- $V_{dd} = 1V$, $P=100W \Rightarrow I_{dd}=100A$
- For $\Delta V_{dd,\text{max}} = 100mV$, 
  $Z_{dd,\text{max}} = 100mV/100A = 1m\Omega$
IR Drop Example

- Intel Pentium 4: ~103W at ~1.275V
  \( I_{dd} = 81 \text{Amps} \)

- For 10% IR drop, total distribution resistance must be less than 1.6m\(\Omega\)

- On-chip wire \( R \approx 20m\Omega/\text{sq. (thick metal)} \)
  - Can’t meet \( R \) requirement even with multiple, complete layers dedicated to power
  - Main motivation for flip-chip packaging
Layout Strategy

1. Keep distance form source of power/gnd as short as possible.
2. Use wide thick metal.
3. Isolate “noisy” sections.
4. Use multiple sources.
Popular On-Chip Power

- Power network usually follows pre-defined template (often referred to as “power grid”)
Inductive Bounce

Inductance in the power & ground paths results in voltage glitches (noise) on the Vdd & GND nodes.

On chip L value of wires is small => usually not significant except:

1. Very large currents: clock drivers, off-chip drivers
2. Package pins, bonding wires (1nH/mm)

Package pins can have from 2 - 40nH of inductance, depending on package type

Strategy:

1. Use multiple bonding pads (wiress) for Vdd and GND
2. Use on -chip by pass capacitors
Pin Inductance

- Major source of inductance is through the bonding pin connections to the chip package.
- C4 bump inductance is 25pH
- Wire-bond inductance of 1nH/mm

Example:
- Processor transient current is 50A in 20ps from 1V supply
- How many C4 bumps do we need to get supply noise spike of less than 10%?
- With wirebonds, how many wirebonds are needed?
Pin Inductance Example

- Processor transient current is 50A in 20ps from 1V supply:

\[ V = L \cdot \frac{dI}{dt} \]
\[ L = V \cdot \frac{dt}{dI} = 0.1V \cdot \frac{20\text{ps}}{50\text{A}} = 0.04\text{pH} \]

- C4 bump inductance is 25pH

- How many C4 bumps do we need to get supply noise spike of less than 10%?

\[ \frac{25\text{pH}}{0.04\text{pH}} = 625 \text{ C4 bumps} \]

\[ \frac{1000\text{pH}}{0.04\text{pH}} > 25K! \text{ bonding wires} \]
On-chip Decoupling Capacitors Help with Inductive and Resistive Effects

- When transistors switch, current is drawn from $C_D$ rather than through package pins and bonding wires - smooths our $dl/dt$.

- Distributed bypass capacitors also smooth out noise from IR drops.

Decap cell in stdcell library added by tools.
Decoupling Capacitors On-chip and on-board

Decoupling capacitors are added:

- On the board (right under the supply pins)
- On the chip (under the supply straps, near large buffers)
- $C_d$ helps avoid current rushing through supply wires
  - Local store of charge
  - “Smoothing filter” on supply voltage
Decoupling Capacitors

- Under the die