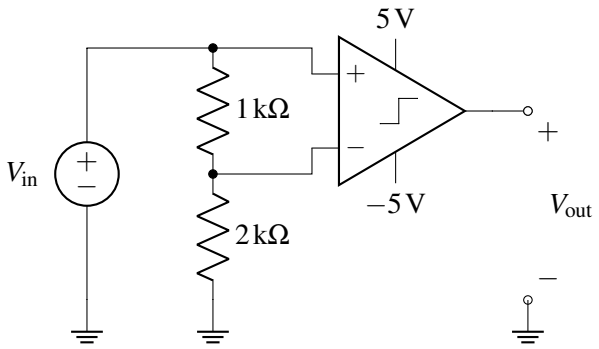
EECS 16A Designing Information Devices and Systems I
Fall 2021 Discussion 9B

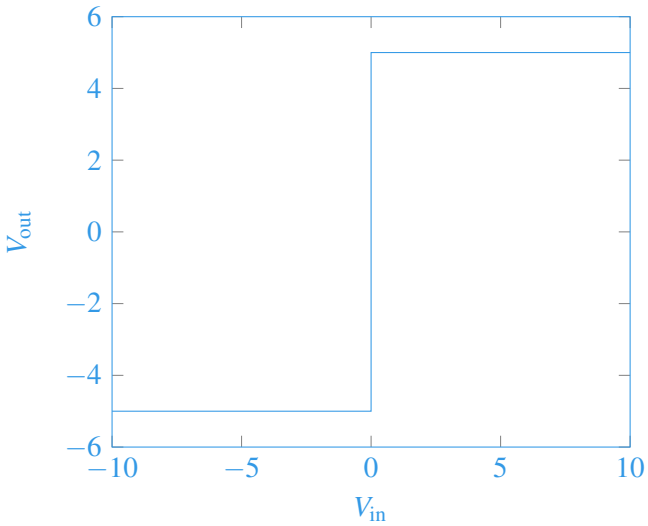
1. Comparators

For each of the circuits shown below, plot V_{out} for V_{in} ranging from $-10\,V$ to $10\,V$ for part (a) and from $0\,V$ to $10\,V$ for part (b).

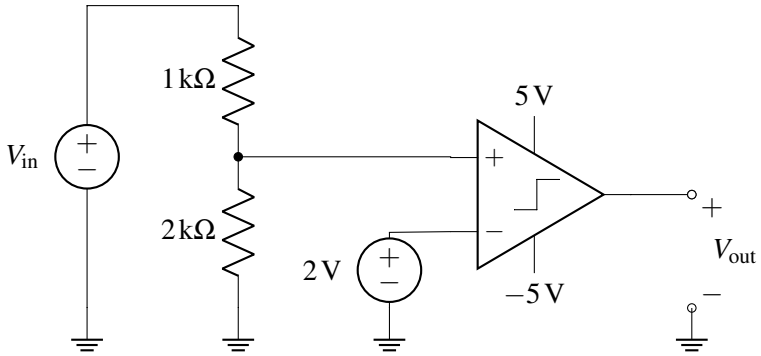
(a)



When the positive terminal's voltage, V_+, is greater than the negative terminal's voltage, V_-, the output voltage would be at the positive supply rail, V_{DD}. Likewise, if the negative terminal's voltage, V_-, has a higher voltage then the value at the negative supply rail, the output voltage would be V_{SS}. Since V_- is just the output of a voltage divider with the source $V_{in} = V_+$, it will always have lower absolute value and same polarity as the positive terminal. Thus, the comparator's output will depend only on the sign of the source V_{in}.



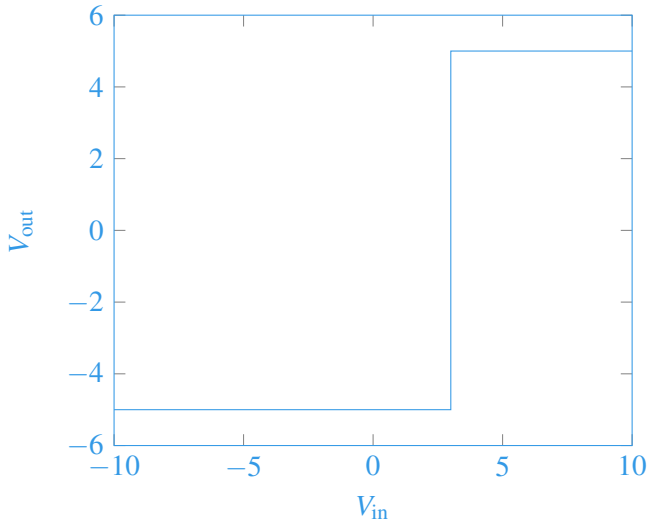
(b)



$$V_+ = \frac{2\,\text{k}\Omega}{1\,\text{k}\Omega + 2\,\text{k}\Omega} V_{in} = \frac{2}{3} V_{in}$$

$$V_- = 2\,\text{V}$$

The comparator will output positive 5V when the voltage divider's output $V_+ > 2\,\text{V}$ and thus when $V_{in} > 3\,\text{V}$. Otherwise, it will output -5V.



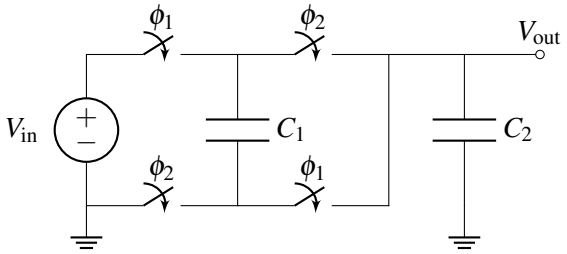
2. Charge Sharing

Recipe for charge sharing:

Step 1: Label the voltages across all the capacitors. Choose whichever direction (polarity) you want for each capacitor - this means you can mark any one of the plates with the "+" sign, and then you can mark the other plate with the "−" sign. Just make sure you stay consistent with this polarity across phases.
Step 2: Draw the equivalent circuit during both phases (Phase 1: ϕ_1 closed, ϕ_2 open - Phase 2: ϕ_1 open, ϕ_2 closed). Also, label all node voltages on the circuit for both phases. No need to try and maintain the same names, since certain nodes of the phase 1 circuit might be merged or split in phase 2.
Step 3: Calculate the note voltages during phase 1. This can be done by using one of the previously introduced circuit analysis techniques (most likely KVL will do the job).

Step 4: Identify all "floating" nodes in your circuit during phase 2. A floating node is a node out of or into which no charge can flow. You can identify those nodes as the nodes connected only to capacitor plates, op amp inputs or comparator inputs. These will be the nodes where we apply charge sharing.
Step 5: For steps 5-7 we will **examine each phase 2 floating node individually**. Pick a floating node from the ones you found in step 4 and identify all capacitor plates connected to that node during phase 2. Then, calculate the charge on each of these plates during phase 1.
To do so, identify all nodes in your circuit during phase 1. Label all node voltages, and write the voltages across each capacitor as functions of node voltages (step 2 and 3 should help you with that). Do this according to the polarities you have selected. Then the charge is found as $Q = CV_C$ (where V_C is the voltage *across* a capacitor).
Careful: The plate marked with the "$-$" sign will have $Q = -CV_C$ and the plate marked with the "$+$" sign will have $Q = CV_C$ stored onto them.
Step 6: Find the total charge on each of the floating nodes during phase 2 as a function of node voltages. Use the same process as in Step 5, but this time using the node voltages during phase 2 to write the voltages across each capacitor. Make sure you kept the polarity same and pay attention to the sign of each plate.
Step 7: Equate the total charge calculated in phase 1 (Step 4) to the total charge calculated in phase 2 (Step 6) (charge conservation).
Step 8: Repeat steps 5-7 for every floating node. This will give you one equation per floating node (i.e. if you have m floating nodes you will have m equations). You can then solve the system of equations to find the node voltages during phase 2 (unknowns). It should have a unique solution!

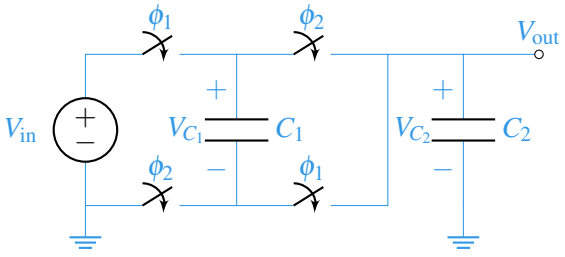
Consider the circuit shown below. In phase ϕ_1, the switches labeled ϕ_1 are on while the switches labeled ϕ_2 are off. In phase ϕ_2, the switches labeled ϕ_2 are on while the switches labeled ϕ_1 are off.



(a) Draw the polarity of the voltage (using $+$ and $-$ signs) across the two capacitors C_1 and C_2. (It doesn't matter which terminal you label $+$ or $-$; just remember to keep these consistent through phase 1 and 2!)

Step 1 of the recipe.

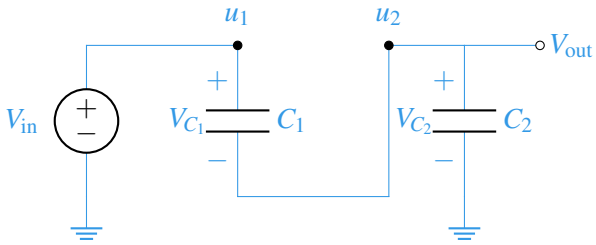
One way of marking the polarities is $+$ on the top plate and $-$ on the bottom plate of both C_1 and C_2. Let's call the voltage drop across C_1 V_{C_1} and across C_2 V_{C_2}.



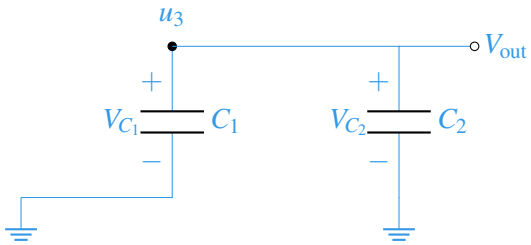
(b) Redraw the circuit in phase ϕ_1 and phase ϕ_2. Keep your polarity from part (a) in mind.

Step 2 of the recipe.

Phase ϕ_1



Phase ϕ_2



(c) Find V_{out} in phase ϕ_2 as a function of V_{in}, C_1, and C_2.

Steps 4-7 of the recipe.

First, we must identify the floating node in phase ϕ_2. For this circuit, the floating node is u_3, as we can see that charge on the "+" plates of C_1 and C_2 cannot flow to ground.

Now that we know what plates are connected to our floating node, we must find the charge on those plates in phase ϕ_1. The two capacitors in series have a total capacitance of $C_{eq} = \frac{C_1 C_2}{C_1+C_2}$. We know that there is a voltage of V_{in} across this capacitor and thus $Q_{C_{eq}} = V_{\text{in}} \frac{C_1 C_2}{C_1+C_2}$ charge. Because they're in series, we know that the charge across the equivalent capacitance is the same as a charge across each individual capacitor. Since we are looking for the charge on the "+" terminals of those capacitors it will be:

$$\begin{aligned} Q_{u_3}^{\phi_1} &= Q_{C_1} + Q_{C_2} \\ &= 2Q_{C_{eq}} \\ &= 2V_{\text{in}} \frac{C_1 C_2}{C_1 + C_2} \end{aligned}$$

Similarly, we must find the charge on those plates in phase ϕ_2.

$$\begin{aligned} Q_{u_3}^{\phi_2} &= V_{C_1} C_1 + V_{C_2} C_2 \\ &= (u_3 - 0)C_1 + (u_3 - 0)C_2 \\ &= (V_{\text{out}} - 0)C_1 + (V_{\text{out}} - 0)C_2 \\ &= V_{\text{out}}(C_1 + C_2) \end{aligned}$$

Because of the conservation of charge, we can equate the total charge in phase ϕ_1 and phase ϕ_2.

$$\begin{aligned} Q_{u_3}^{\phi_1} &= Q_{u_3}^{\phi_2} \\ 2V_{\text{in}}\frac{C_1C_2}{C_1+C_2} &= V_{\text{out}}(C_1+C_2) \\ V_{\text{out}} &= 2\frac{C_1C_2}{(C_1+C_2)^2}V_{\text{in}} \end{aligned}$$

(d) How will the charges be distributed in phase ϕ_2 if we assume $C_1 \gg C_2$?

We know that the capacitors are in parallel in phase ϕ_2, so the voltage across both capacitors is the same. Considering that $Q = CV$, if $C_1 \gg C_2$, then $Q_1 \gg Q_2$.