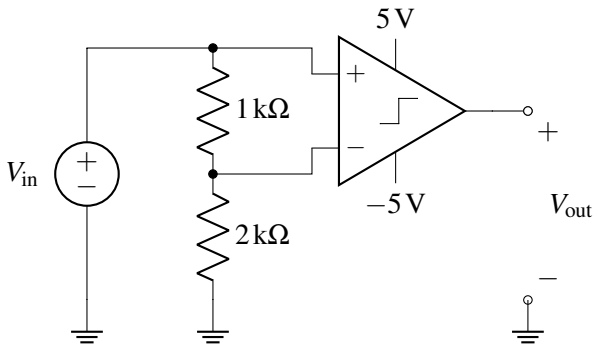
EECS 16A Designing Information Devices and Systems I
Fall 2021 Discussion 9B

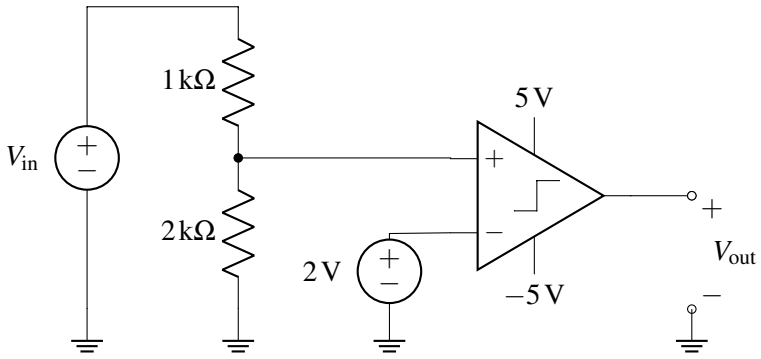
1. Comparators

For each of the circuits shown below, plot V_{out} for V_{in} ranging from $-10\,V$ to $10\,V$ for part (a) and from $0\,V$ to $10\,V$ for part (b).

(a)



(b)



2. (Optional) Charge Sharing

Recipe for charge sharing:

Step 1: Label the voltages across all the capacitors. Choose whichever direction (polarity) you want for each capacitor - this means you can mark any one of the plates with the "+" sign, and then you can mark the other plate with the "−" sign. Just make sure you stay consistent with this polarity across phases.
Step 2: Draw the equivalent circuit during both phases (Phase 1: ϕ_1 closed, ϕ_2 open - Phase 2: ϕ_1 open, ϕ_2 closed). Also, label all node voltages on the circuit for both phases. No need to try and maintain the same names, since certain nodes of the phase 1 circuit might be merged or split in phase 2.
Step 3: Calculate the note voltages during phase 1. This can be done by using one of the previously introduced circuit analysis techniques (most likely KVL will do the job).
Step 4: Identify all "floating" nodes in your circuit during phase 2. A floating node is a node out of or into which no charge can flow. You can identify those nodes as the nodes connected only to capacitor plates, op

amp inputs or comparator inputs. These will be the nodes where we apply charge sharing.

Step 5: For steps 5-7 we will **examine each phase 2 floating node individually**. Pick a floating node from the ones you found in step 4 and identify all capacitor plates connected to that node during phase 2. Then, calculate the charge on each of these plates during phase 1.

To do so, identify all nodes in your circuit during phase 1. Label all node voltages, and write the voltages across each capacitor as functions of node voltages (step 2 and 3 should help you with that). Do this according to the polarities you have selected. Then the charge is found as $Q = CV_C$ (where V_C is the voltage *across* a capacitor).

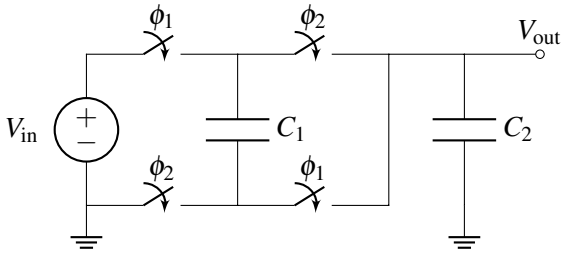
Careful: The plate marked with the "$-$" sign will have $Q = -CV_C$ and the plate marked with the "$+$" sign will have $Q = CV_C$ stored onto them.

Step 6: Find the total charge on each of the floating nodes during phase 2 as a function of node voltages. Use the same process as in Step 5, but this time using the node voltages during phase 2 to write the voltages across each capacitor. Make sure you kept the polarity same and pay attention to the sign of each plate.

Step 7: Equate the total charge calculated in phase 1 (Step 4) to the total charge calculated in phase 2 (Step 6) (charge conservation).

Step 8: Repeat steps 5-7 for every floating node. This will give you one equation per floating node (i.e. if you have m floating nodes you will have m equations). You can then solve the system of equations to find the node voltages during phase 2 (unknowns). It should have a unique solution!

Consider the circuit shown below. In phase ϕ_1, the switches labeled ϕ_1 are on while the switches labeled ϕ_2 are off. In phase ϕ_2, the switches labeled ϕ_2 are on while the switches labeled ϕ_1 are off.



(a) Draw the polarity of the voltage (using $+$ and $-$ signs) across the two capacitors C_1 and C_2. (It doesn't matter which terminal you label $+$ or $-$; just remember to keep these consistent through phase 1 and 2!)

(b) Redraw the circuit in phase ϕ_1 and phase ϕ_2. Keep your polarity from part (a) in mind.

(c) Find V_{out} in phase ϕ_2 as a function of V_{in}, C_1, and C_2.

(d) How will the charges be distributed in phase ϕ_2 if we assume $C_1 \gg C_2$?