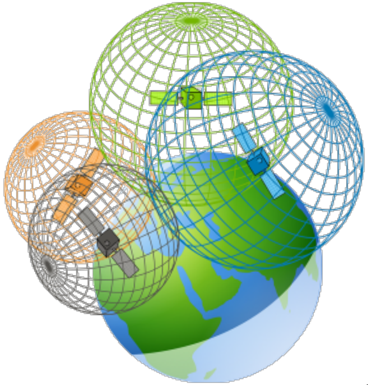

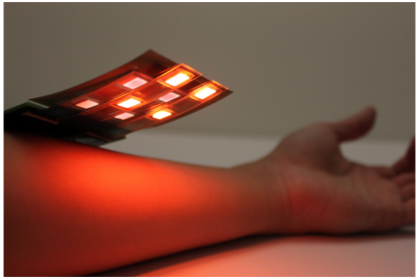

Welcome to EECS 16A!

Designing Information Devices and Systems I

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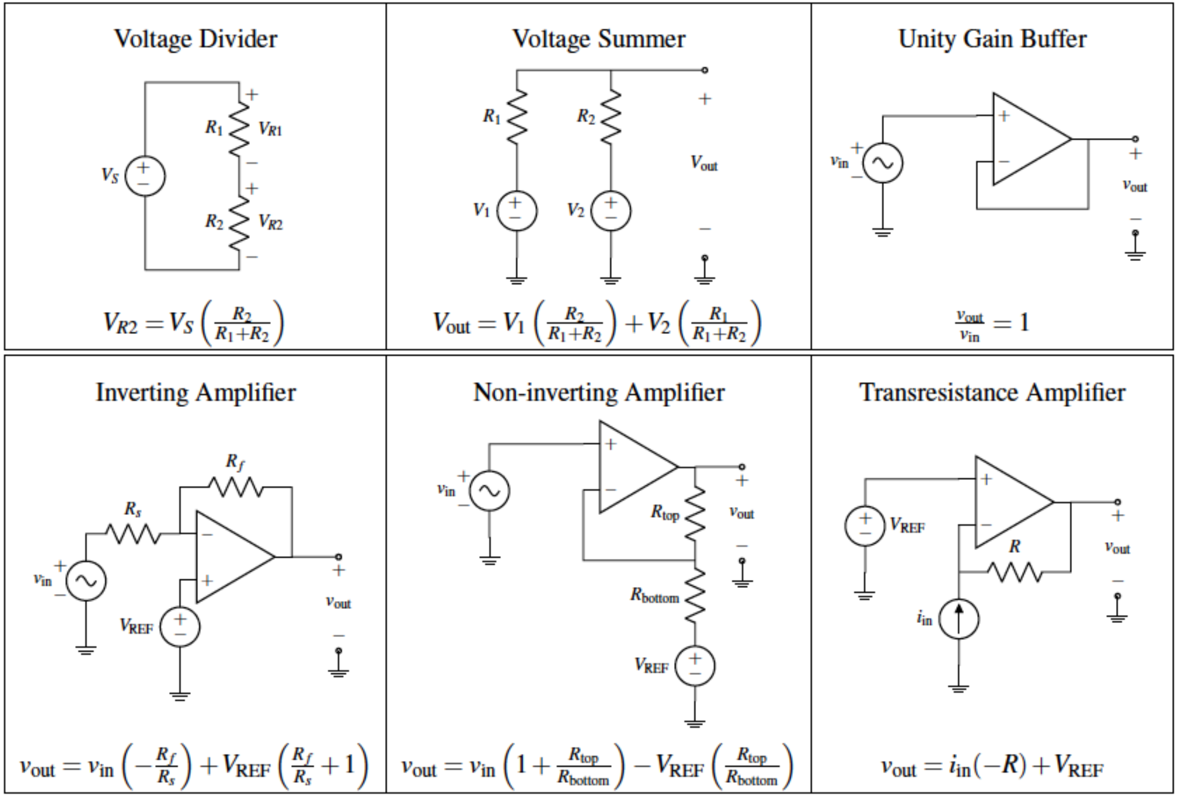
Fall 2021

Module 2
Lecture 12
Design Procedure and Examples (Note 20)

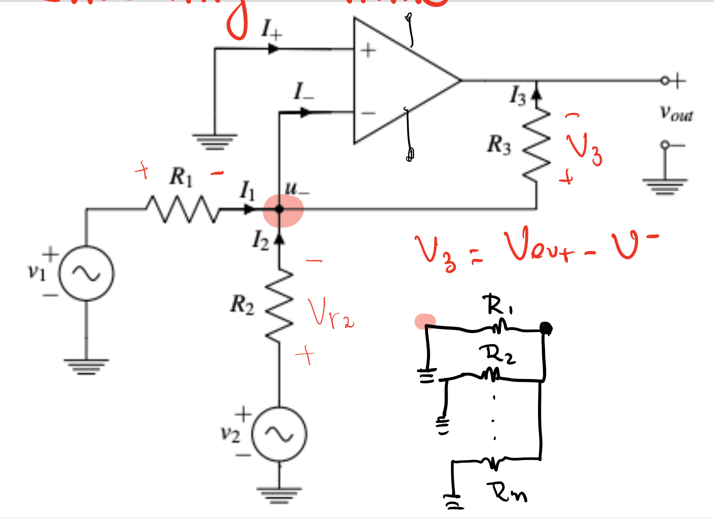
Today


Voltage Divider
$V_{R2} = V_S \left(\frac{R_2}{R_1+R_2}\right)$
Voltage Summer
$V_{out} = V_1 \left(\frac{R_2}{R_1+R_2}\right) + V_2 \left(\frac{R_1}{R_1+R_2}\right)$
Unity Gain Buffer
$\frac{v_{out}}{v_{in}} = 1$
Inverting Amplifier
$v_{out} = v_{in}\left(-\frac{R_f}{R_s}\right) + V_{REF}\left(\frac{R_f}{R_s}+1\right)$
Non-inverting Amplifier
$v_{out} = v_{in}\left(1+\frac{R_{top}}{R_{bottom}}\right) - V_{REF}\left(\frac{R_{top}}{R_{bottom}}\right)$
Transresistance Amplifier
$v_{out} = i_{in}(-R) + V_{REF}$

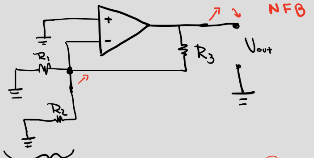
Artificial Neuron

- Neurons in our brain are interconnected.
- The output of a single-neuron is dependent on inputs from several other neurons.
- This idea is represented with vector-vector multiplication – the output is a linear combination of several inputs.
- An artificial neuron circuit must perform addition

Inverting summer



Check for NFB:



$V^+ = V^-$: GR2

$V^+ = 0 \Rightarrow V^- = 0$

KCL: $\frac{V^- - V_1}{R_1} + \frac{V^- - V_2}{R_2} = I^- + \frac{V_{out} - V^-}{R_3}$

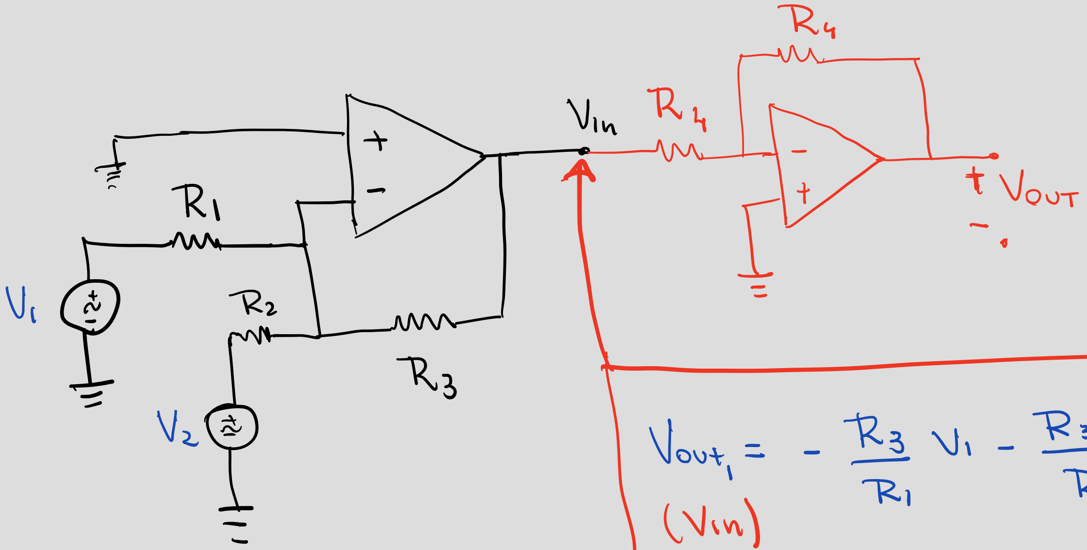
$$-\frac{V_1}{R_1} - \frac{V_2}{R_2} = \frac{V_{out}}{R_3}$$

$$V_{out} = -\frac{R_3}{R_1} \cdot V_1 + \left(-\frac{R_3}{R_2} V_2\right) + \cdots + \left(-\frac{R_3}{R_N} V_N\right)$$

only negative coef.

weights (a_{11} v_1, a_{12} v_2, a_{1N} v_N)

All weights are negative: How can we make a_1 and a_2 positive?



$$V_{out_1}\ (V_{in}) = -\frac{R_3}{R_1} V_1 - \frac{R_3}{R_2} \cdot V_2$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$$

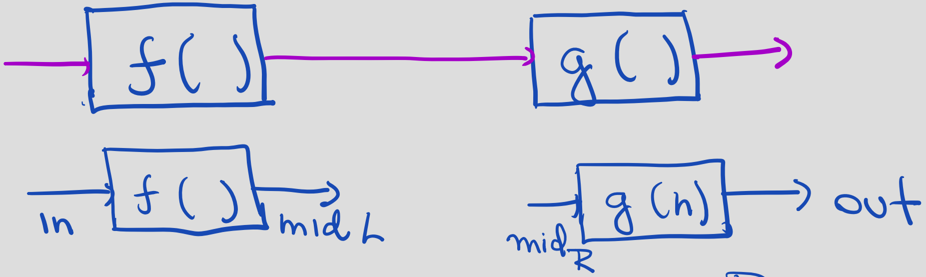
↳ result from inverting amplifier

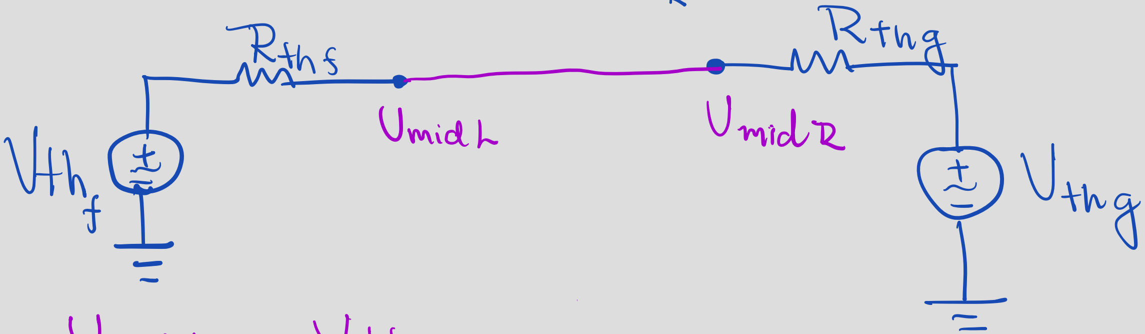
$$V_{out} = -\frac{R_2}{R_1} \cdot V_{in}$$

$V_{out} = -V_{in}$ (when R_1 and R_2 are the same)

Cascading Blocks

We want blocks f( ) and g( ) to keep their functionality.





$V_{midL} = V_{th_f}$

Before connection

After Connection

$$V_{midh} = \frac{R_{Thg}}{R_{thg} + R_{Thf}} \cdot V_{thf} + \frac{R_{thf}}{R_{thf} + R_{thg}} \cdot V_{thg}$$

If $R_{thf} = 0$ or $R_{thg} \to \infty$ is o.c.

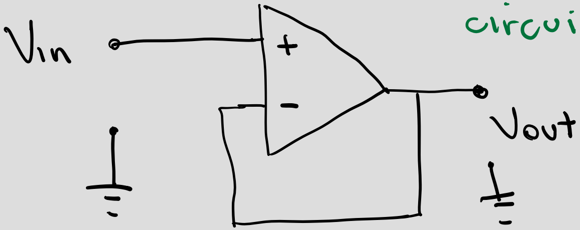
Ideal isolation:

From perspective of block f: see an open circuit;
$R_{Thg} \equiv$ O.C.

From perspective of block g: see a Voltage Source
$R_{Thf} = 0$

Unity Gain Buffer

↳ Allows us to isolate circuits



$U^+ = V_{in}$

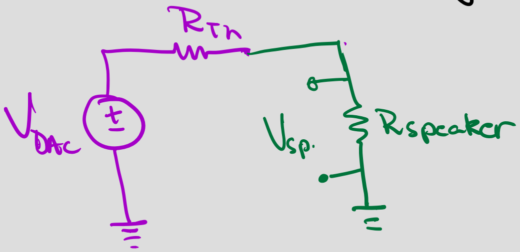
$U^- = V_{out}$

GR2

$U^+ = U^-$

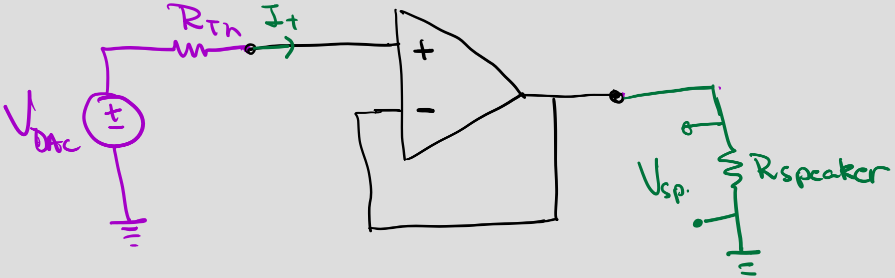
$V_{in} = V_{OUT}$

Speaker Design



$V_{speaker} = \frac{V_{DAC}}{126}$

loading



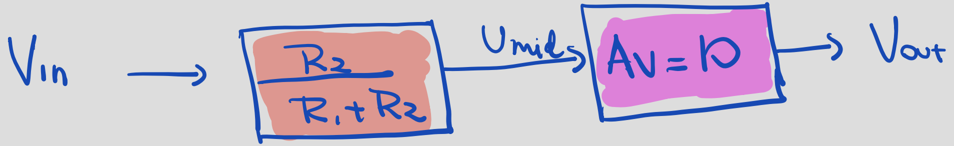
$I^+ = 0 \Rightarrow U^+ = V_{DAC}$

$V_{out} = V_{speaker} = U^- \Rightarrow U^+ = U^-$

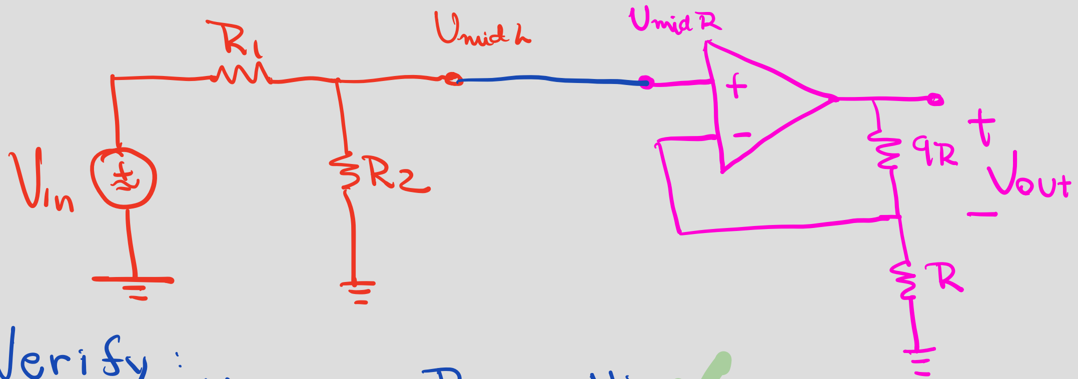
$V_{DAC} = V_{speaker}$

Example 1

Want this:



Implement:



$$V_{out} = V_{in}\left(1 + \frac{R_{Top}}{R_{Bottom}}\right)$$

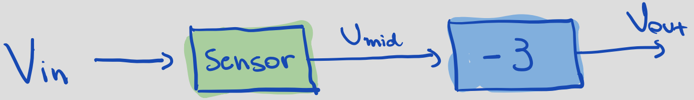
Verify:

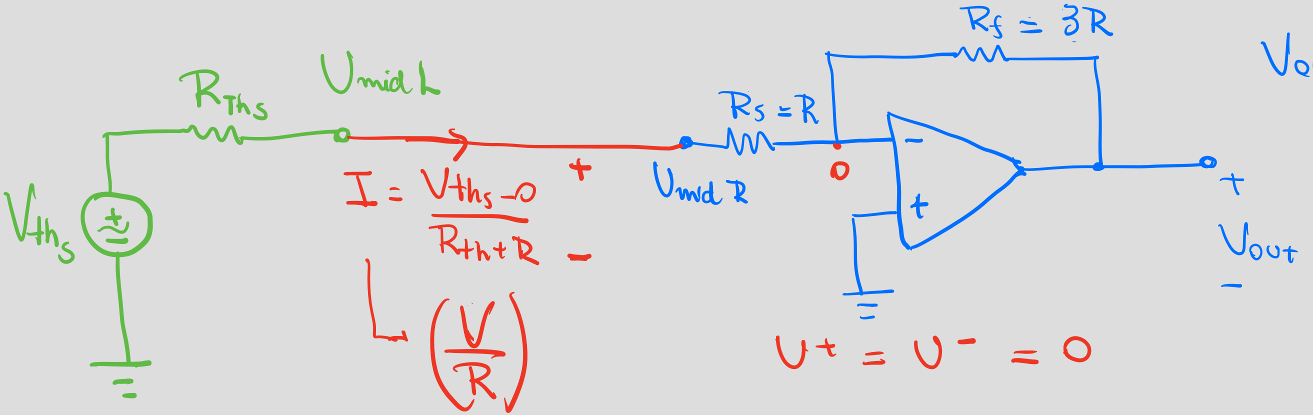
$$V_{mid L} = \frac{R_2}{R_1+R_2} \cdot V_{in} \checkmark$$

$$V_{mid L} = V_{mid R} \Rightarrow A_V = \frac{V_{out}}{V_{mid R}} = 10 \checkmark$$

Example 2

Want this:





$$V_{out} = V_{in}\left(-\frac{R_f}{R_s}\right)$$

Before connection

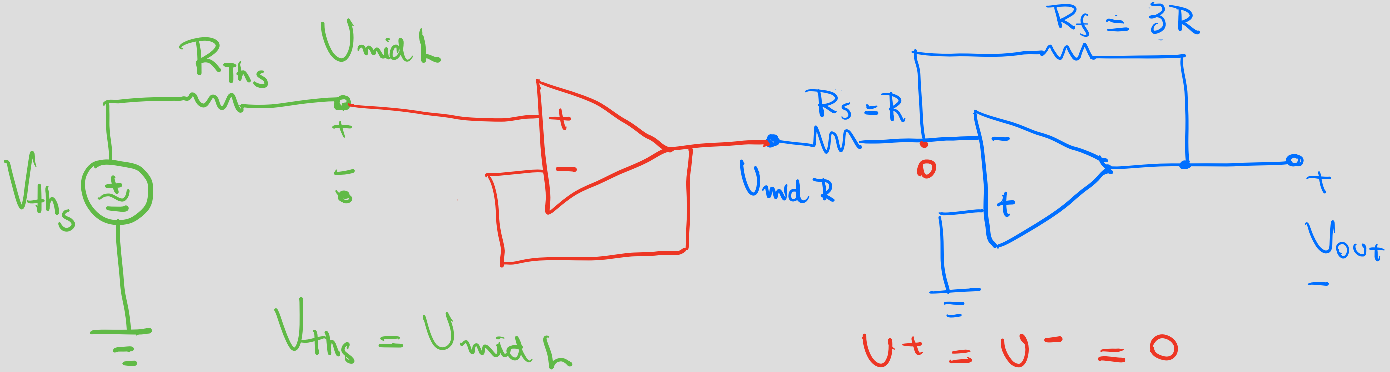
$$U_{mid\,L} = V_{ths}$$

When connected:

$$U_{mid\,L} = \frac{R}{R + R_{ths}} \cdot V_{ths} \neq V_{ths}$$

Solution: ?

Buffer!



$$V_{ths} = U_{mid\,L}$$

$$U^+ = U^- = 0$$

$$\hookrightarrow U_{mid\,L} = U_{mid\,R}$$

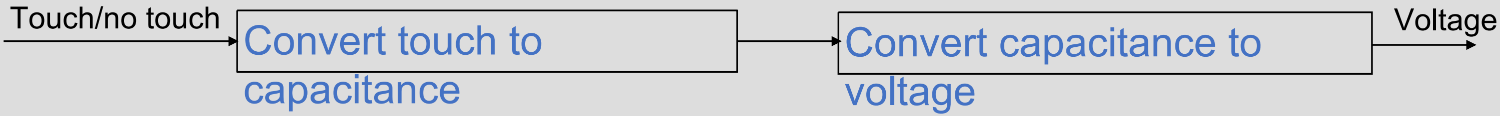
$$\hookrightarrow V_{out} = V_{ths}\left(-\frac{3R}{R}\right)$$

Design Procedure

Step 1 (**Specification**): Concretely restate the goals for the design.

Frequently, a design prompt will include a lot of text, so we'd like to restate all of the most important features of our design. We'll refer to these specifications later to determine if our design is complete.

Step 2 (**Strategy**): Describe your strategy (often in the form of a block diagram) to achieve your goal. To do this, start by thinking about what you can measure vs. what you want to know.



Step 3 (**Implementation**): Implement the components described in your strategy. This is where pattern matching is useful: remind yourself of blocks you know, (ex. voltage divider, inverting amplifier) and check if any of these can be used to implement steps of your strategy.

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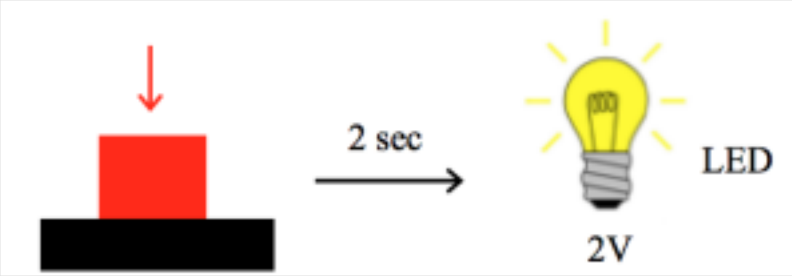
Step 4 (**Verification**): Check that your design from Step 3 does what you specified in Step 1.
Check block-to-block connections, as these are the most common point for problems.
Does one block load another block causing it to behave differently than expected?
Are there any contradictions (ex. a voltage source with both ends connected by a wire, or a current source directed into an open circuit)?

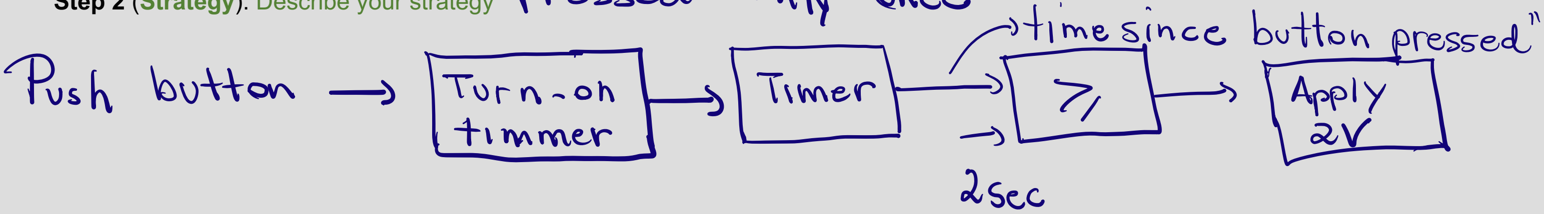
Example 3

Your boss comes to you as asks you to build a countdown timer that will turn on a Light Emitting Diode (LED) two seconds after a button is pressed. She tells you that the LED will emit light when 2V is applied across it.



Step 1 (**Specification**): Build a circuit that measures 2s after a button is pressed; and then applies 2V across a LED. Assume the button is pressed only once

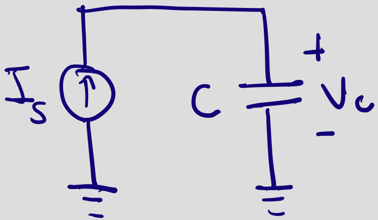
Step 2 (**Strategy**): Describe your strategy



Step 3 (**Implementation**): Implement the components described in your strategy

Turn on circuit :

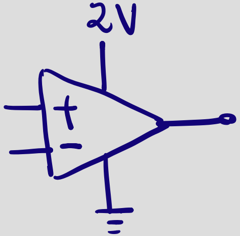
Timer :



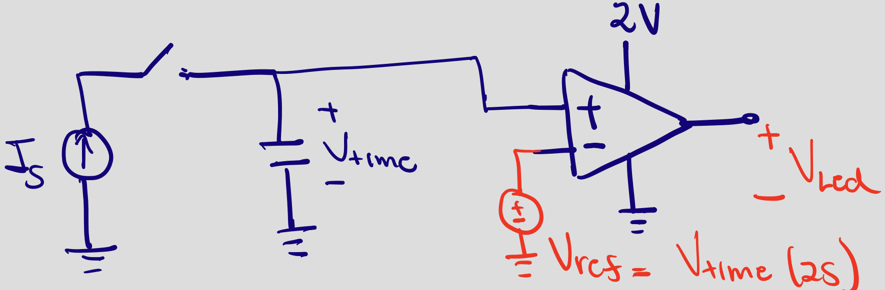
$$I_c = C\frac{dV_c}{dt}$$

$$\underbrace{V_c(t)}_{V_{time}} = \frac{I_s}{C}\cdot t + V_c(0)$$

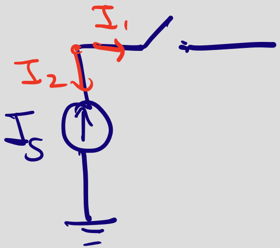
$\geq$:



Together :



Step 4 : Verify :



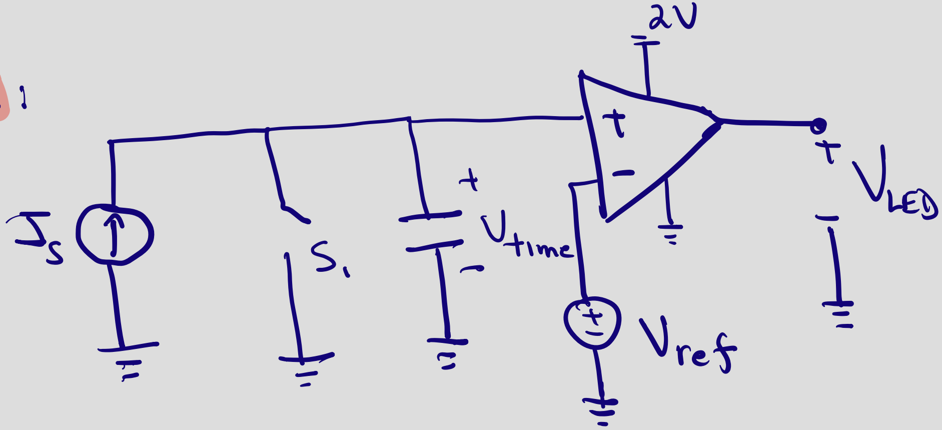
$I_1 = 0$ (o.c. def.)

$I_2 = -I_S$ (elem. def)

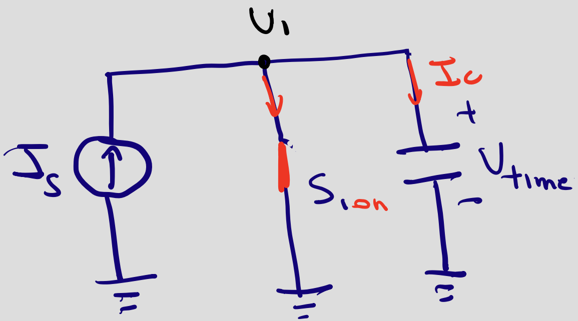
$I_1 + I_2 = 0$ (KCL)

$0 + (-I_S) = 0$ ✗ (violention)

Revise :



Before button is pushed: S_1 is **ON**.



$V_{time} = ?$

$V_1 = 0$ (wire def.)

$V_{time} = V_1 = 0$

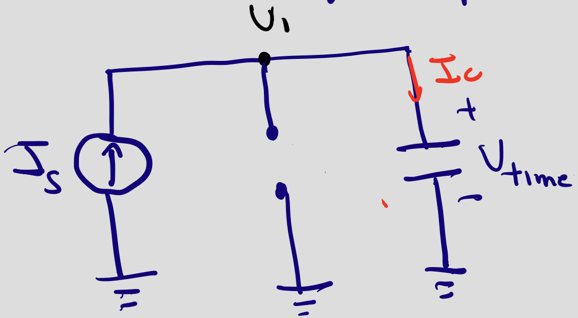
$$I_c = C \frac{dV_{time}}{dt} = 0$$

KCL

$I_s = I_{sw} + I_c$ ($I_c \to 0$)

$I_s = I_{sw}$

When you push the button : S_1 is off



@ $t = t_0$

$$V_{time}(t_0) = 0$$

$$V_{time}(t) = \frac{I_s}{C}(t - t_0) + 0$$

2s

$$V_{time}(t_0 + 2s) = V_{ref}$$