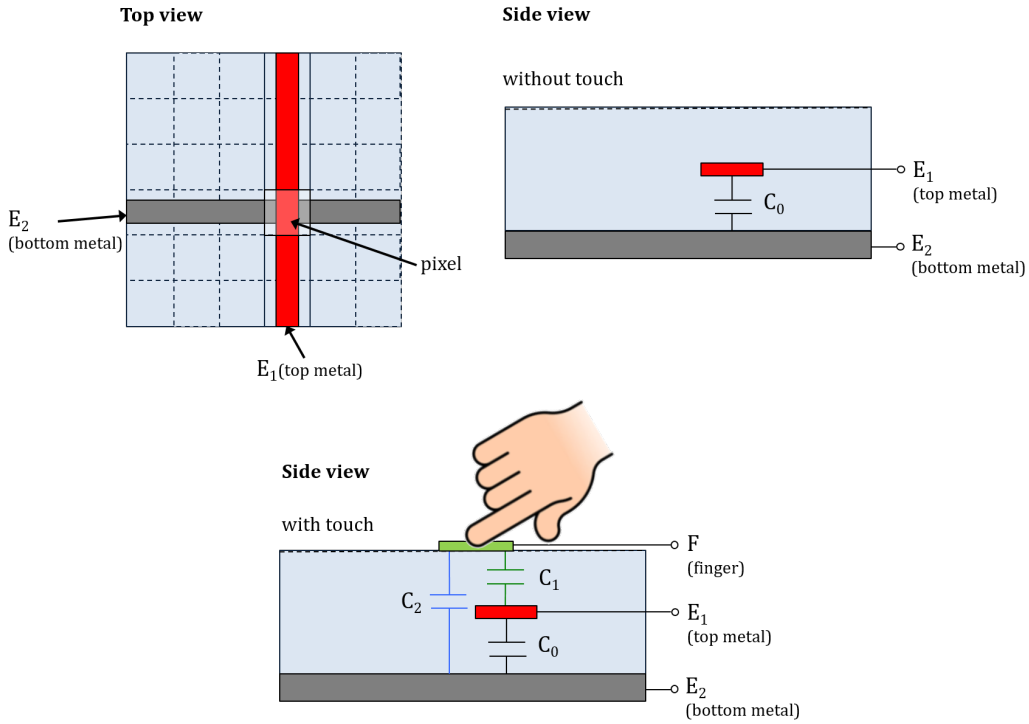
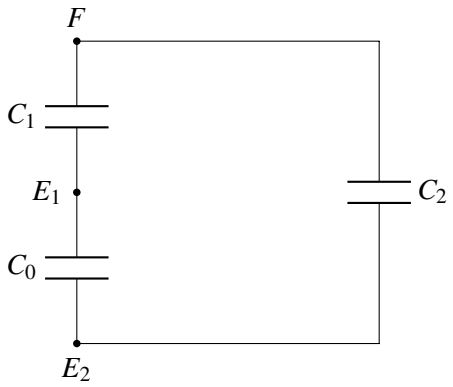
EECS 16A Designing Information Devices and Systems I
Fall 2021 Lecture Notes Note 17

17.1 Capacitive Touchscreen

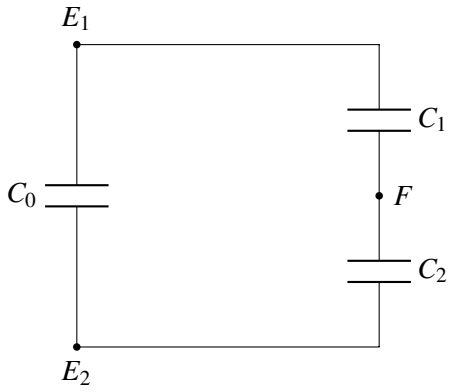
Viewing the physical structure corresponding to one pixel on the capacitive screen, we want to be able to tell if there is a finger touch on top of the pixel.



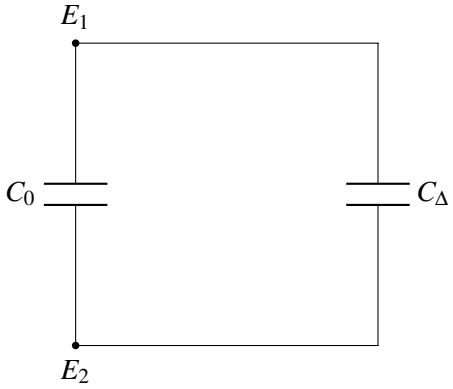
Our finger touches the dielectric at the top, C_2 is the capacitance between our finger (F) and electrode E_2, and C_1 is the capacitance between our finger (F) and electrode E_1. Now, we can draw the equivalent circuit model corresponding to the pixel we're looking at:



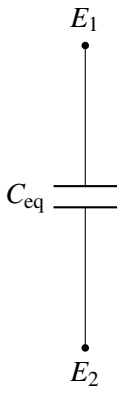
A smart phone can only sense something that is between electrodes E_1 and E_2 as it is impractical to physically connect a measuring device to our finger. So, we redraw our circuit as follows:



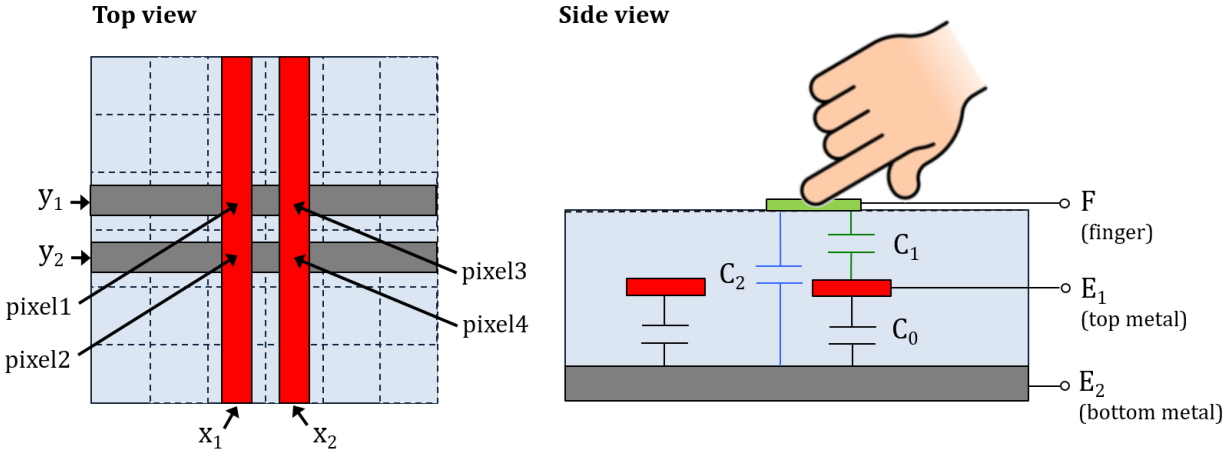
Since we care about the circuit behavior at nodes E_1 and E_2, we can further simplify the circuit by replacing the series combination of C_1 and C_2 with some capacitance $C_\Delta = \frac{C_1 C_2}{C_1 + C_2}$.



If we consider the parallel combination of C_0 and C_Δ as some equivalent capacitance C_{eq}, we know that C_{eq} will have some value greater than C_0 because $C_{\text{eq}} = C_0 + C_\Delta$ and $C_\Delta > 0$.



When a finger presses on top of a pixel, the equivalent capacitance between E_1 and E_2 will become greater than the default capacitance without a finger pressing on top. This characteristic allows us to tell if there is a finger pressing on top of each pixel on our 2D capacitive touchscreen.



Given 4 pixels and their corresponding locations, we can measure the capacitance at (x_1, y_1) to know if there is a finger pressing on top of pixel 1. Similarly, to know if there is a finger pressing on top of pixels 2, 3, 4, we can measure the capacitances at (x_1, y_2), (x_2, y_1), (x_2, y_2). If we sense an increase in the capacitance at the pixel location, we know there is a finger pressing on top of this pixel.

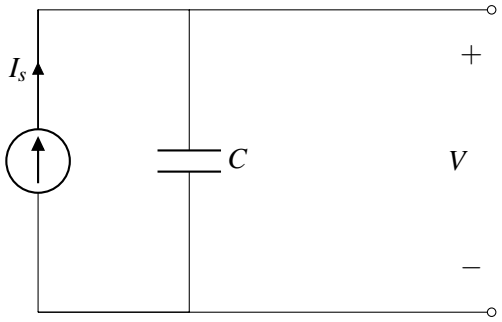
17.2 Capacitance Measurement

To detect a finger touch, we need to be able to measure capacitance. There are various ways you can use to measure capacitance. In this lecture, we will cover one specific method to measure capacitance. First, let's review some basic physics for a capacitor. As you know:

$$I = C \times \frac{dV}{dt}, \tag{1}$$

$$Q = C \times V. \tag{2}$$

We can build a circuit with a current source I_s and a capacitor C. If we charge the capacitor C using the current source I_s for a time interval t,

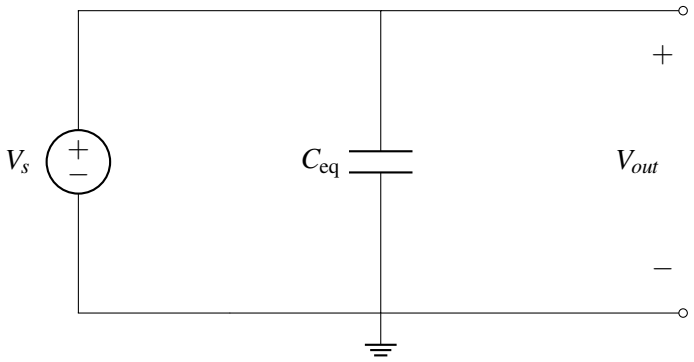


we can then find V to be:

$$V = \frac{I_s \times t}{C}. \tag{3}$$

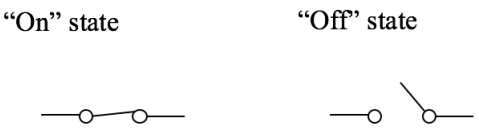
V measured depends on the amount of charge $Q = I_s \times t$ and the capacitance value C. So, if we charge a capacitor using some current source for a finite time period, we can map the voltage across the capacitor to capacitance. However, building a current source is not that easy, so we have to come up with some workarounds to measure capacitance.

- **Attempt #1** Our first attempt is connecting the capacitor to a voltage source and measuring the voltage across the capacitor directly:

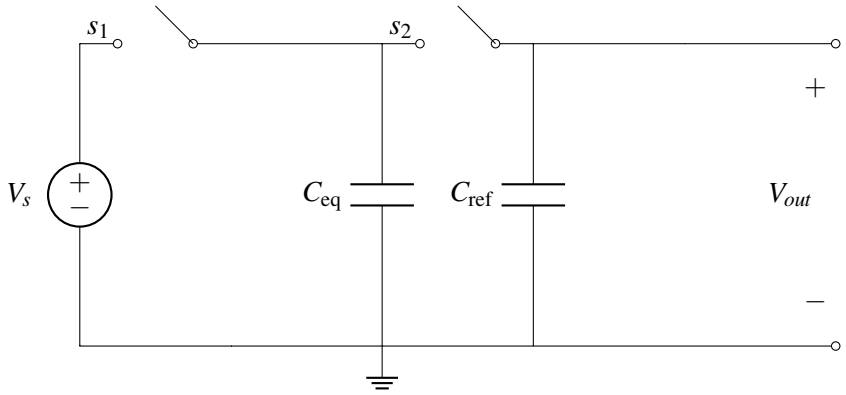


  We can immediately see that no matter how C_{eq} changes, the voltage measured V_{out} is always going to be equal to V_s.

- **Attempt #2** The issue in our first attempt is that after we charge C_{eq} by the voltage source, the voltage across C_{eq} will stay at V_s. In order to use the voltage source as the power source in our circuit, we must disconnect V_s from C_{eq} after charging it, and then somehow discharge C_{eq} so the voltage across it, V_{out}, is different from V_s and the difference must depend on the value of C_{eq}.
  How to disconnect V_s from C_{eq}? We can add switches to the circuit. A switch has two states, at its on state, the switch is closed and becomes a perfectly conducting wire with zero resistance, and when the switch is turned off, it becomes an open circuit.

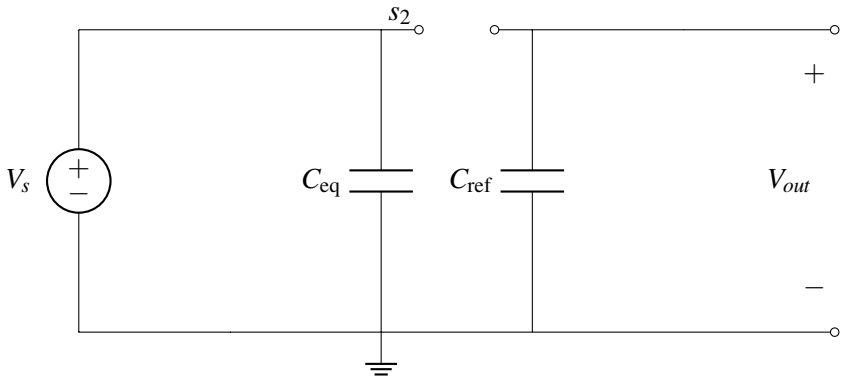


To discharge C_{eq}, we will connect it to a reference capacitor C_{ref} in parallel so some of the charge on C_{eq} is transferred to C_{ref}, and we will measure the voltage V_{out} across them.



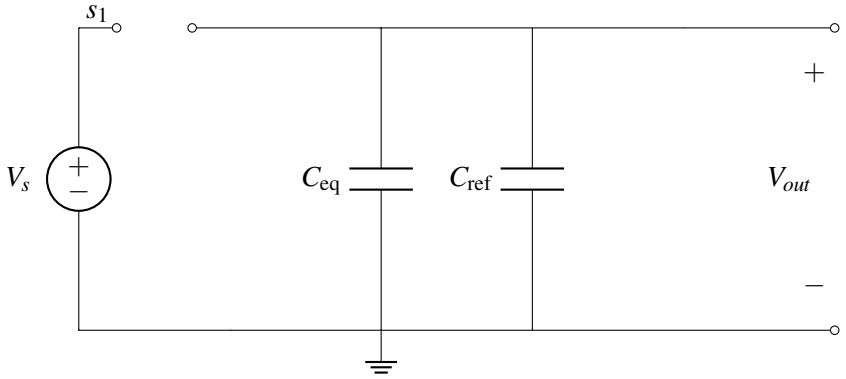
There are two cases (phases) of this circuit.

- **Phase 1:** s_1 is closed and s_2 is open.



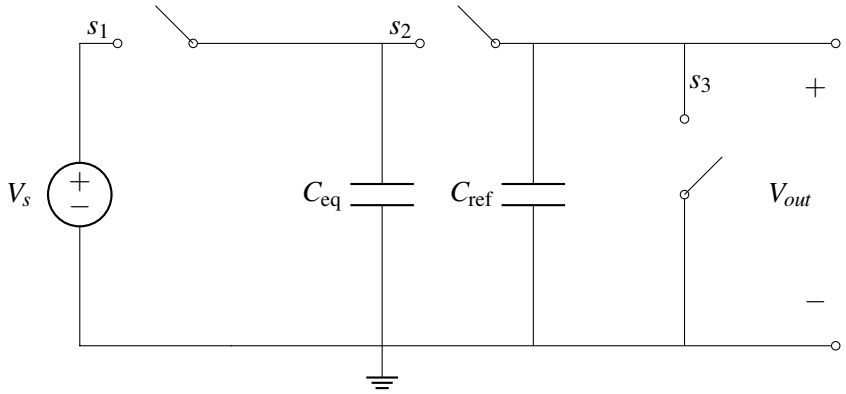
  In phase 1, C_{eq} is connected to voltage source V_s and C_{ref} is not connected to anything.

- **Phase 2:** s_1 is open and s_2 is closed.

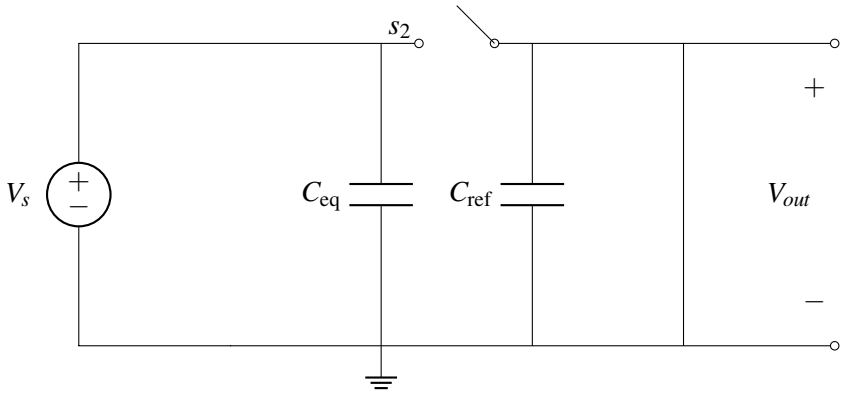


  In phase 2, C_{eq} is disconnected from V_s and C_{ref} is connected to C_{eq}. However, there is one serious problem with this circuit, since we are not sure what is the initial charge of C_{ref}, we cannot perform any circuit analysis. Our second attempt fails because the initial condition of C_{ref} is not clear.

- **Attempt #3** We learned from our second attempt that we must somehow know the initial condition of C_{ref}. How do we know the initial condition of C_{ref}? It turns out that we can acquire this missing piece of information by adding another switch s_3!

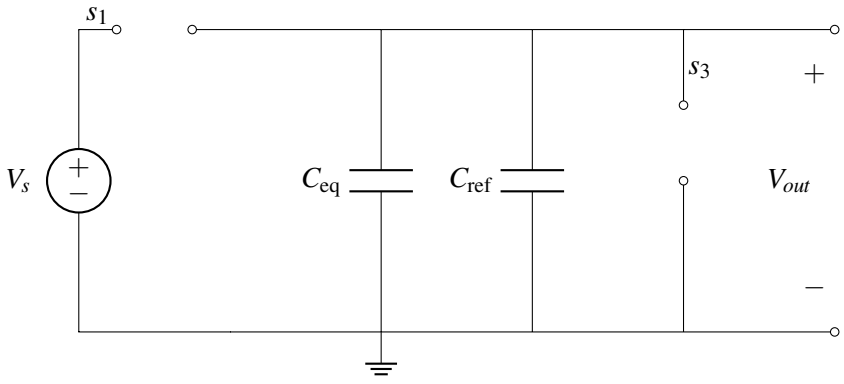


  - **Phase 1:** s_1 is closed, s_2 is open, s_3 is closed.



    In this phase, the voltage across C_{eq} is V_s, and the voltage across C_{ref} is zero.

  - **Phase 2:** s_1 is open, s_2 is closed, s_3 is open.



    In this phase, the voltage across C_{eq} is the same as the voltage across C_{ref}.

17.3 Circuit Analysis with Charge Sharing

How do we analyze this circuit? We know that the total charge of the two capacitors must be preserved between phase 1 and phase 2, this indicates that:

$$Q_{\text{phase 1}} = Q_{\text{phase 2}}. \tag{4}$$

The total charge in each phase can be calculated by summing up Q_{eq} and Q_{ref} for each phase.

$$Q_{\text{phase 1}} = Q_{\text{eq}} + Q_{\text{ref}} = C_{\text{eq}} \times V_s + C_{\text{ref}} \times 0\text{V}. \tag{5}$$

$$Q_{\text{phase 2}} = Q_{\text{eq}} + Q_{\text{ref}} = C_{\text{eq}} \times V_{out} + C_{\text{ref}} \times V_{out}. \tag{6}$$

From equations (**??**) and (**??**) , we have:

$$C_{\text{eq}} \times V_s + C_{\text{ref}} \times 0\text{V} = C_{\text{eq}} \times V_{out} + C_{\text{ref}} \times V_{out}. \tag{7}$$

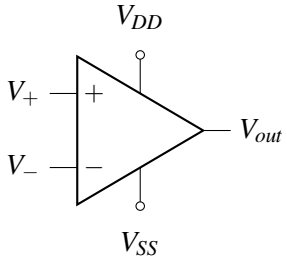
Therefore, we can derive the following equation for V_{out}:

$$V_{out} = \frac{C_{\text{eq}}}{C_{\text{eq}} + C_{\text{ref}}} \times V_s. \tag{8}$$

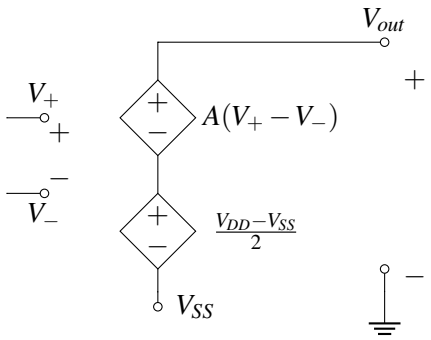
This particular circuit analysis approach we have used is called "charge sharing". Charge sharing refers to the sharing of charge among capacitors. We can use the charge sharing approach to solve many capacitor problems.
Now we can solve for C_{eq} given V_{out}. Recall that we only want to figure out whether or not our finger is touching this pixel, i.e. is C_{eq} greater than its default value when there is no finger touch?

17.4 Comparator & Op-amp Basics

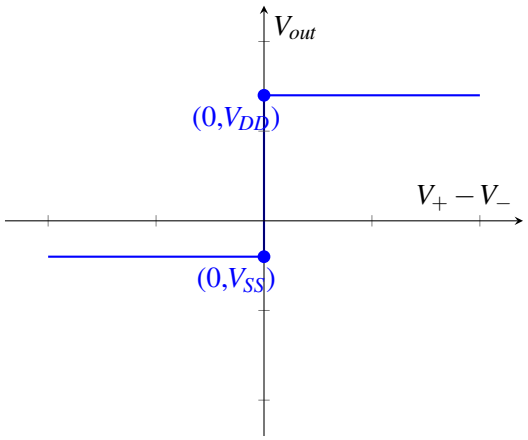
We want to figure out if there is a finger pressing on top of a pixel from V_{out}. In order to do so, we can use a comparator. Before explaining how a comparator works, we will first introduce the concept of op-amp.
Op-amp (operational amplifier), by definition, is an amplifier that can amplify something small into something much bigger. For example, a speaker is an audio amplifier, if you connect your smart phone to a speaker, it can generate sounds much louder than your phone can. The circuit symbol for an op-amp is:



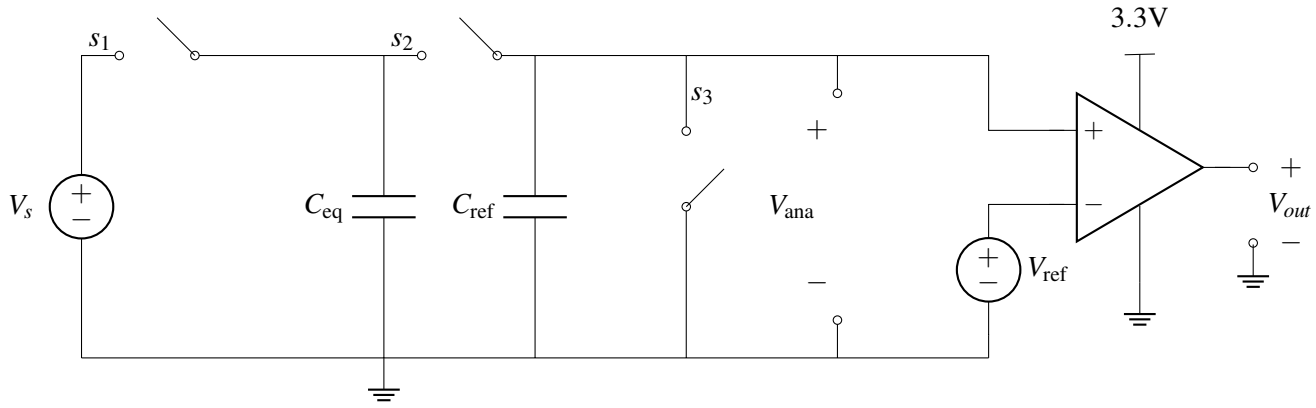
We have two input terminals named V_+ and V_-, two power supply terminals named V_{DD} and V_{SS}, and one output terminal named V_{out}. The op-amp circuit can transform a voltage signal $(V_+ - V_-)$ into V_{out}. For the op-amp to function correctly, we need to connect the two external voltage sources V_{DD}, V_{SS} to the op-amp (typically $V_{DD} > 0$ and $V_{SS} \leq 0$). The symbol actually represents the following equivalent circuit:



In the circuit we see a new symbol — a diamond with +/- signs inside. This represents a voltage-controlled voltage source where the voltage across it depends on the voltage(s) in other parts of the circuit. (An introduction to dependent sources can be found in Note 15 Section 15.2.) In this case, the voltage across the top voltage-controlled voltage source is $A\,(V_+ - V_-)$ where A is a constant. For good op-amps, the constant A term is very large – approaching infinity, but the output voltage cannot go to infinity and is limited by the two external voltage supplies ($V_{SS} \leq V_{out} \leq V_{DD}$). The bottom voltage-controlled voltage source is dependent on the power supplies of the op-amp. If V_+ and V_- are exactly equal, V_{out} is the average of the supply voltages V_{DD} and V_{SS}. Note that the dependent voltage sources are referenced to V_{SS}, not ground.
Equivalently, we have the following plot that describes the relationship between V_{out} and $(V_+ - V_-)$.



For any ideal op-amp, when $V_+ < V_-$ ($V_+ - V_- < 0$), we have V_{out} equals V_{SS}; when $V_+ - V_- > 0$, we have V_{out} equals V_{DD}. If we zoom in around $V_+ - V_- = 0$ by a million times, we will be able to see there is actually some finite slope associated with the transition region.
Now, we add an op-amp to the circuit model we built to extract C_{eq}.



Since the two input voltages to the op-amp are the output of the circuit V_{ana}, and our threshold voltage V_{ref}, if the voltage V_{ana} is greater than V_{ref}, the output voltage V_{out} will be 3.3 V. If $V_{\text{ana}} < V_{\text{ref}}$, V_{out} will be 0V. Recall for V_{ana}, we have

$$V_{\text{ana}} = \frac{C_{\text{eq}}}{C_{\text{eq}} + C_{\text{ref}}} \times V_s. \tag{9}$$

When there is touching, $C_{\text{eq}} = C_0 + C_\Delta$ in which $C_\Delta > 0$, we have:

$$V_{\text{ana, touch}} = \frac{C_0 + C_\Delta}{C_0 + C_\Delta + C_{\text{ref}}} \times V_s \tag{10}$$

When there is no touching:

$$V_{\text{ana, no-touch}} = \frac{C_0}{C_0 + C_{\text{ref}}} \times V_s \tag{11}$$

For any finite capacitance $C_\Delta > 0$, $V_{\text{ana, touch}}$ is always greater than $V_{\text{ana, no-touch}}$.
V_{ana} is connected to the positive voltage input (V_+) of the op-amp, V_{ref} is connected to the negative voltage input (V_-) of the op-amp. If we set up V_{ref} such that:
(1) $V_{\text{ana, touch}} > V_{ref}$, i.e. $V_+ - V_- > 0$, V_{out} will be equal to 3.3 V when there is touching.
(2) $V_{\text{ana, no-touch}} < V_{ref}$, i.e. $V_+ - V_- < 0$, V_{out} will be equal to 0 V when there is no touching.
Now we have built a **comparator** circuit that can compare V_{ana} against V_{ref} using an op-amp!
How should we set up the threshold voltage V_{ref}? Intuitively, we want to set it to be halfway between $V_{\text{ana, no-touch}}$ and $V_{\text{ana, touch}}$. This actually allows our comparator circuit to be robust against non-idealities, we will have the same amount of margin for any V_{ana} that deviates from its ideal values, either from $V_{\text{ana, touch}}$ or from $V_{\text{ana, no-touch}}$.
A second important question is **how should we set up C_{ref}?** Recall that $V_{ana} = \frac{C_{\text{eq}}}{C_{\text{eq}}+C_{\text{ref}}} \times V_s$. We realize that V_{ana} is associated with C_{ref}. As long as we do not set C_{ref} to some value much greater (for example, 1000 times greater) than C_{eq} so that V_{ana} becomes too small (for our op-amp to pick up the signal), we can get some reasonable V_{ana}, which then allows us to set up V_{ref} according to $V_{\text{ana, touch}}$ and $V_{\text{ana, no-touch}}$.
Practically, we will set up one of C_{ref}, V_{ref} first, and then set up the other value according to $V_{\text{ref}} = \frac{1}{2}(V_{\text{ana, touch}} + V_{\text{ana, no-touch}})$.

17.5 Comparators in Practice

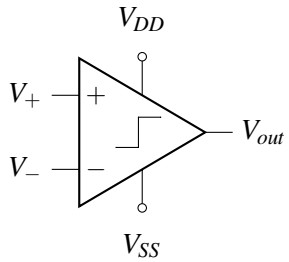
In the previous section, we used an ideal op-amp to function as a comparator for our capacitive touchscreen design. Even though for ideal op-amps which have infinite open loop gain, A, this is okay to do, in practice

circuit designers rarely use op-amps as comparators. Since op-amps are optimized for linear signal amplification with output voltages always staying between the supply rails (V_{DD}, V_{SS}), and for stability, they tend to be very slow when having to resolve a small input difference into a large digital output (V_{DD} or V_{SS}).

Dedicated comparators, by contrast, are special, distinct components designed to output only the supply voltages, (V_{DD} or V_{SS}), and are preferred to op-amps for their faster operation. The plot of input and output voltages for a comparator is identical to that of an ideal op-amp in the comparator configuration, shown in the previous section.

For any ideal comparator, (just like for any ideal op-amp), when $V_+ - V_- < 0$, we have V_{out} equals V_{SS}; when $V_+ - V_- > 0$, we have V_{out} equals V_{DD}.

The circuit symbol for a comparator is shown below:



In summary, in the context of this class we will say that *ideal* op-amps can operate as *ideal* comparators. Keep in mind though, that the actual circuit design and implementation of these two circuit blocks (more of which you can see in classes like EE 105, EE140 and EECS151) are fundamentally different.