EECS 16A Designing Information Devices and Systems I
Summer 2020 Midterm 2 Instructions

Read the following instructions before the exam.

Format & How to Submit Answers

There are 12 problems (4 introductory questions, and 8 exam questions, comprising 42 subparts total) of varying numbers of points. The problems are of varying difficulty, so pace yourself accordingly and avoid spending too much time on any one question until you have gotten all of the other points you can. Don't get bogged down in calculations; if you are having trouble with one problem, there may be easier points available later in the exam!

All answers will be submitted to the Gradescope "Midterm 2" Assignment (`https://www.gradescope.com/courses/137582/assignments/576104`). All questions, except introductory questions, are multiple choice and are **worth 3 or 4 points each**. **There are 150 points possible on the exam, but your final score will be taken out of 140 points**. This means that a score of 100/150, normally 67%, will be bumped up to 100/140, or 71%. You cannot score more than 100% on this exam.

Partial credit may be given for certain incorrect answer choices for some problems. There is no penalty for incorrect answers.

Post any content or clarifying questions privately on Piazza. There will be no exam clarifications; if we find a bug on the exam, that sub-question will be omitted from grading.

Timing & Penalties

You have 120 minutes for the exam, with a 5 minute grace period. After the 5 minute grace period ends, exam scores will be penalized exponentially as follows: an exam that is submitted N minutes after the end of the grace period will lose 2^N points. **The exam will become available at your personalized link at 7:10 pm PT; the grace period will expire at 9:15 pm PT.** If your submission is timestamped at 9:16 pm PT, you will lose 2 points; if it is timestamped at 9:18 pm PT, you will lose 8 points.

We will count the latest time at which you submit any question as your exam timestamp. Do NOT edit or resubmit your answers after the deadline. We recommend having all of your answers input and submitted by 9:10 pm; it is your responsibility to submit the exam on time.

If you cannot access your exam at your link by 7:15 pm, please email eecs16a@berkeley.edu. If you are having technical difficulties submitting your exam, you can email your answers (either typed or scanned) to eecs16a@berkeley.edu.

Academic Honesty

This is an open-note, open-book, open-internet, and **closed-neighbor** exam. You may use any calculator or calculation software that you wish, including Wolfram-Alpha and Mathematica. **No collaboration is allowed, and do not attempt to cheat in any way. Cheating will not be tolerated.**

We have zero tolerance against violation of the Berkeley Honor Code. Given supporting evidence of cheating, we reserve the right to automatically fail all students involved and report the instance to the student conduct committee. We reserve the right to **audit students with oral exams** after the midterm to ensure academic honesty. Feel free to report suspicious activity through this form. (`https://forms.gle/ZzXLksZEmx9bn1mj7`).

Our advice to you: if you can't solve a particular problem, move on to another, or state and solve a simpler one that captures at least some of its essence. You will perhaps find yourself on a path to the solution.

Good luck!

EECS 16A Designing Information Devices and Systems I
Summer 2020 Midterm 2

1. **Pledge of Academic Integrity (2 points)**
   By my honor, I affirm that:

   (1) this document, which I will produce for the evaluation of my performance, will reflect my original, bona fide work;

   (2) as a member of the UC Berkeley community, I have acted and will act with honesty, integrity, and respect for others;

   (3) I have not violated—nor aided or abetted anyone else to violate—nor will I—the instructions for this exam given by the course staff, including, but not limited to, those on the cover page of this document; and

   (4) I have not committed, nor will I commit, any act that violates—nor aided or abetted anyone else to violate—the UC Berkeley Code of Student Conduct.

   Write your name and the current date as an acknowledgement of the above. (See Gradescope)

2. **Administrivia (2 points)**
   I know that I will lose 2^n points for every n minutes I submit after the exam submission grace period is over.

   For example, if the exam becomes available at my personalized link at 7:10 p.m. PT; the grace period will expire at 9:15 p.m. PT. If my submission is timestamped at 9:16 p.m. PT, I will lose 2 points; if it is timestamped at 9:18 p.m. PT, I will lose 8 points.

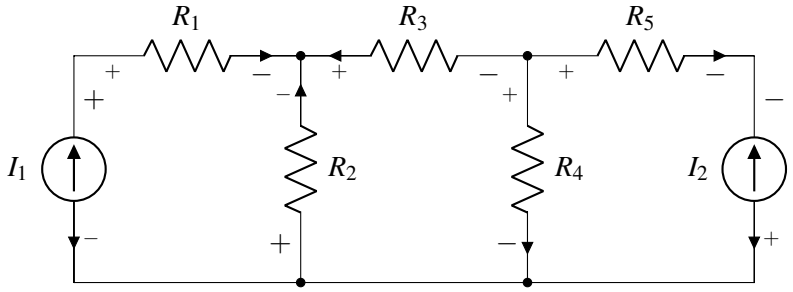
   - ○ Yes

3. **What do you enjoy most about EECS16A? (2 points)**

4. **Tell us about something that makes you happy. (2 points)**

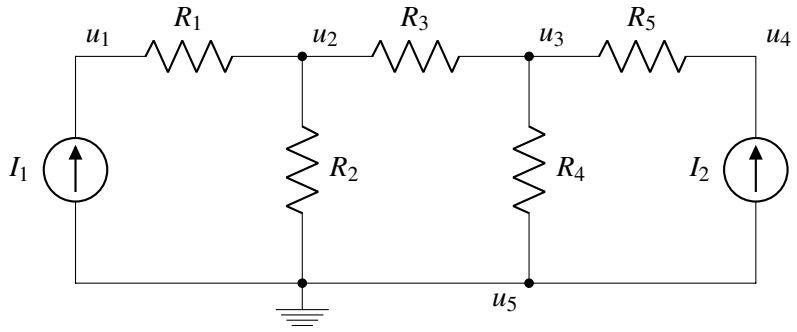
5. Circuit Analysis (12 points)

(a) (4 points) Which components have been labeled according to passive sign convention? Select all that apply.

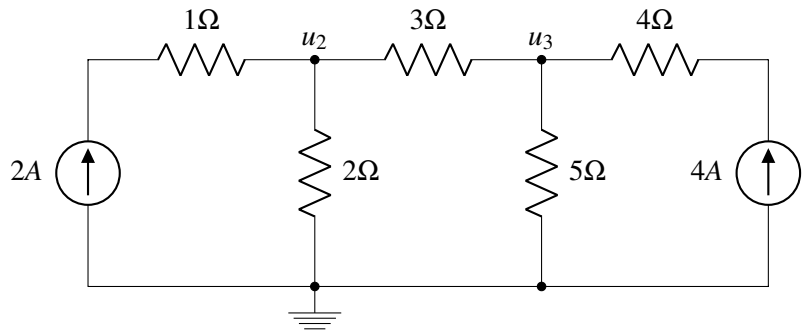


(1) I_1
(2) R_2
(3) R_1
(4) I_2
(5) R_4
(6) R_5
(7) R_3

(b) (4 points) Find the correct KCL expression at the node with node voltage u_3.



(c) (4 points) Given the node voltage $u_3 = 12V$, find u_2.

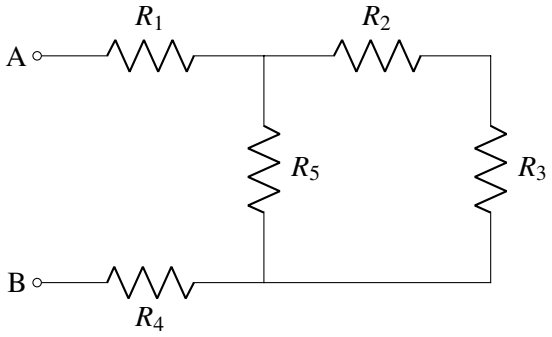


6. Equivalence in Resistive and Capacitive Networks (15 points)

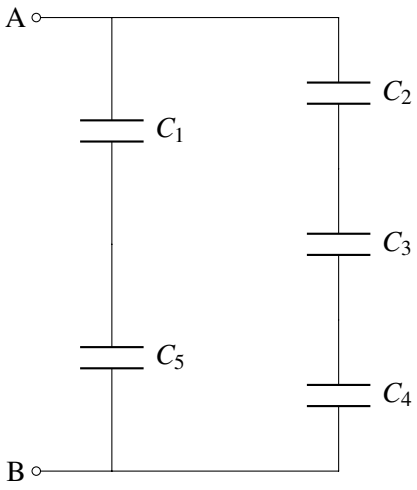
For all of the following networks find an expression or a numerical value for the equivalent resistance or capacitance between terminals A and B.

Hint: You can use the equivalence formulas for series and parallel combinations of resistors and capacitors for all of the subparts in this question.

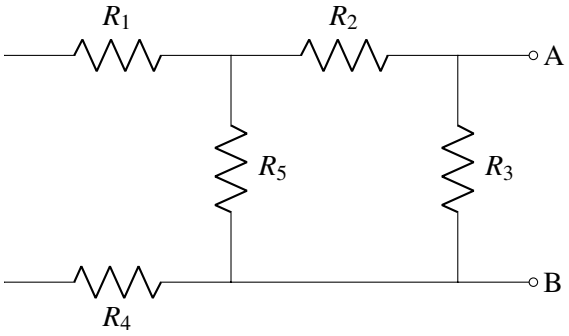
(a) (3 points)



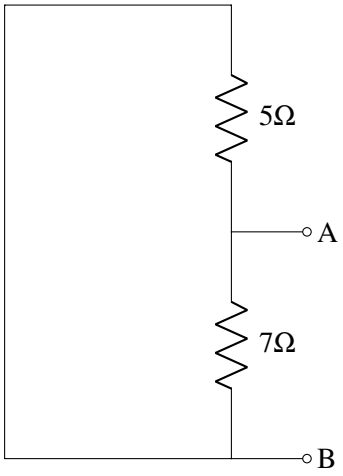
(b) (3 points)



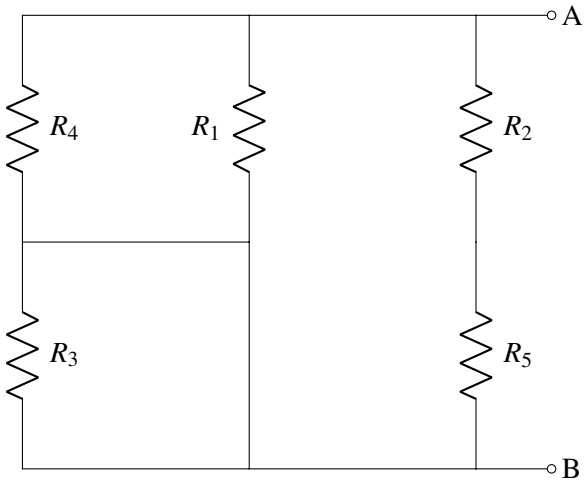
(c) (3 points)



(d) (3 points)

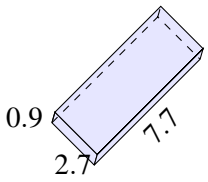


(e) (3 points)



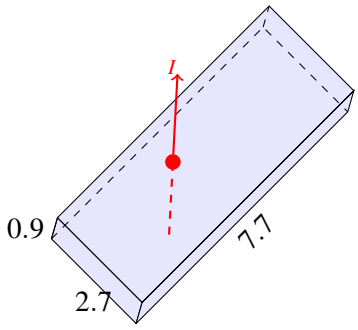
7. Resist the Power! (23 Points)

(a) (4 points) You are given a resistive slab with resistivity $5.7\Omega \cdot \text{cm}$ and dimensions 0.9cm, 2.7cm, and 7.7cm as denoted on the figure below. The dimensions and the resistivity of the slab remain the same throughout the rest of the problem.

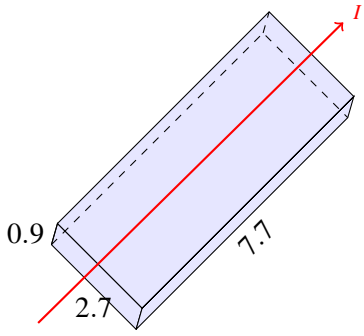


Suppose we connect opposite faces of the slab to a voltage source so that current can flow through it. Notice that there are 3 possible configurations we can have for this slab, leading to 3 possible directions in which the current can flow (drawn in the answer choices below). Which direction will lead to the **highest** current flow I assuming we use the same valued voltage source all three times?
Assume the resistivity is the same throughout the slab and does not vary with respect to the direction of current flow.

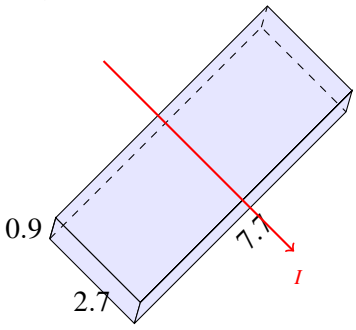
(A) Parallel to 0.9 (current goes through 2.7, 7.7 face):



(B) Parallel to 7.7 (current goes through 0.9, 2.7 face):



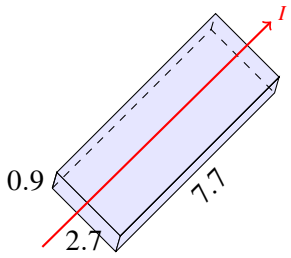
(C) Parallel to 2.7 (current goes through 0.9, 7.7 face):



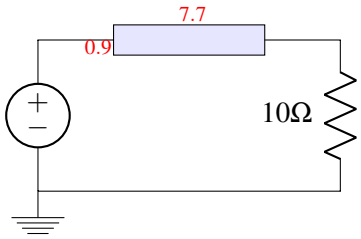
(D) Choices (A) and (C) are tied for the maximum current flow.

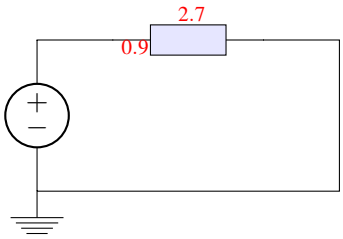
(E) The direction doesn't matter; the resistor is physically the same, so the current will be the same.

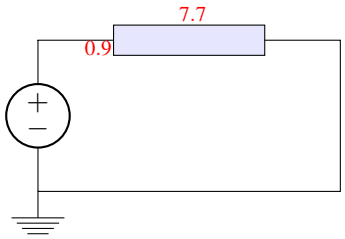
(b) (3 points) We connect the voltage source so that current flows parallel to 7.7 (through the $0.9, 2.7$ face), as shown below. What is the resistance of the slab, R_{slab}?

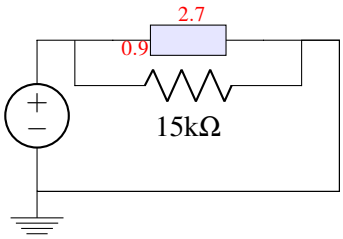


(c) (4 points) You are experimenting with various circuit configurations involving the slab and a voltage source. 2 dimensions are labeled (in red), and the 3rd is the one going "into" the page (not to scale). Which of the following configurations leads to the *minimum* power dissipation by the slab?

(A)


(B)


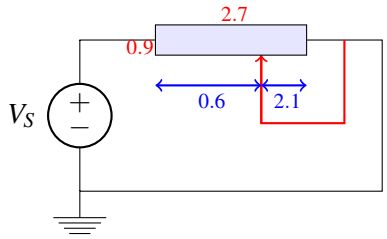
(C)


(D)


(E) More than one of the labeled circuits has the same power dissipated across the slab.

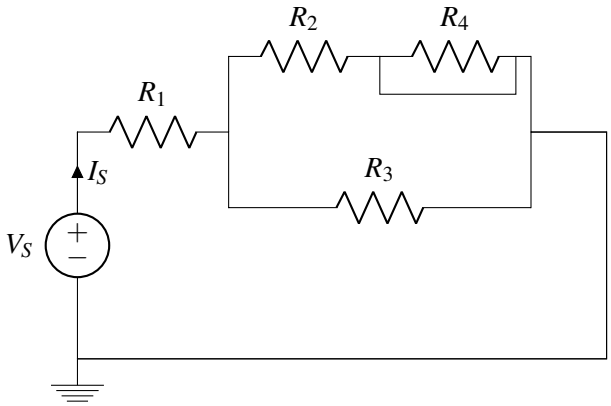
(d) (4 points) Suppose you selected configuration (A) from above, which may or may not be correct. What is the power dissipated by the slab in that configuration?

(e) (4 points) You realize that you can turn the slab into a variable resistor! You attach an ideal metal connector (shown in red) between one end of the resistive slab and some point in the middle of the slab, as shown below.

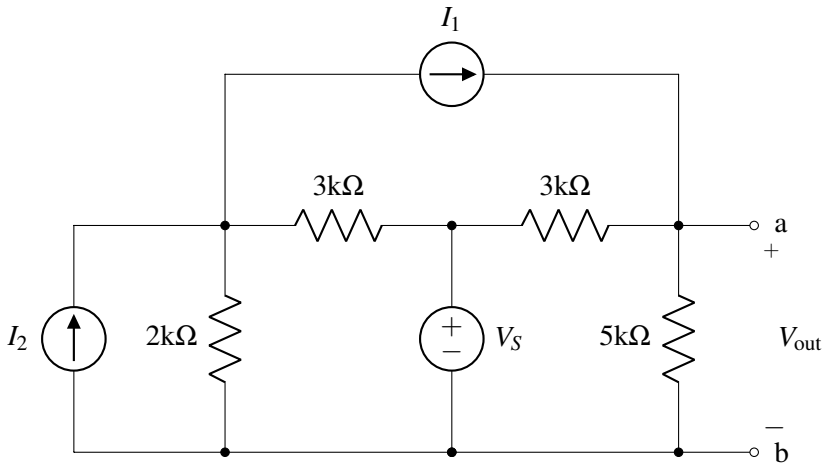


Draw the equivalent circuit diagram for this physical configuration.

(f) (4 points) You construct a new circuit using several resistive slabs, a variable resistor and a voltage source, for which the equivalent circuit diagram is shown below. Which resistor has **no** current passing through it, regardless of it's value? Which resistor has the **most** current passing through it, regardless of its value?
Note: Assume R_1 - R_4 are finite positive value resistors (non-zero and non-infinite).



8. Superimposing Thevenin (16 points)



(a) (4 points) Calculate the Thevenin equivalent resistance between terminals a, b. Round to three decimal places if neccessary.

(b) (4 points) Calculate the output voltage V_{out} when all sources except I_2 are nulled.

(c) (4 points) Calculate the output voltage V_{out} when all sources except I_1 are nulled.

(d) (4 points) Let αI_2 be the correct answer to part (b), and let βI_1 be the correct answer to part (c). Calculate the Thevenin equivalent voltage between the terminals a, b.

9. Misadventures with Measurements (20 points)

You are learning about voltmeters and ammeters in EECS 16A Module 2. A voltmeter is an instrument used to measure the voltage difference between any two nodes in a circuit, while an ammeter measures the current through any circuit element. We can model the voltmeter and the ammeter as resistors: R_{VM} and R_{AM} respectively.

(a) (4 points) Suppose we want to measure the voltage across nodes a and b (V_{ab}) in the circuit on the left in Figure 1. To accomplish this, we connect the voltmeter across nodes a and b, as shown on the right in Figure 1.

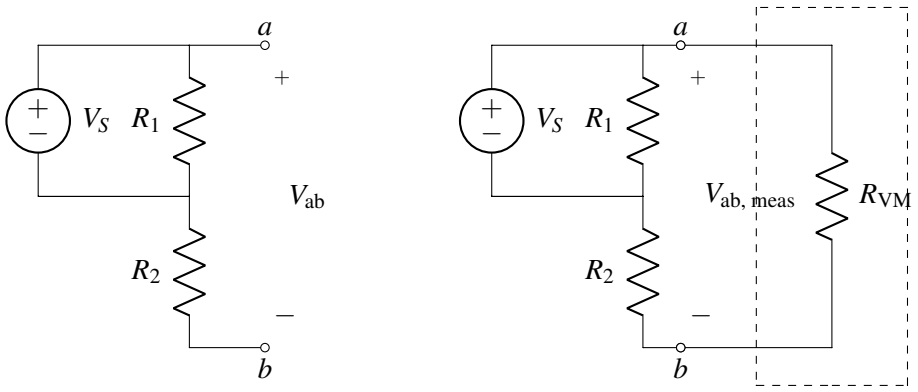


Figure 1: Left: Circuit without the voltmeter connected, Right: Voltmeter measuring $V_{\text{ab, meas}}$

Assuming that $R_{VM} \to \infty$, what is the value of voltage $V_{\text{ab, meas}}$ approximately, in terms of R_1, R_2, R_{VM}, and V_S?

(b) (4 points) For this part, let's assume that $V_S = 5\text{V}$, $R_{VM} = 490\text{k}\Omega$ for Figure 1. (In this case, the voltmeter is non-ideal and R_{VM} is comparable to R_1 and R_2). This non-ideality causes a discrepancy between the voltage V_{ab} before connecting the voltmeter and the measured voltage, $V_{\text{ab, meas}}$. The percentage error is given by

$$\%err = \frac{V_{ab} - V_{\text{ab, meas}}}{V_{ab}} \times 100\% \tag{1}$$

Find all the combinations of R_1 and R_2 that keep the % error below 1%.

(1) $R_1 = 5.0\text{k}\Omega$, $R_2 = 6.1\text{k}\Omega$
(2) $R_1 = 5.0\text{k}\Omega$, $R_2 = 10.1\text{k}\Omega$
(3) $R_1 = 10.1\text{k}\Omega$, $R_2 = 4.9\text{k}\Omega$
(4) $R_1 = 6.1\text{k}\Omega$, $R_2 = 5.0\text{k}\Omega$
(5) $R_1 = 5.0\text{k}\Omega$, $R_2 = 4.9\text{k}\Omega$

(c) (4 points) Now let us modify the previous circuit by short circuiting terminals a and b, as shown on the left of Figure 2. Suppose we want to measure the current through R_2. To do so, we insert an ammeter in series with R_2, as shown on the right in Figure 2.

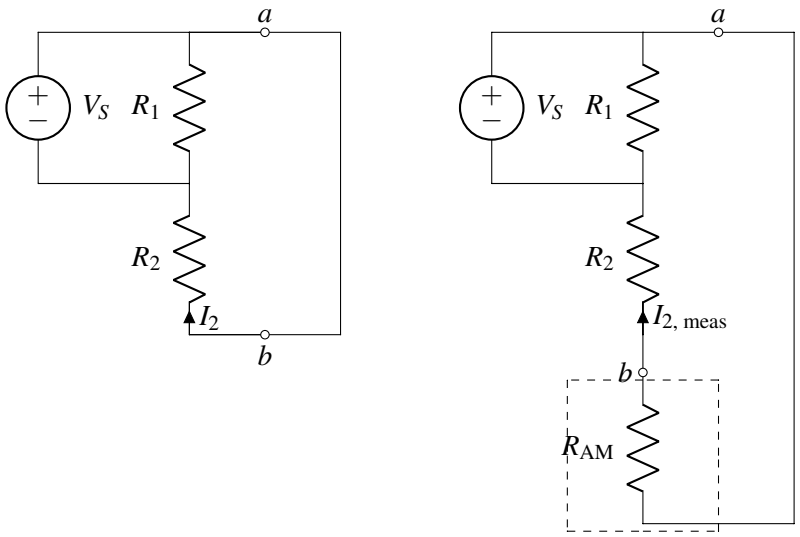


Figure 2: Left: Circuit without the ammeter connected, Right: ammeter measuring I_2

Assuming that $R_{AM} \to 0$, what is the value of the current $I_{2,\text{ meas}}$ approximately, in terms of R_1, R_2, R_{AM}, and V_S?

(d) (4 points) A photoresistor is a special kind of resistor, whose resistance decreases when we shine light on it. We introduce a photoresistor, R_{Ph}, in the circuit from the last part, arriving at the circuit in Figure 3. Depending on the light intensity, R_{Ph} varies between 100Ω and 100kΩ. Here we assume that $V_S = 5\text{V}$, $R_{AM} = 100\Omega$ (non-ideal ammeter).

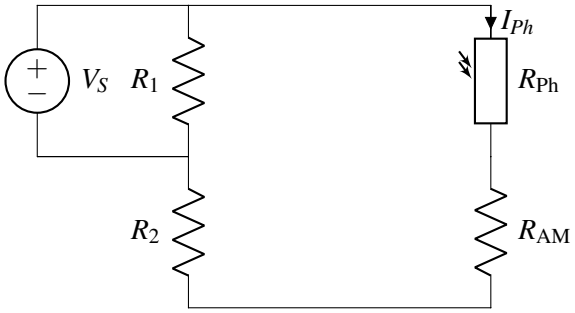


Figure 3: Circuit with ammeter measuring I_{Ph} through the photoresistor

We want the maximum current through R_{Ph} to stay below 1.0mA. Choose value(s) of R_2 to make sure that $I_{Ph} < 1.0\text{mA}$ for the full range of R_{Ph}. Choose all the options that are applicable.

(1) $R_2 = 4750.0\Omega$
(2) $R_2 = 4850.0\Omega$
(3) $R_2 = 4900.0\Omega$
(4) I_{Ph} does not depend on R_2
(5) $R_2 = 4700.0\Omega$
(6) None of these options are correct

(e) (4 points) For this part, let's assume that the voltmeter and ammeter are ideal, i.e. $R_{VM} \to \infty$ and $R_{AM} = 0\Omega$.

Values of V_S, R_1 and R_2 are unknown. Let us revisit the circuits from parts (a) and (c).

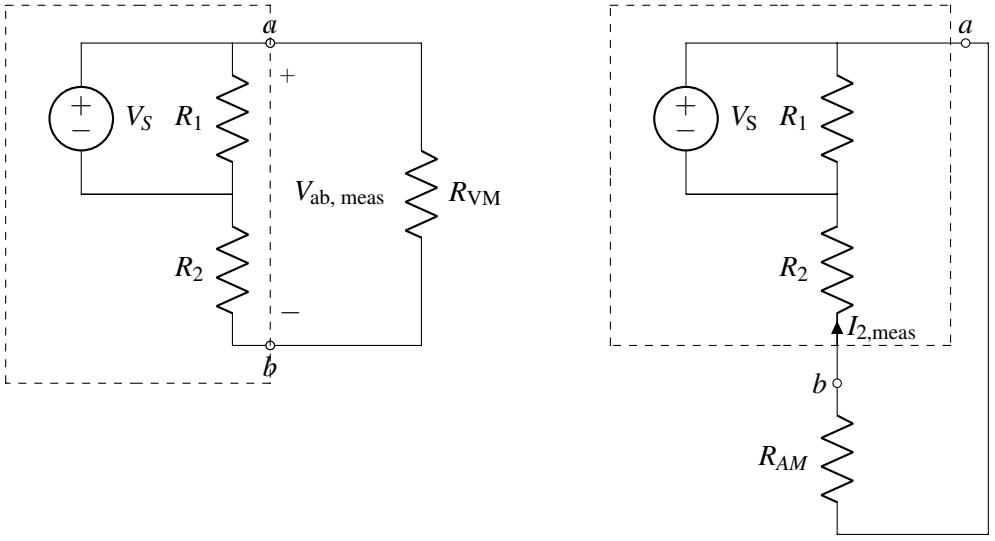
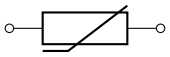


Figure 4: Left: Voltmeter measuring $V_{ab,\,meas}$, Right: ammeter measuring $I_{2,\,meas}$

We measure $V_{ab,\,meas} = 2$V for the circuit on the left in Figure 4, while we measure $I_{2,\,meas} = 1.0$mA for the circuit on the right. Find the Thevenin equivalent of the circuit in the box between terminals a and b, i.e. find V_{TH} and R_{TH}.

10. Thermostat (12 points)

Your house is too cold! You've decided to design a thermostat that will turn on the heater if the temperature is below a certain threshhold, and turn off the heater once the house gets warm enough. In order to implement it, you've decided to use a new component known as a thermistor, which is represented in circuit diagrams with the following symbol:

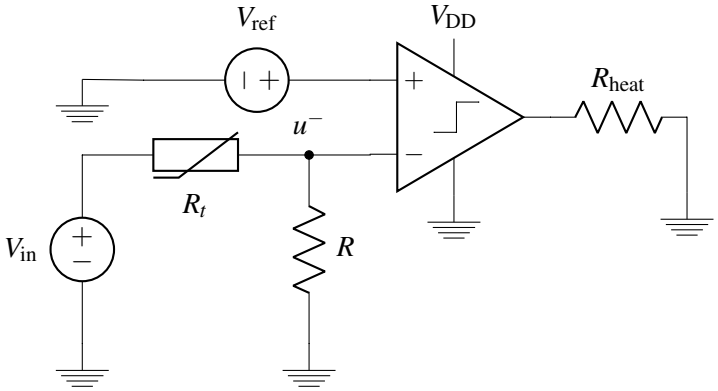


A thermistor is a variable resistor where the resistance changes with the temperature. For this problem we will be using a thermistor where the resistance increases as the temperature decreases, according to the following equation:

$$R_t = R_0 - k(T - T_0) \tag{2}$$

where T is the current temperature, R_0 is the resistance that occurs at the reference temperature T_0, and k is a positive constant representing the sensitivity of the thermistor.

(a) (4 points) In an old 16A textbook, you find the following circuit diagram that you think might be useful:

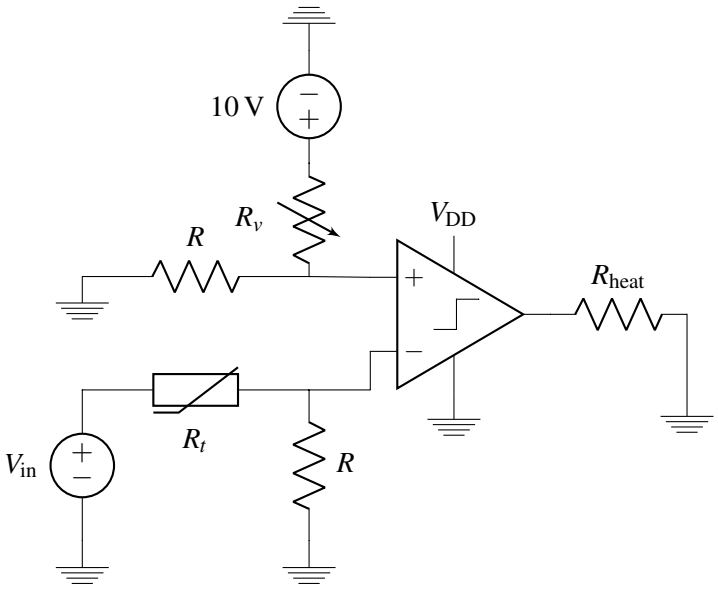


What is the voltage at the negative input of the comparator, u^- ? Write your answer in terms of V_{in}, R, R_0, k, and T_0.

(b) (4 points) The comparator should output V_{DD} when the temperature is less than T_d, the desired temperature, turning the heater on, and it should output ground otherwise, turning the heater off. Based on the part (a) diagram and equation 2, express T_d, the point at which the thermostat switches off the heat, as a function of V_{in}, V_{ref}, V_{DD}, R, R_0, k, and T_0.

(c) (4 points) In order to make it possible to change the setting of the thermostat after the thermistor has been picked, you've added a variable resistor, R_v, to your circuit. It has the following symbol:

The new circuit that you have configured is shown below.



You want to make sure that your thermostat can heat your home up to 85°F, but no more than that. To that end you have picked $V_{in} = 10\,V$, $R = 8\,k\Omega$, $V_{DD} = 100\,V$, $R_{heat} = 5\,\Omega$, and a thermistor with $R_0 = 4\,k\Omega$, $T_0 = 65°F$, and $k = 10\,\Omega/°F$. What is the range of R_v values that achieves this design goal?

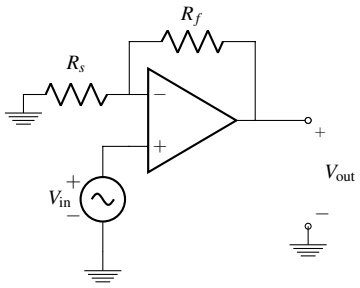
11. Op Amp Drills (26 points)

Congratulations! Fresh off your EECS 16A experience you have been hired as an intern at Linear Circuits, Inc. to design next generation systems. Your first task will be to come up with a circuit that can perform linear operations to received signals of interest. Specifically, you want to build a circuit whose output is a weighted sum of multiple received inputs, i.e. $V_{\text{out}} = \alpha V_{\text{in},1} + \beta V_{\text{in},2} + \gamma V_{\text{in},3} + ...$, with the coefficients $\alpha, \beta, \gamma \in \mathbb{R}$.

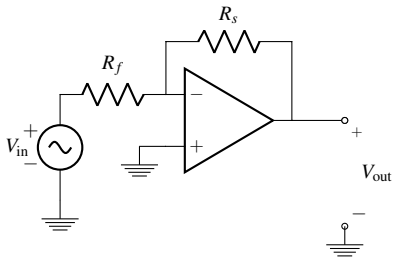
To do so you will be using your favorite circuit element, the op amp! As usual with circuit design, you decide to start simple and then combine your fundamental building blocks to achieve more complicated functionality.

(a) (3 points) Which of the following op amp configurations would you use in order to get an input-output relationship of the form: $V_{out} = (1 + \frac{R_f}{R_s})V_{in}$?

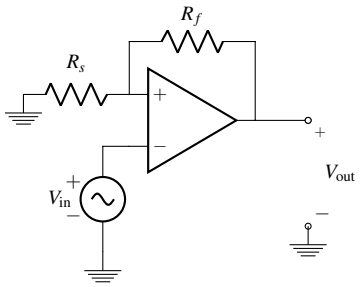
(A)



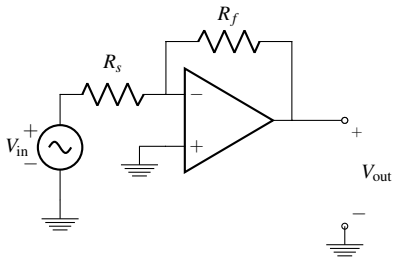
(B)



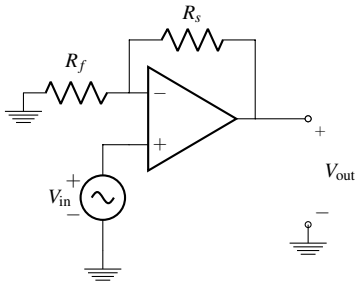
(C)



(D)

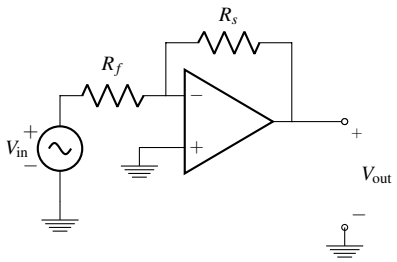


(E)

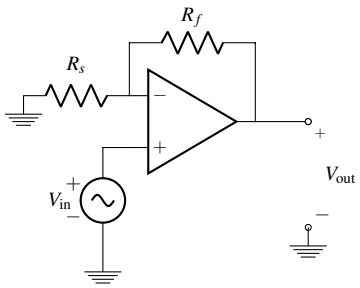


(b) (3 points) The circuit from part (a) can only multiply the input by positive numbers, and your boss tells you that you need to implement negative coefficients as well. Which of the following configurations results in $V_{out} = -\frac{R_f}{R_s} V_{in}$?

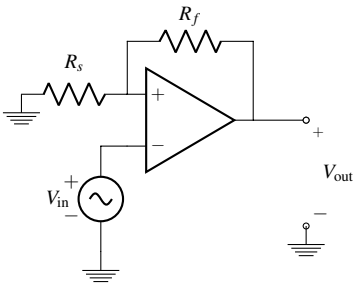
(A)



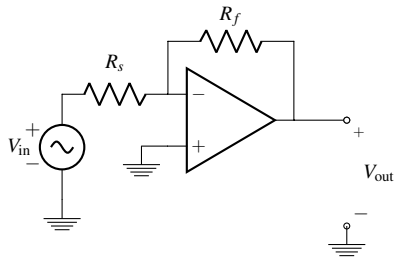
(B)



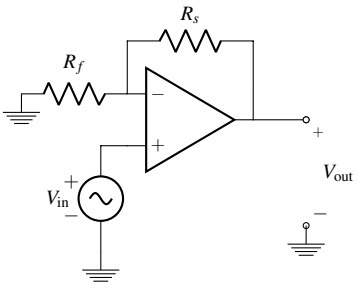
(C)



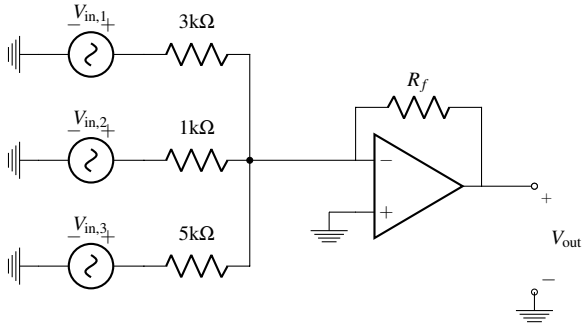
(D)



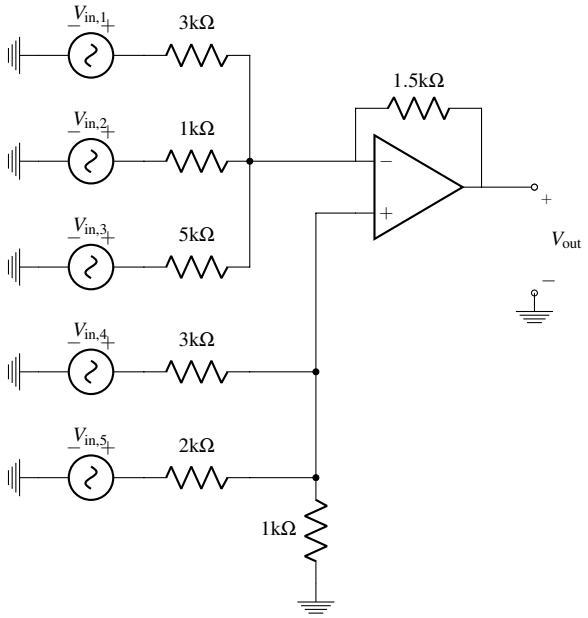
(E)



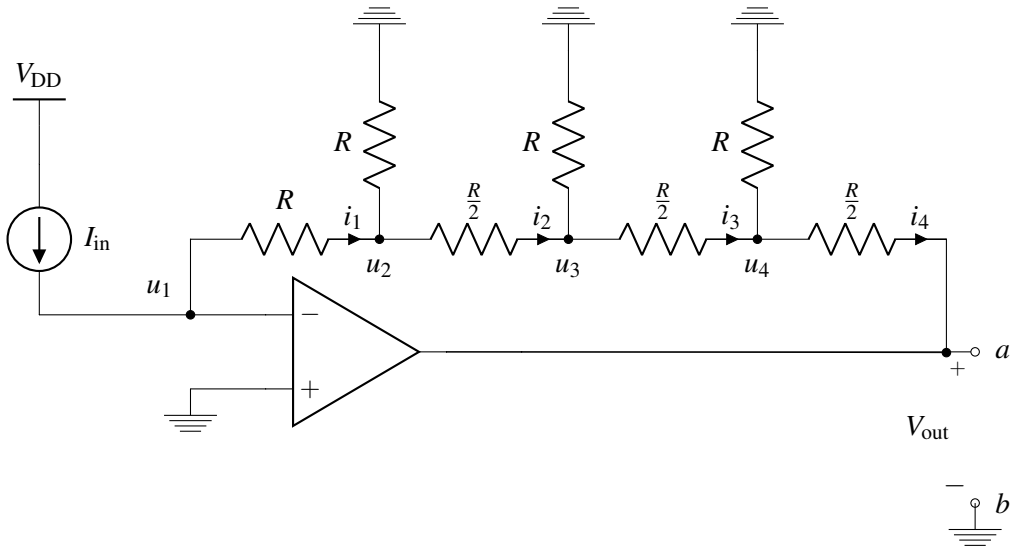
(c) (4 points) Now that you have both positive and negative coefficients, your next step is to combine multiple inputs into one output, using the following circuit. Express V_{out} in terms of $V_{\text{in},1}$, $V_{\text{in},2}$, $V_{\text{in},3}$, and R_f.



(d) (4 points) However, your boss points out that your design above doesn't allow for a mixture of positive and negative coefficients. Determined to succeed, you design the following circuit. What is the output of your new design as a function of the input voltages $V_{\text{in},1}$, $V_{\text{in},2}$, ..., $V_{\text{in},5}$?



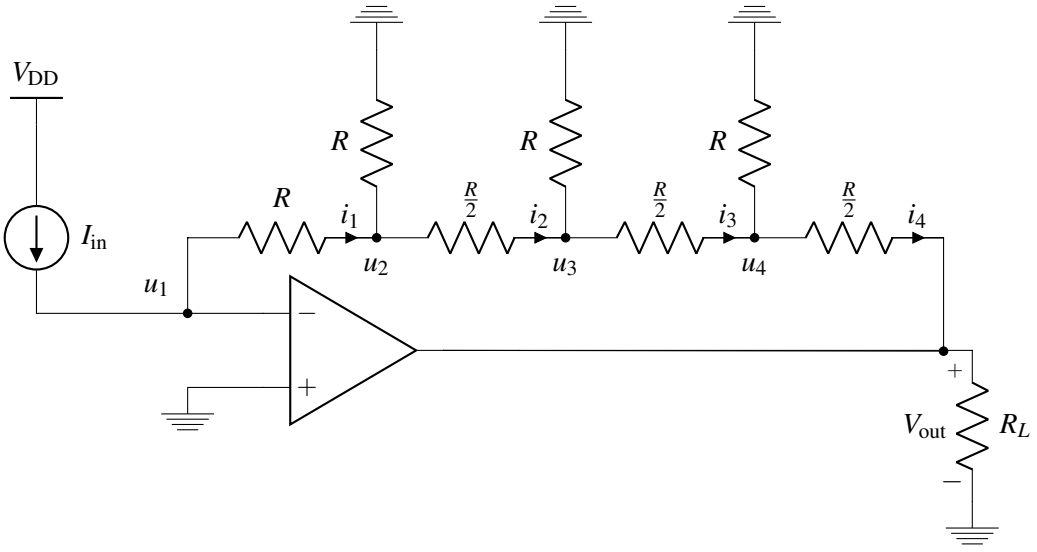
After successfully tackling the previous task and creating a weighted voltage summer, your mentor presents you with another problem. Your job will be to analyze the following circuit. Your mentor claims that you can use this circuit to convert an input current to an output voltage.



(e) (4 points) To verify his claim, analyze the circuit and calculate the currents labeled i_1, i_2, i_3, i_4, and the output voltage V_{out}. What are their values?

(f) (4 points) What is the Thevenin equivalent voltage and the Thevenin equivalent resistance between terminals a and b in the circuit above?

(g) (4 points) As is the case in most real-world applications, you want to use this incoming signal in order to drive a load that will actuate something. That "something" can be a speaker, a motor, or a heater among other things. Which of the quantities you calculated in part (e) (i_1, i_2, i_3, i_4, V_{out}), if any, will change if you connect a load resistance as shown in the figure below?



12. MP3 Player (18 points)

Smartphones store songs as a sequence of binary numbers (0s or 1s) called "bits" that must be converted to analog voltages before the song is played through a headset or speaker. The circuits that achieve this are called "Digital to Analog Converters", or DACs for short. Let's design a DAC!

(a) (4 points) You build the following 4-bit DAC:

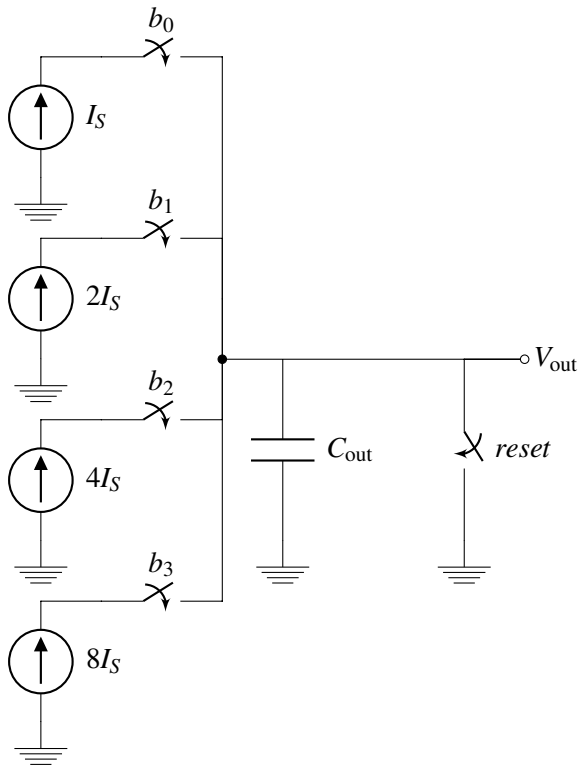


Figure 5: Current Source 4-bit DAC circuit

You circuit converts a sequence of 4 bits to a voltage as follows: Initially, the capacitor, C_{out}, is discharged, so $V_{\text{out}}(0) = 0$. Then, with the *reset* switch open, the switches b_0 - b_3 are controlled by the input bit sequence: If bit b_i has a value of "1" then the corresponding switch is closed; if it has a value of "0" the switch is open. After a fixed amount of time, t_{charge}, all the b_i switches are opened, and the output voltage, $V_{\text{out}}(t_{\text{charge}})$, is measured.

What is the value of C_{out} that makes the largest possible output voltage, $V_{\text{out,max}}(t_{\text{charge}})$, equal to 3V? Let $t_{\text{charge}} = 20\mu$s and $I_s = 2\mu$A.

Disclaimer: *Normally, open-circuiting a current source (which happens here when one of the switches b_i is open) can be dangerous. In this problem, please assume that the current source is automatically shut off when connected to an open circuit.*

(b) (4 points) You show your circuit to your TA, Ben, who reminds you that it's really hard to build a current source. Luckily for you, Ben is very resourceful and provides you with a circuit of his own. His DAC uses capacitors sharing charge to produce different voltages.

To remind you how this idea works he tells you to analyze the circuit in Figure 6. For time $t < 0$, the switch is open and the capacitors are charged to voltages V_1 and V_2, respectively. At time $t = 0$ the switch is closed. What is the voltage V_1 after the charges have redistributed?

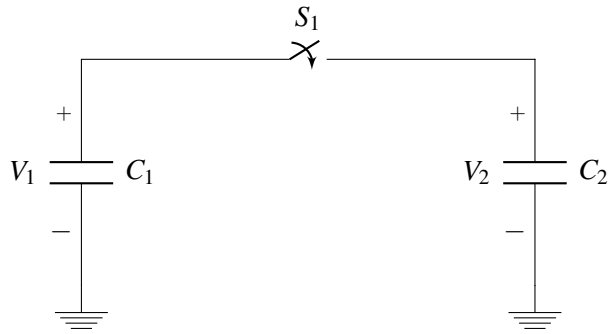


Figure 6: Capacitor Charge Sharing

Use the following values: $C_1 = 4\text{F}$, $C_2 = 8\text{F}$, $V_1 = 3\text{V}$, $V_2 = 6\text{V}$.

Following Ben's advice, you build a full DAC, shown in Figure 7. It operates in two phases and is controlled by a bit signal b, which can be 0 or 1. The table below indicates the state of each switch for both phases.

Switch	**Phase 1**	**Phase 2**
S_1	closed if $b = 1$, open otherwise	open
S_2	closed if $b = 0$, open otherwise	open
S_3	open	closed

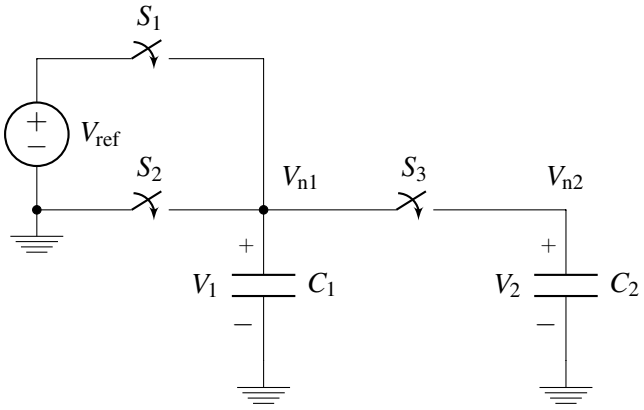


Figure 7: DAC Circuit Diagram

(c) (3 points) Draw the circuit that corresponds to the DAC circuit diagram (Figure 7) during **Phase 1** when $b = 1$.

(d) (3 points) Draw the circuit that corresponds to the DAC circuit diagram (Figure 7) during **Phase 2** when $b = 1$.

(e) (4 points) The circuit repeatedly cycles through Phases 1 and 2. In each step, the value of the control signal b represents one "bit" of the number to be converted. Given that $C_1 = C_2$, fill in the values of V_{n1} (voltage of C_1 measured in Phase 1) and V_{n2} (voltage of C_2 measured in Phase 2) in the table below. The first two rows are filled in for illustration. Assume C_2 is initially discharged at the beginning of Step 1.

Step	**b**	$\mathbf{V_{n1}}$ **in Phase 1**	$\mathbf{V_{n2}}$ **in Phase 2**
1	0	0V	0V
2	1	V_{ref}	$\frac{1}{2}V_{ref}$
3	1	a	b
4	1	c	d