Recipe: Charge Sharing!

March 16, 2017

1 What Is Charge Sharing?

Charge sharing, quite simply, is the sharing of charges among capacitors. You have entered this section of our esteemed cookbook having conquered the messy but rewarding world of resistive circuits. With blood afresh on your hands, and armed with the fruits of your toil, it is now time for you, the intrepid 16A Circuit Solver, to tackle that elusive final frontier: capacitors.

Before we *charge* headlong into battle, let's recall a few *ground* rules about capacitors[1]:

- In steady state, no current flows through them[2]
- In steady state, charges will be stored on the parallel plates of each capacitor. The charges stored on each plate of *a capacitor* will be equal in magnitude, and opposite in sign.
- These charges, stored on the parallel plates of a capacitor, go hand-in-hand with a *voltage difference* across the plates of the capacitor. Voltage always drops from the plate holding positive charge to the plate holding negative charge.

A lot of capacitor problems involve circuits with essentially voltage/current sources, capacitors, and switches. We can play around with opening and closing these switches, basically creating different *phases* of the circuit. Each phase actually corresponds to a different circuit. But these circuits are all linked to one another. Between two consecutive phases, the charges will move between different capacitors. This charge sharing recipe will help us formalize how, and where, charge is *shared* in the circuit, and give us a tried and tested method to approach these problems. In other words, it is our battle armor, and needless to say, shock-proof.[3]

Oh, also. We can hear you asking. Why might people want to *make* these circuits? You'll find out soon.

[1] We'll give you a second to collectively groan at those horrible, horrible puns

[2] It simply can't! Capacitors are, simplistically, just parallel plates with a non-conducting material (more accurately, a dielectric) between them.

[3] Again, profuse apologies.

2 Total Prep Time

Anywhere from five minutes to five hours depending on your circuit... Ok just kidding, we're nice people.

3 Ingredients

- **Your circuit (which usually has more than one "phase" depending on the positions of the switches in the circuits)**
- Sign conventions
- Circuit drawing skillz
- Identification of nodes in a circuit
- Relationship between charge and voltage across a capacitor
- Law of conservation of charge
- Branch voltages and KVL

4 Directions

1. **Branch voltage labeling**: Label the voltages across all the capacitors. Choose whichever direction (polarity) you want for each capacitor – this means you can mark any one of the plates with the + sign, and then you can mark the other plate with the − sign. Just make sure you stay consistent with this polarity across phases!
2. **Circuit drawing**: Draw the circuit in each phase. *Remember: keep polarities of voltages consistent across all phases!*
3. **(Using your solution for the circuit in phase $i-1$)** Solve the circuit in phase i!
   (a) Identify all the nodes in the circuit. As in nodal analysis, an intersection of *two or more elements* constitutes a node. Label all the node voltages.
   (b) Write the voltage differences across each capacitor according to the polarities you have defined and the node voltages you labeled earlier.
   (c) Use the relationship between charge and voltage across a capacitor ($Q = CV$) to determine the charge on *each plate on each capacitor*, in terms of the node voltages and capacitances. (*Stop to taste:* Make sure to convince yourself of the sign of charge on each plate! The plate marked with the + sign should have charge $+Q$, and the plate marked with the − sign should have charge $-Q$.)

(d) Identify the *floating nodes*. Floating nodes are nodes that are not connected to a voltage source or an explicit ground.[4] For each floating node, mark the plates of capacitors that are connected to it. Then, the law of conservation of charge for this floating node says: "The total charge on these plates will remain the same in phase i and phase $i-1$!" Why do you think this is true? Because these charges are basically *shared* between the plates – they can travel from one plate to another, but they cannot go anywhere else.

(e) Write the equation for charge conservation at all the floating nodes in phase i. At this point, you may need to write KVL to find the voltage that you are trying to solve for. Hence, determine the node voltages in the circuit for phase i.

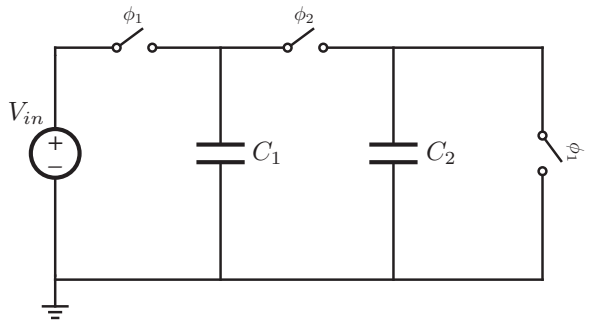
(f) Using the node voltages, determine the voltage difference across all the capacitors according to the polarities marked. Then, calculate the charge stored in each capacitor. We have now solved the circuit for phase i! Hooray.

4. **Repeat step 3 until all phases are done.**

5. **Your circuit is now solved and demystified! It's now time to enjoy the fruits of your toil, which are...more circuits. We're sorry.**

5 Example Circuit 1 - Capacitance Sensor

Let's begin with the following circuit. You may be familiar with it from the capacitive touch-screen lab:



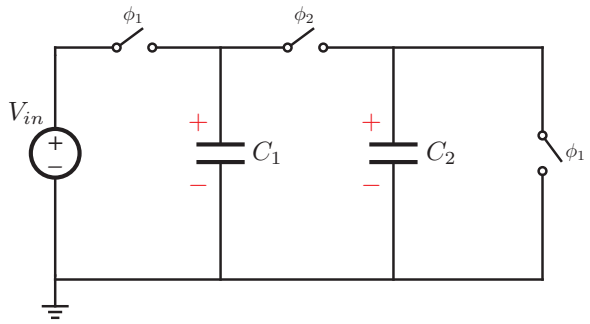
The switches labeled ϕ_1 are closed in phase 1 and open in phase 2. The switches labeled ϕ_2 are open in phase 1 and closed in phase 2. When a

[4] Keep in mind that nodes that we set as reference nodes are still floating nodes, unless they were explicitly set to ground. If this is confusing, don't worry about it too much.

switch is "open" it behaves like an open circuit. When a switch is "closed" it behaves like a short circuit.

(a) **Branch voltage labeling**

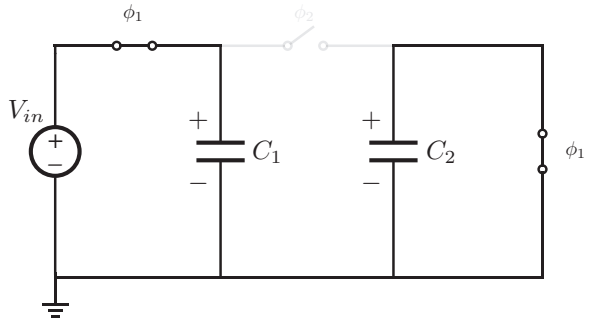
There are two capacitors in the circuit, C_1 and C_2. Here we place the $+$ sign on the two top plates and the $-$ sign on the bottom plates. It may be good practice to try messing around with these signs and showing that the procedure still works.



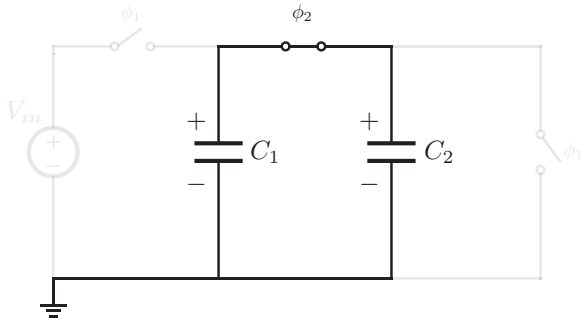
The reason that we write these signs is to be consistent with charge polarity from phase to phase. You can think of it like a guess. We are guessing that the top plates of C_1 and C_2 have positive charges, and that the bottom plates have negative charges. It turns out that this guess does not matter. If this is confusing, try to flip the signs ($-$ signs on the two top plates and $+$ signs on the bottom plates) and go through the procedure. The result will be the same!

(b) **Circuit Drawing**

We have two phases in the circuit - phase 1 (ϕ_1) and phase 2 (ϕ_2). So let's replace the switches with short circuits and open circuits as needed.



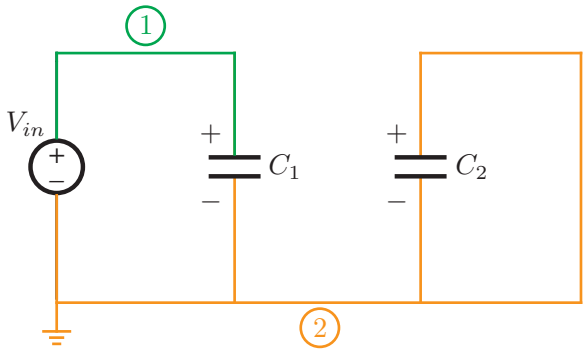
Very cool. One small thing about the figures. Notice how we kept the $+$ and $-$ signs that we decided on in part 1. The 'off' parts of



the circuit are greyed out so that you can see exactly how we modify the circuit between the two phases.

(c) **Solve the circuit!**

Arthur C. Clarke said that "any sufficiently advanced technology is indistinguishable from magic." This is where the magic happens. Let's start with phase 1. Label the nodes.



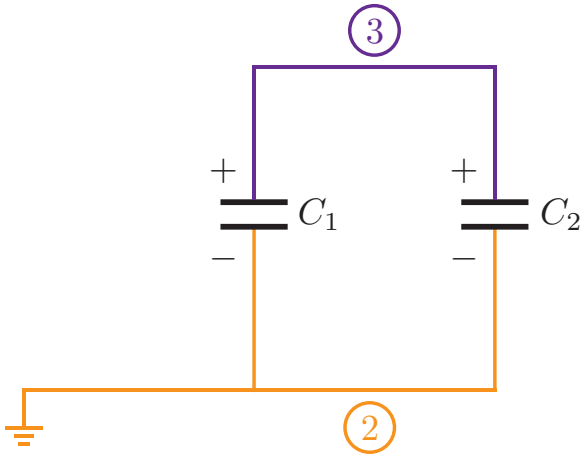
Now we continue with our procedure. All of the node voltages in this phase are known. $V_1 = V_{in}$ and $V_2 = 0$ is our reference voltage. We can use this to find the charge on each capacitor. Charge is given by capacitance $\times$ $(V_{+plate} - V_{-plate})$

$$Q_{C_1,\phi_1} = C_1 (V_1 - V_2) = C_1 V_1$$

$$Q_{C_2,\phi_1} = C_2 (V_2 - V_2) = 0$$

We know every node voltage in phase 1. Let's move on to phase 2. Label the nodes.

In phase 1, we knew every node voltage. In phase 2, we do not. V_2 is still our reference voltage. But node 3 is *floating*. Its voltage is



determined by charge that exists from the previous phase. To find this voltage, we continue with our procedure. Write the charge on each capacitor.

$$Q_{C_1,\phi_2} = C_1 \left(V_3 - V_2\right) = C_1 V_3$$

$$Q_{C_2,\phi_2} = C_2 \left(V_3 - V_2\right) = C_2 V_3$$

So how can we use this information to solve for the unknown voltage V_3? We use conservation of charge. The sum of all charge connected to node 3 must be the same as the sum of all capacitor charges from phase 1. That means:

$$Q_{C_1,\phi_1} + Q_{C_2,\phi_1} = Q_{C_1,\phi_2} + Q_{C_2,\phi_2}$$

We know all of these charges! Plug in the results from our previous analysis:

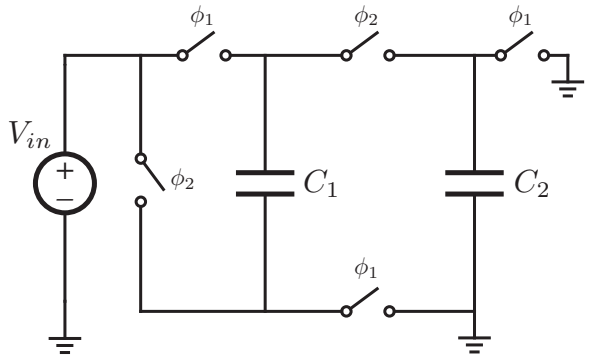
$$C_1 V_{in} = C_1 V_3 + C_2 V_3$$

$$V_3 = \frac{C_1}{C_1 + C_2} V_{in}$$

No circuit can stop us!

6 Example Circuit 2 - Switched Capacitor

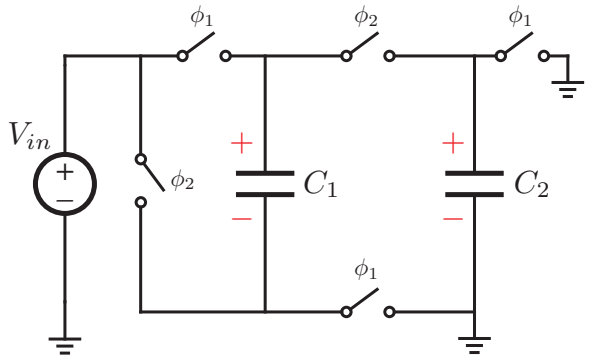
Now we will move on to a slightly more involved example. We'll see how nicely our procedure works:



The switches labeled ϕ_1 are closed in phase 1 and open in phase 2. The switches labeled ϕ_2 are open in phase 1 and closed in phase 2. Begin the procedure:

(a) **Branch voltage labeling**

There are two capacitors in the circuit, C_1 and C_2. Here we place the $+$ sign on the two top plates and the $-$ sign on the bottom plates. It may be good practice to try messing around with these signs and showing that the procedure still works.



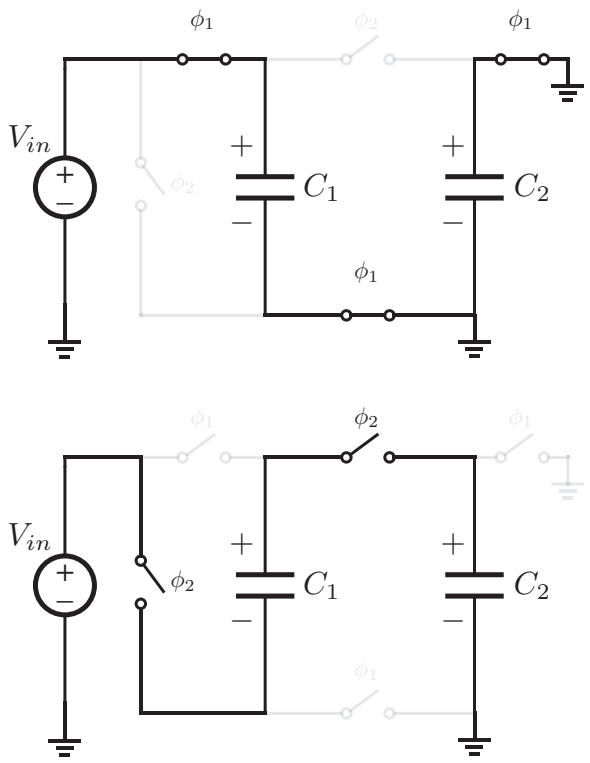
Great! We will keep this convention consistent in the remaining steps.

(b) **Circuit Drawing**

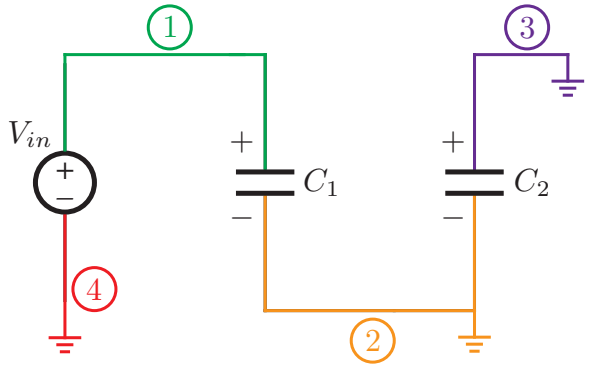
We have two phases in the circuit - phase 1 (ϕ_1) and phase 2 (ϕ_2). So let's replace the switches with short circuits and open circuits as needed.

(c) **Solve the circuit!**

Easier said than done, right? Let's start with phase 1. First, let's identify the nodes. Notice that we have been very explicit with our nodes, even identifying a few connected nodes twice. If you feel



comfortable, this is not necessary. But it cannot hurt. Remember, this recipe is a juggernaut, a bulldozer, a force that can be stopped only by the lack of its driver's will. And while it may be five or ten times slower than a more elegant method, it will never be wrong.



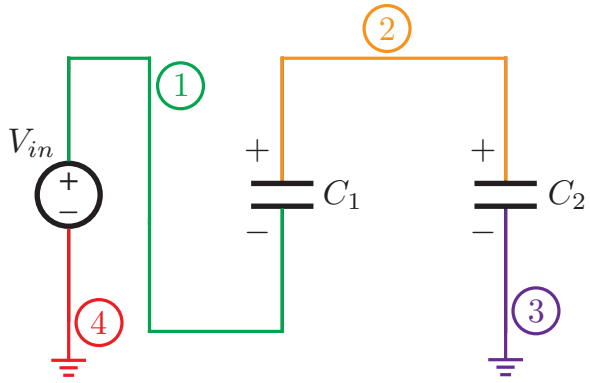
Notice that in this circuit we have a de-facto reference voltage (nodes 2, 3 and 4) that we set to 0V. Now given the polarities that we chose

earlier, we can find the charges on the + plates of C_1 and C_2. Just to reiterate, charge is given by capacitance $\times$ $(V_{+plate} - V_{-plate})$

$$Q_{C_1,\phi_1} = C_1 (V_1 - V_2)$$
$$Q_{C_1,\phi_1} = C_1 V_{in}$$

$$Q_{C_2,\phi_1} = C_2 (V_3 - V_2)$$
$$Q_{C_2,\phi_1} = 0$$

In phase 1 we know every single voltage in the circuit. Great. Now we cast off into the bitter unknown: phase 2. Again, we first label the nodes.



This time we are not so lucky. Nevertheless, we must persevere. Let's find the charge on our two capacitors in phase 2.

$$Q_{C_1,\phi_2} = C_1 (V_2 - V_1)$$
$$Q_{C_1,\phi_2} = C_1 (V_2 - V_{in})$$

$$Q_{C_2,\phi_2} = C_2 (V_2 - V_3)$$
$$Q_{C_2,\phi_2} = C_2 V_2$$

In phase 2, we do not know every node voltage. The renegade node 2 is a *floating* node. That means that its voltage is fixed by charge stored in a previous phase. So let's look at the two connected plates. We have the + plate from C_1 and the + plate from C_2. At this point we can perform the final step of the analysis. We must equate the charge on these two plates from phase 1 and the charge on the two plates from phase 2. This is because of *conservation of charge*. The charges have nowhere to go! We trap them like rats in a maze, only

this maze is of the existential sort that funnels our analysis to the values of the voltages in the circuit.

At the node 2 we look at the signs on the attached plates. We have the + plate of C_1 and the + plate of C_2. So on the left side of the charge conservation equation, we will add Q_{C_1,ϕ_1} and Q_{C_2,ϕ_1}, and on the right side of the equation, we will add Q_{C_1,ϕ_2} and Q_{C_2,ϕ_2}.

$$Q_{C_1,\phi_1} + Q_{C_2,\phi_1} = Q_{C_1,\phi_2} + Q_{C_2,\phi_2}$$
$$C_1 V_{in} + 0 = C_1 (V_2 - V_{in}) + C_2 V_2$$

Now we have one equation and one unknown (V_2) so we can solve. This leads us to the result:

$$V_2 = \frac{2C_1}{C_1 + C_2} V_{in}$$

Yes!

7 Example Circuit 3 - SAR ADC

If the previous circuit wasn't enough, let's look at a famous circuit introduced in discussion. We can use this circuit in an analog-to-digital converter to do what we call a binary search (check wikipedia for SAR ADC, it's a very cool circuit). Here we go:

It's scary, I know. But even in the face of seemingly insurmountable odds both you and the recipe will persevere.

(a) **Branch Voltage Labeling**

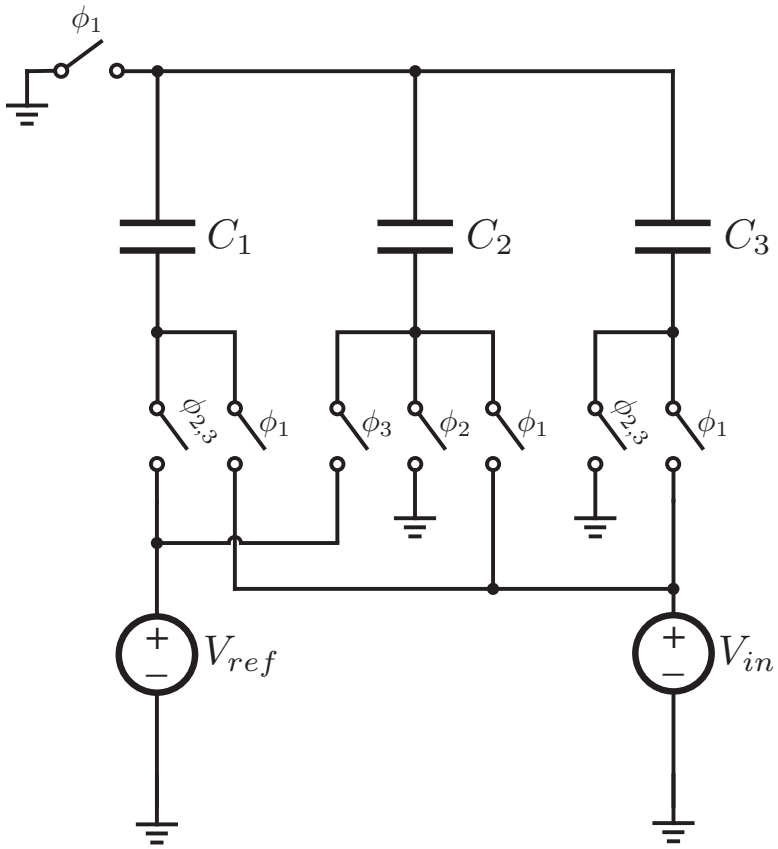
This circuit has three capacitors, C_1, C_2, and C_3. As before, we'll place the + signs on the top plates and the − signs on the bottom plates. And as before, you should try switching the orders of these signs around and see if you get the same answer at the end. (Spoiler alert: you will.)

(b) **Circuit Drawing**

Now, in this circuit, we have three phases: 1, 2 and 3. As before, we draw the circuit in each of the phases replacing the switches by open circuits or short circuits as needed. Note that if a switch is marked as $\phi_{2,3}$, it simply means that the switch will be closed in phases 2 and 3, and open otherwise (in phase 1). Nothing new! :-)

(c) **Solve the Circuit!**

Remember that we're not just solving *a* circuit. We are actually solving three circuits, one for each phase. I'm sure you have a plethora of curses for the 16A staff fresh on your lips right now. But before you use them, hear us out...



Here's the circuit for phase 1. As earlier, we have identified all the nodes. Don't forget the ground node(s)!

Next, we calculate the charges on the + plates of C_1, C_2 and C_3 in terms of the node voltages V_1, V_2, and V_3. Note that $V_1 = 0$, $V_2 = V_{in}$, and $V_3 = 0$.

Then,

$$Q_{C_1,1} = (V_1 - V_2)C_1$$

giving

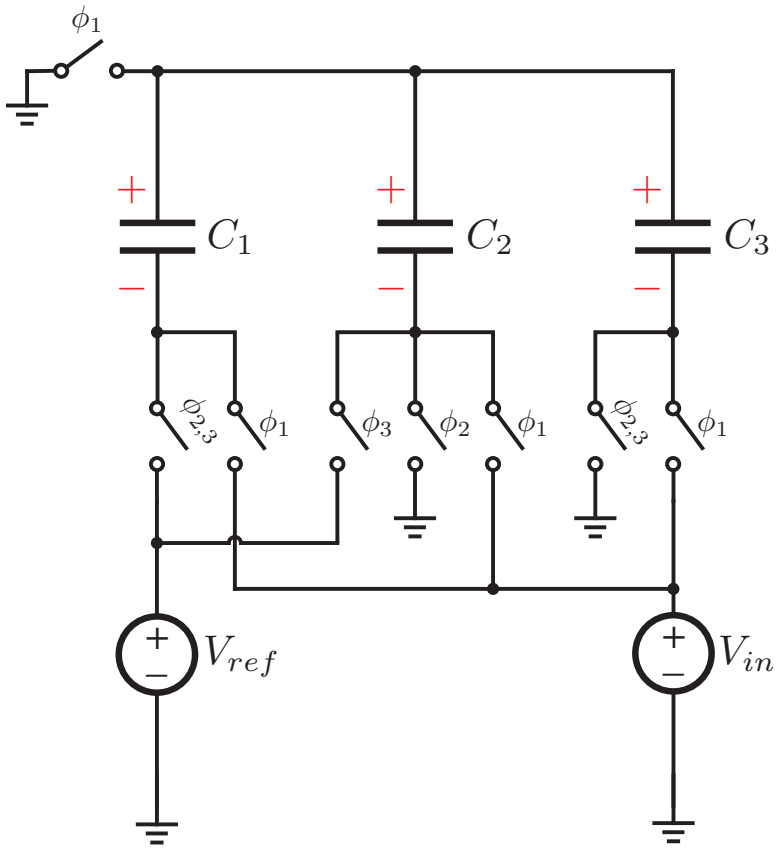
$$Q_{C_1,1} = -V_{in}C_1$$

and

$$Q_{C_2,1} = (V_1 - V_2)C_2$$
$$Q_{C_2,1} = -V_{in}C_2$$

similarly,

$$Q_{C_3,1} = -V_{in}C_3$$



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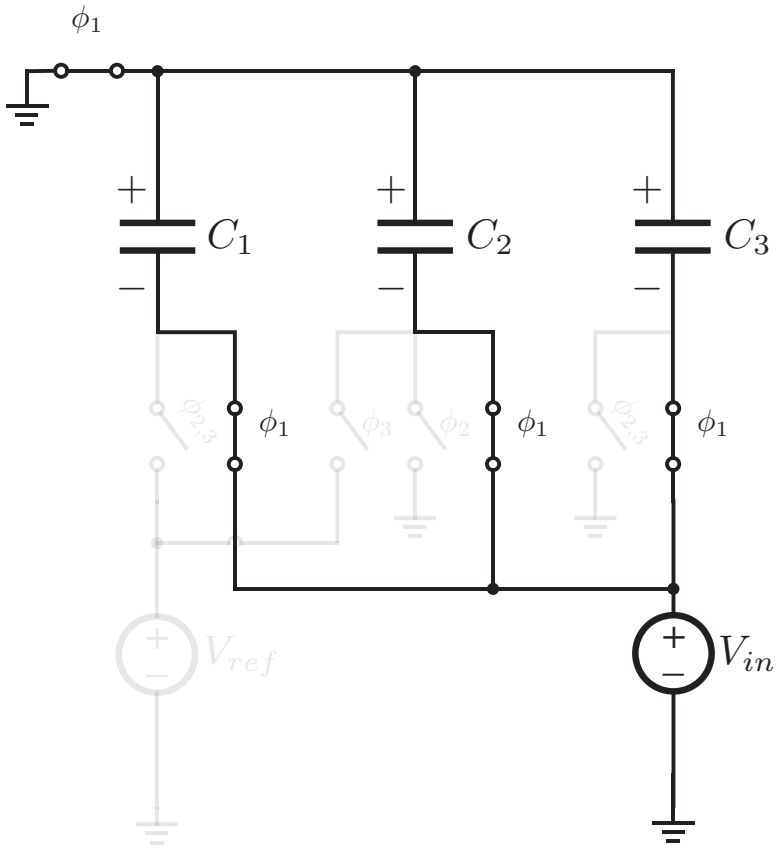
Note that all the capacitors are charged to the same voltage, i.e. $-V_{in}$, *in this phase*. You might astutely observe that they are in parallel. If you did *not* astutely observe this, fear not. You don't need to have done so to solve this circuit.

So we know all the voltages and charges exactly in phase 1 (remember, we know V_{in}). Next up: phase 2! As before, label all the nodes and feel good about yourself. :-)

Note that we have labeled all the ground nodes with the same label, 3. We don't always have to do this but it's convenient to do so. Note that $V_3 = 0$, and $V_4 = V_{ref}$. But we do not know V_1 in this phase. We finally ran out of luck!

But, we're intrepid circuit solvers. We don't give up. Instead, we move on to the next step. We find the charges across C_1, C_2 and C_3 in phase 2.

$$Q_{C_1,2} = (V_1 - V_4)C_1$$

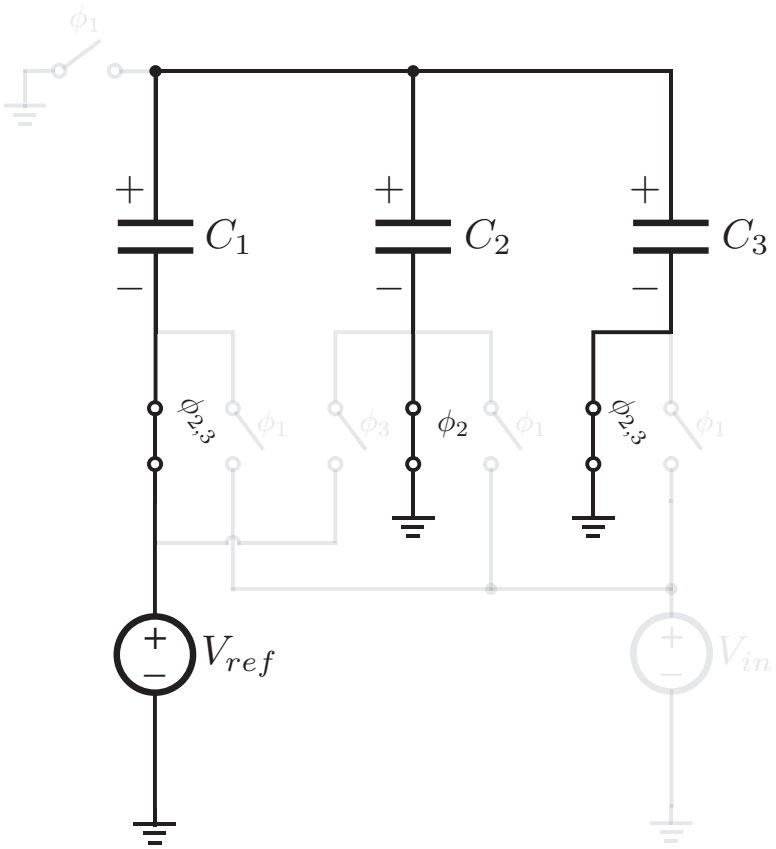


$$Q_{C_1,2} = (V_1 - V_{ref})C_1$$

$$Q_{C_2,2} = (V_1 - V_3)C_2$$
$$Q_{C_2,2} = V_1 C_2$$

$$Q_{C_3,2} = (V_1 - V_3)C_3$$
$$Q_{C_3,2} = V_1 C_3$$

Since we do not know V_1 in phase 2, we attempt to solve for it! To do this, let's identify where charge is conserved. Note that, in phase 2, node 1 is a *floating node* – which means that the *total charge* on all the plates connected to it (in this case, the top plates of 1, 2 and 3) cannot really go anywhere between phase 1 and phase 2. (Sure, the charges can flow from plate to plate. But ultimately, they are all still going to be residing somewhere on the green piece of metal that



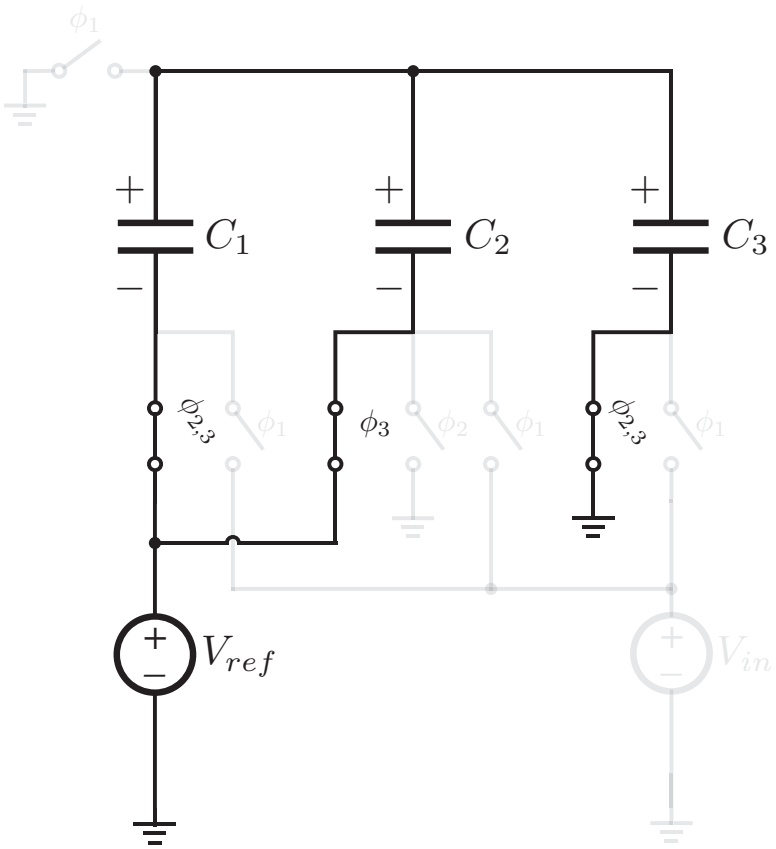
is part of the circuit. By the way, if you don't want to be identifying weirdly colored pieces of metal that charges are going to be trapped in, i.e. if electrons aren't your thing, worry not. There's an easier way to identify floating nodes. Any node that is not connected to a voltage source, current source or ground is going to be a floating node. Simply because there will be no source or sink of charge connected to that node.)

After that little ramble, we soldier on. We say that the total charge on all the plates connected to node 1 is conserved. This simply means that

$$Q_{C_1,1} + Q_{C_2,1} + Q_{C_3,1} = Q_{C_1,2} + Q_{C_2,2} + Q_{C_3,2}$$

Substituting our expressions for charges in phases 1 and 2 in, we'll get

$$-V_{in}C_1 - V_{in}C_2 - V_{in}C_3 = (V_1 - V_{ref})C_1 + V_1C_2 + V_1C_3$$



giving us

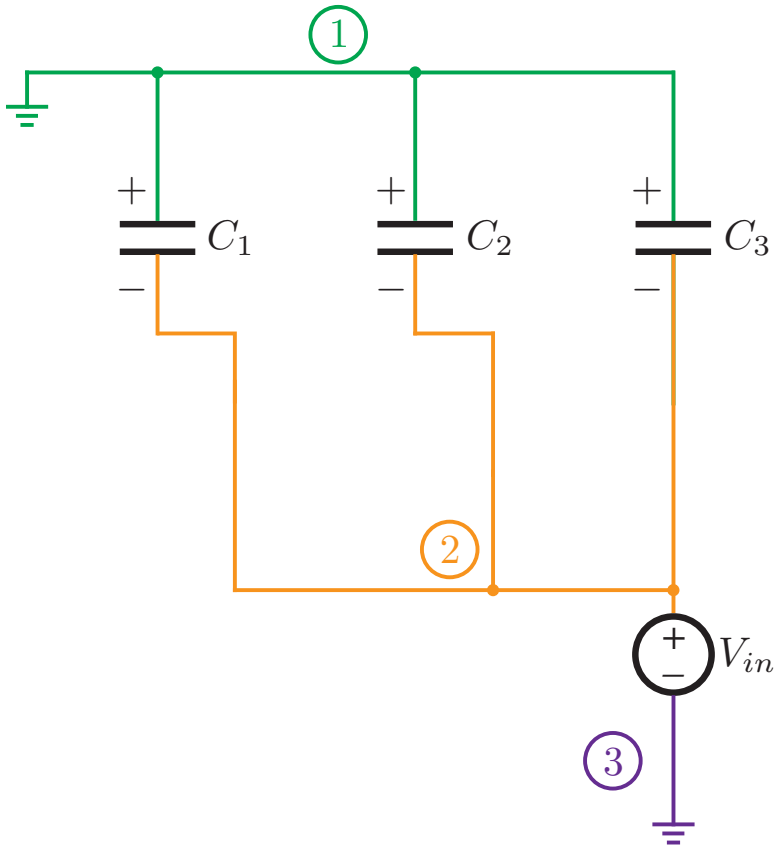
$$V_1 = \frac{V_{ref} C_1}{C_1 + C_2 + C_3} - V_{in}$$

Now, think about it. Is V_1 going to be positive or negative? That depends on a bunch of things – on the values of C_1, C_2, and C_3, as well as how V_{in} compares to V_{ref}. This very question is the crux of the SAR-ADC and how it works, and when we introduce specific values for C_1, C_2 and C_3, you'll see why more clearly. Yay! How exciting. Nod your head vigorously and happily and make affirmative noises at this stage; then, sober up when you remember that you have one more phase ahead of you.

But you shouldn't be afraid anymore. Again, label all the nodes!

Again, $V_3 = 0$ and $V_4 = V_{ref}$.

(Note that V_1 is again unknown in phase 3, and it is in fact different from V_1 in phase 2. This is because the bottom plate of C_2 has now been connected to V_{ref} instead of ground. So a change has been made in the circuit!)



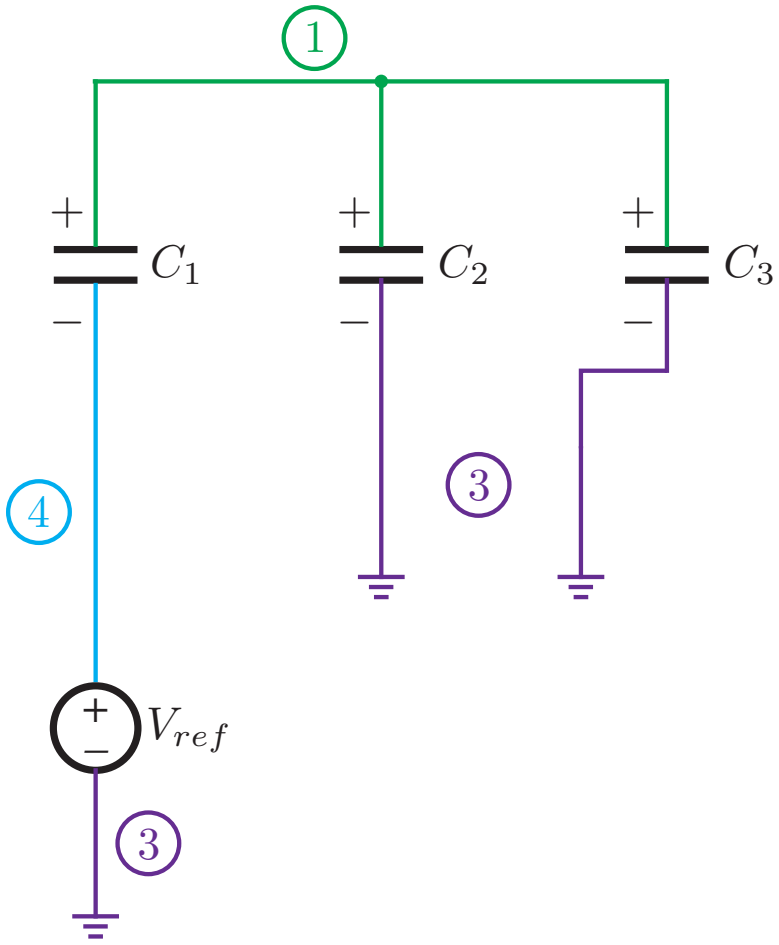
First, we find the charges across C_1, C_2 and C_3 in phase 3. You got this.

$$Q_{C_1,3} = (V_1 - V_4)C_1$$
$$Q_{C_1,3} = (V_1 - V_{ref})C_1$$

$$Q_{C_2,3} = (V_1 - V_4)C_2$$
$$Q_{C_2,3} = (V_1 - V_{ref})C_2$$

$$Q_{C_3,3} = (V_1 - V_3)C_3$$
$$Q_{C_3,3} = V_1 C_3$$

Next step: identify the floating node(s) in phase 3. Hint: you've already done this...



Yes, it's node 1. Give yourself a pat on the back! This means that the poor charges had nowhere to go between *all three phases*. All they've been able to do is haplessly scurry from plate to plate, perhaps searching for escape from the weird green maze but finding none.

Anyway, what this means in equations, if you prefer that sort of thing, is that

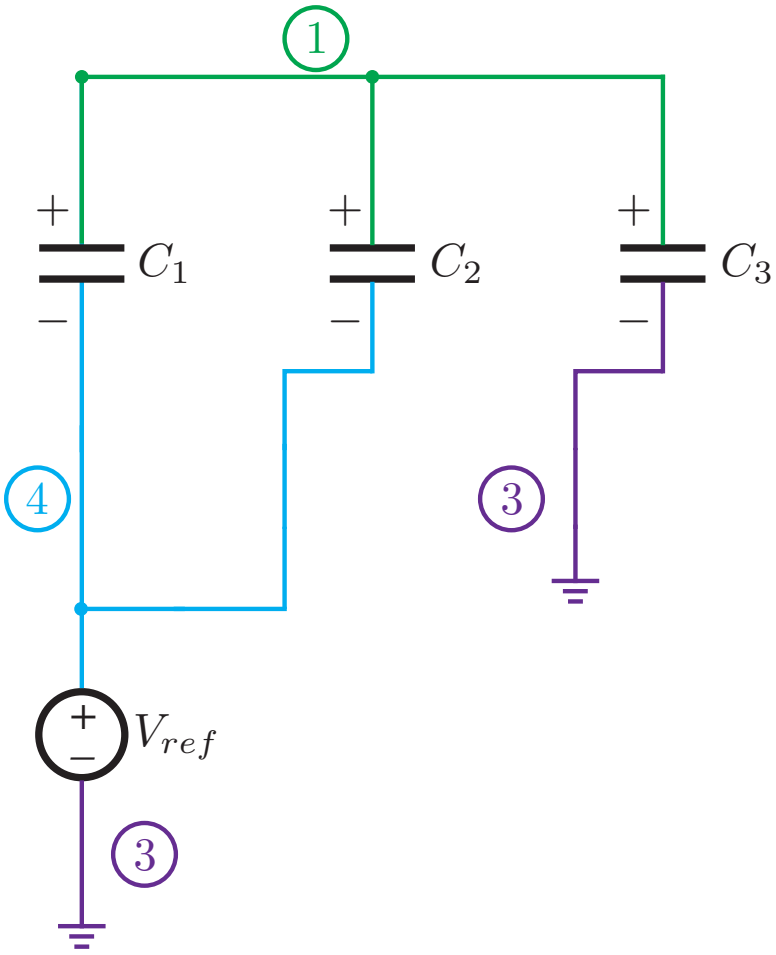
$$Q_{C_1,1}+Q_{C_2,1}+Q_{C_3,1} = Q_{C_1,2}+Q_{C_2,2}+Q_{C_3,2} = Q_{C_1,3}+Q_{C_2,3}+Q_{C_3,3}$$

We can use the part of the equation that says

$$Q_{C_1,1} + Q_{C_2,1} + Q_{C_3,1} = Q_{C_1,3} + Q_{C_2,3} + Q_{C_3,3}$$

Substituting our expressions for charge in phases 1 and 3, we get

$$-V_{in}C_1 - V_{in}C_2 - V_{in}C_3 = (V_1 - V_{ref})C_1 + (V_1 - V_{ref})C_2 + V_1C_3$$



Ultimately, we'll get

$$V_1 = \frac{V_{ref}(C_1 + C_2)}{C_1 + C_2 + C_3} - V_{in}$$

Again, whether V_1 is going to be positive or negative really will depend on a bunch of things. To see this more explicitly, let's set particular values for C_1, C_2 and C_3:

$$C_1 = 2\mu F$$
$$C_2 = 1\mu F$$
$$C_3 = 1\mu F$$

Plugging these values into our results, we will get the following answers for V_1 in phases 2 and 3:

Phase 2:

$$V_1 = \frac{V_{ref}}{2} - V_{in} \tag{1}$$

Phase 3:

$$V_1 = \frac{3V_{ref}}{4} - V_{in} \tag{2}$$

These answers should be ringing some bells in a land far, far away! To hear them, journey on to the discussion 7B worksheet, where this example is taken further. :)

8 A Little Note About Capacitors In Series and Parallel

Some of you might have looked at these examples, and noted that capacitors were sometimes in series in phases, and sometimes in parallel. You might have noticed that we did not apply the formulae for equivalent capacitance directly, anywhere.

We want to emphasize that in solving charge sharing problems, you *never need to use* these formulae. In fact, if you are at all unsure about whether the equivalent series/parallel capacitance formulae can be used safely, we recommend you do not use them. Small steps often get you further than giant leaps.