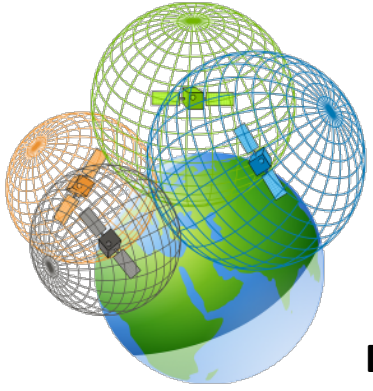


Welcome to EECS 16A!

Designing Information Devices and Systems I

Ana Claudia Arias and Miki Lustig

Fall 2021

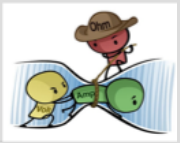
Module 2
Lecture 2
Introduction to Circuit Analysis
(Note 12)

Last Class (0203)…

Quantities	Analytical Symbol	Units
Current	I	Amperes (A)
Voltage	V	Volts (V)
Resistance	R	Ohms (Ω)

I ⇒ flows through an element
V ⇒ applied across an element
R ⇒ opposition to current flow

Electronic Materials
- Conductors
- Semiconductor
- Insulators



* **Charge** ⇒ Can be either positive or negative; basic element of eletric flow. Unit: Coulomb [C]

* **Current** ⇒ Net amount of charge that passes through some cross-section area over a period of time.

$$[A] \rightarrow I = \frac{dQ}{dt} \quad \frac{[C]}{[s]}$$

Last Class (0203)…

Quantities	Analytical Symbol	Units
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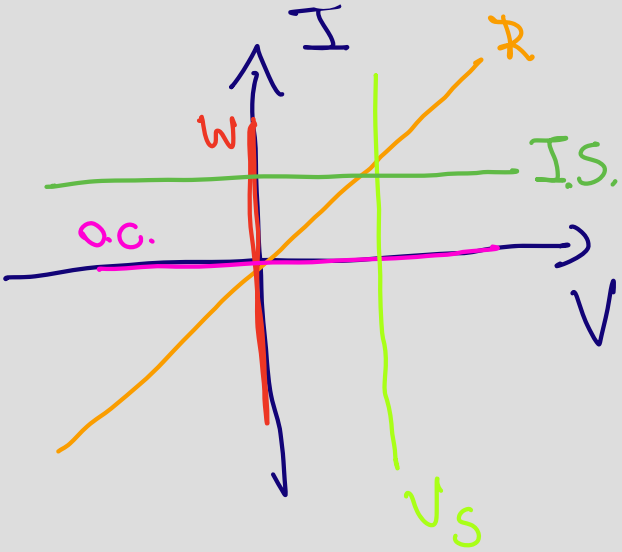
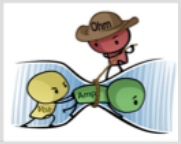
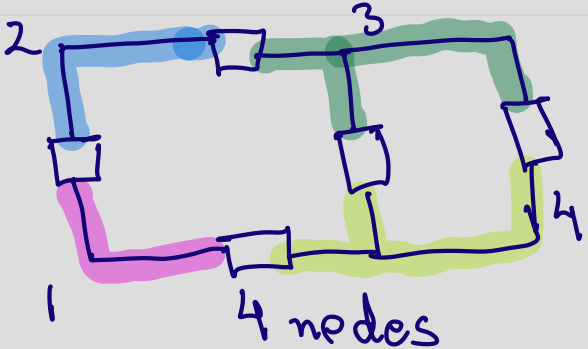


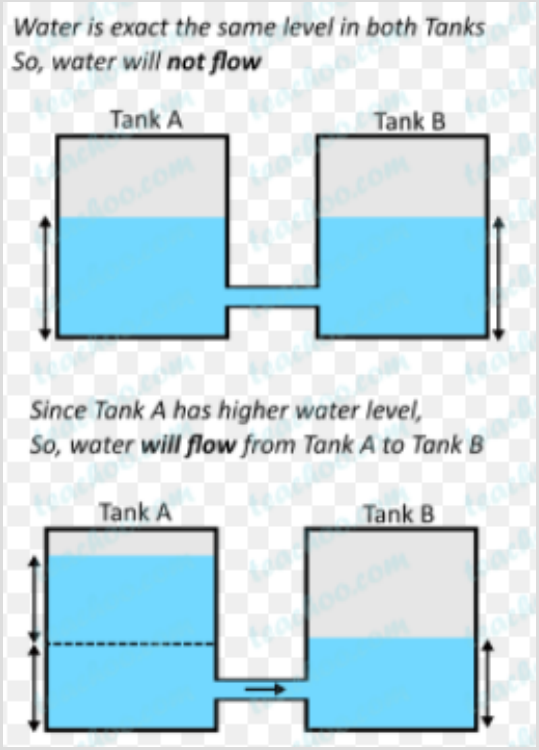


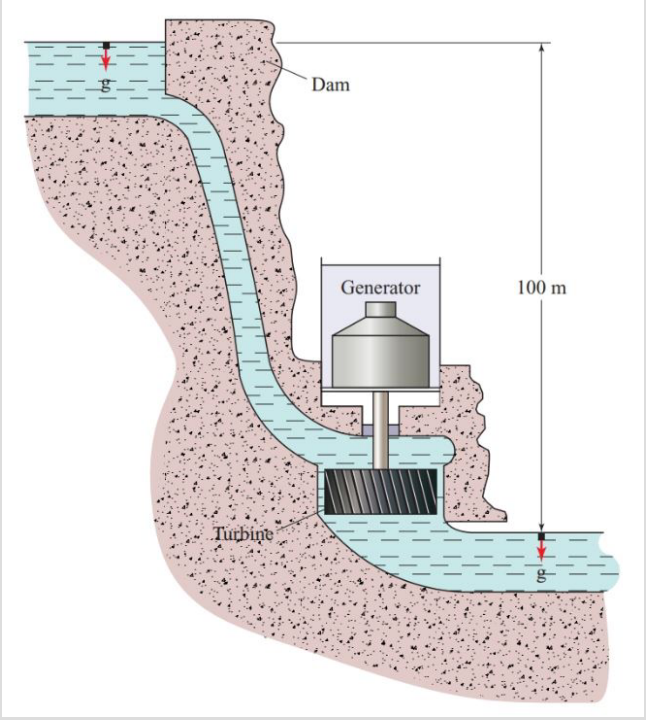


Today

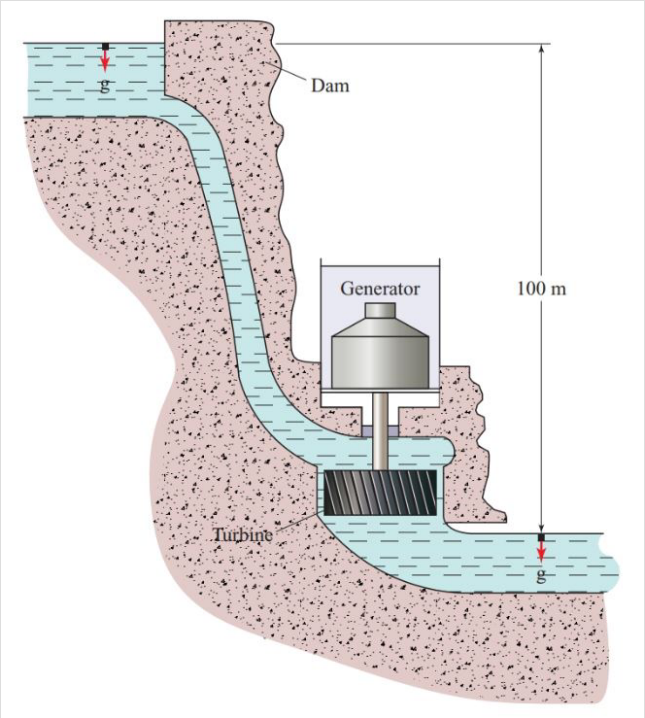
- KCL ; KVL ⇒ RULES
- Circuit analysis
- First operator!

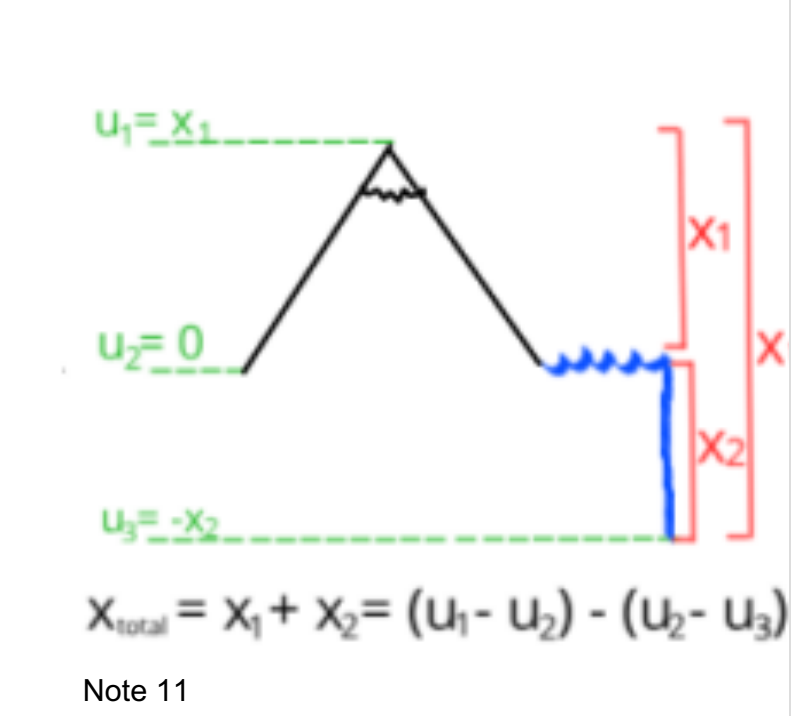
Potential Energy





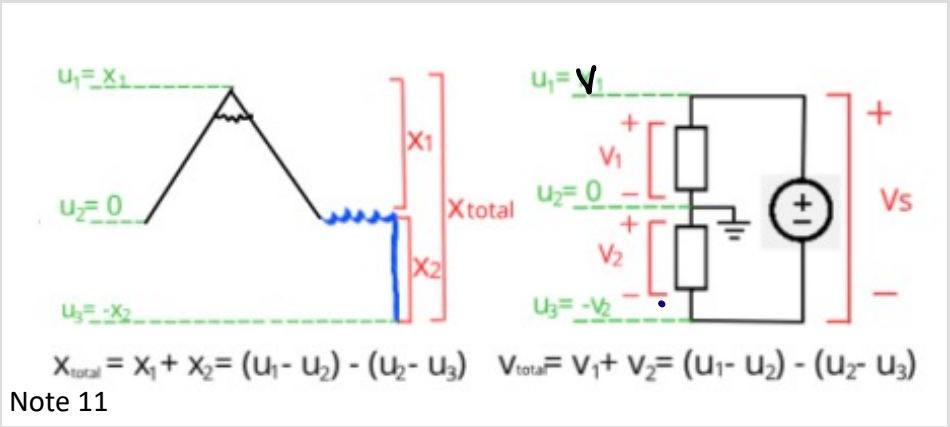
Potential and Voltage





Note 11

Electronic Devices depend on movement of charges



Note 11

U_1, U_2, U_3

potentials

$V_1 = U_1 - U_2$

$V_2 = U_2 - U_3$

$V_{total} = V_1 + V_2$

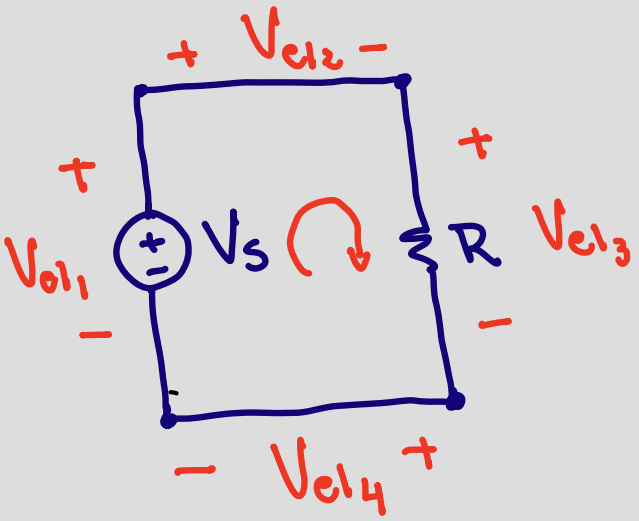
$V_{total} = V_S$

We always need to define a reference for potentials.

Ground = 0

Rules for circuit analysis: Kirchoff's Voltage Law (KVL)

Sum of Voltages across the elements in a loop equal zero



$$V_{el_1} - V_{el_2} - V_{el_3} - V_{el_4} = 0$$

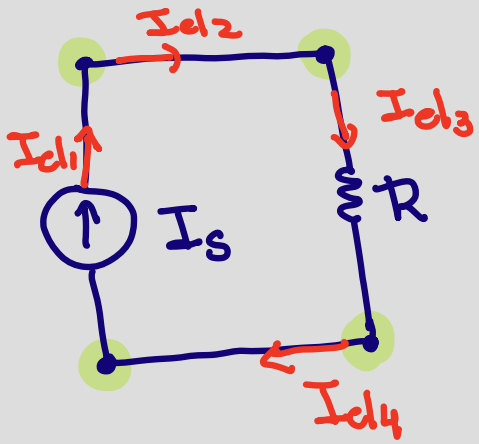
V_{el_1} + V_{el_2} − V_{el_3} − V_{el_4}

$$V_{el_1} = V_S$$

$$V_{el_3} = ?$$

Rules for circuit analysis: Kirchoff's Current Law (KCL)

The current flowing into any junction must equal the current flowing out



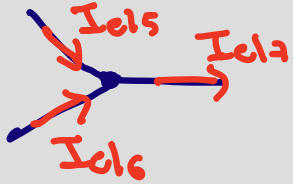
$$I_{cl_1} = I_{cl_2}$$

$$I_{cl_2} = I_{cl_3}$$

$$I_{cl_3} = I_{cl_4}$$

$$I_{cl_4} = I_{cl_1}$$

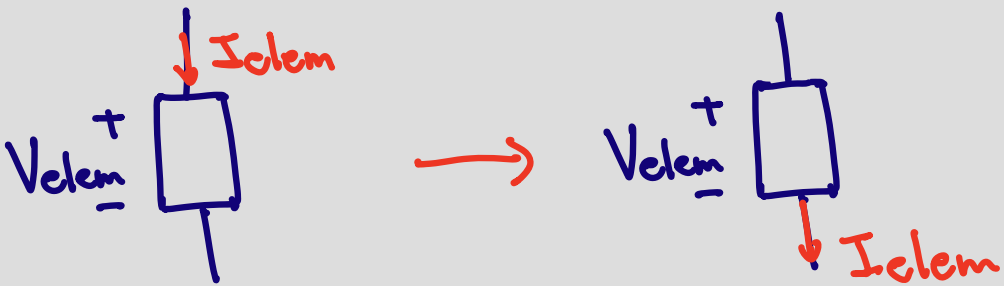
Example 2:



$$I_{cl_5} + I_{cl_6} = I_{cl_7}$$

Rules for circuit analysis: KCL within the element

The current flowing into any junction must equal the current flowing out



Same current!

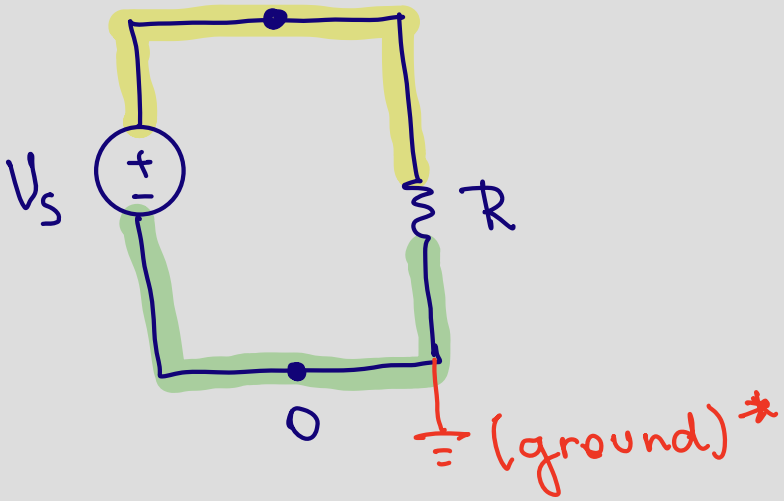
Both are allowed.

Ielem goes into a (+) or out of a (−) terminal

* Passive sign convention

Circuit Analysis Algorithm : step 1

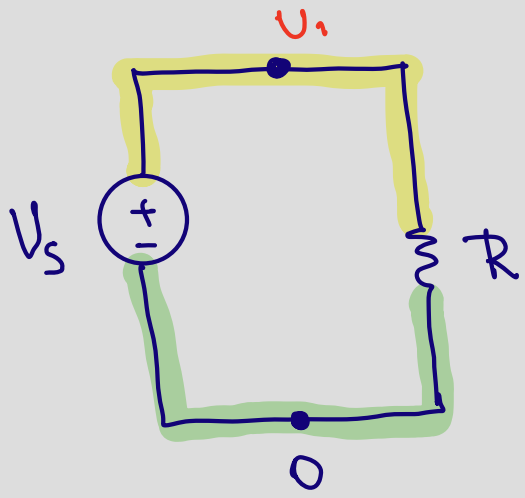
Pick a reference node and label it as 0 potential. All voltages measured relative to this node.



* Tells you where the reference is.

Circuit Analysis Algorithm : step 2

Label all remaining nodes as potentials U_i
$[U_1 \dots U_{N-1}]$

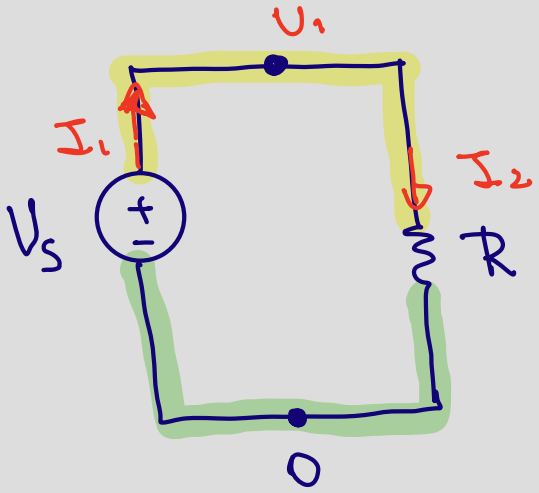


$U_1 - 0 = U_1 = V$

Voltage between node 1 and node "0".

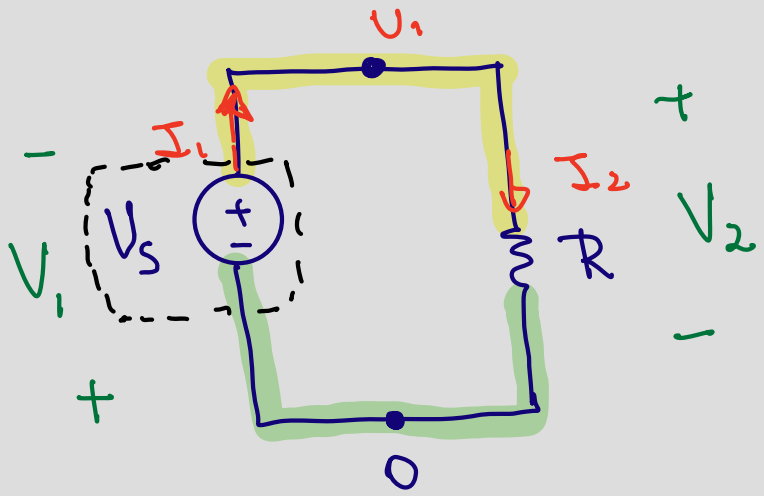
Circuit Analysis Algorithm : step 3

Label all branch currents with I_m
Arbitrarily pick directions of I_m
$[I_1 \ldots I_k]$



Circuit Analysis Algorithm : step 4

Add signs + and – element voltages to each element following the passive sign convention



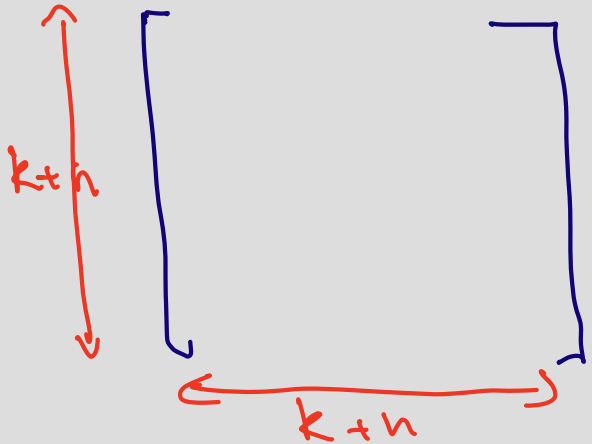
Circuit Analysis Algorithm : step 5

$A\vec{x} = \vec{b}$

$\vec{x}$:. unknowns

$\vec{b}$:. knowns / constants

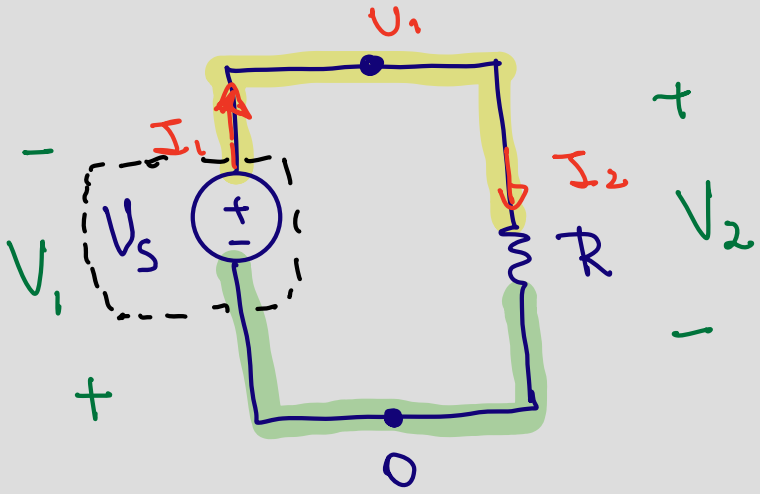
A :. knowns / constants



$$\vec{x} = \begin{bmatrix} i_1 \\ \vdots \\ i_k \\ v_1 \\ \vdots \\ v_n \end{bmatrix} \quad k+n \qquad \vec{b} = \begin{bmatrix} b_1 \\ \vdots \\ b_{k+n} \end{bmatrix} \quad k+n$$

Circuit Analysis Algorithm : step 6

Use KCL to fill as many rows of A as possible (linear independence) # Nodes -1 = N-1



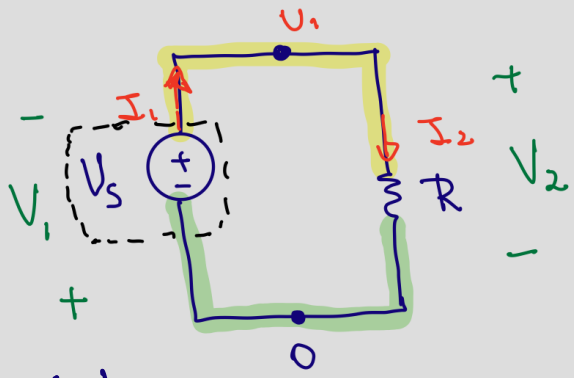
$$I_1 = I_2$$

$$I_1 - I_2 = 0$$

$$\begin{bmatrix} 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ V_1 \end{bmatrix} = \begin{bmatrix} 0 \end{bmatrix}$$

Circuit Analysis Algorithm : step 7

Use current-voltage relationships for each element to fill the rest of the A matrix



Voltage Element = $-V_S$

$V_{el_1} = 0 - V_1$

$V_1 = V_1 = V_S$

$$\begin{bmatrix} 1 & -1 & 0 \\ 0 & 0 & 1 \\ 0 & R & -1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ V_1 \end{bmatrix} = \begin{bmatrix} 0 \\ V_S \\ 0 \end{bmatrix}$$

$V_1 = V_S$

$I_1 = V_S/R$

$I_2 = V_S/R$

Resistor

$V_{el_2} = I_2 \cdot R$

$V_{el_2} = V_1 - 0 = V_1$

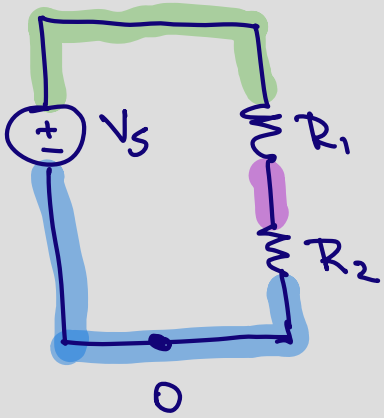
$V_1 = I_2 \cdot R$

$I_2 \cdot R - V_1 = 0$

Node Voltage Analysis – Voltage Divider

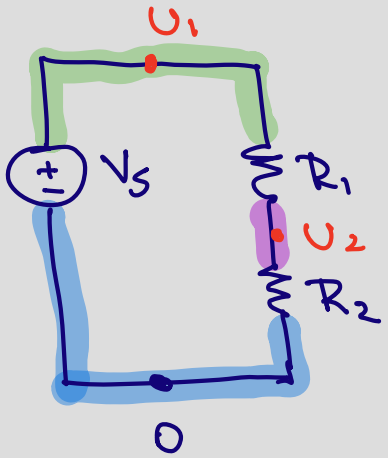
(Operator) → make circuit analysis faster

Step 1 – Pick a node and label it as ground



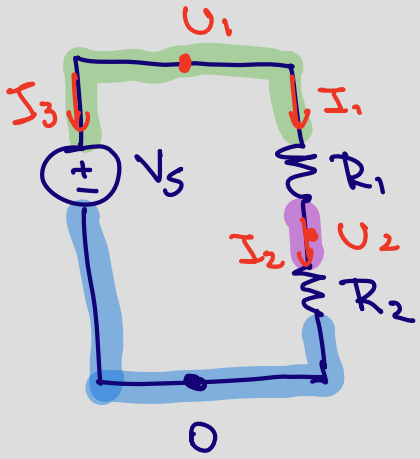
Node Voltage Analysis – Voltage Divider

Step 2 – Label all remaining nodes as some potential U_i.



Node Voltage Analysis – Voltage Divider

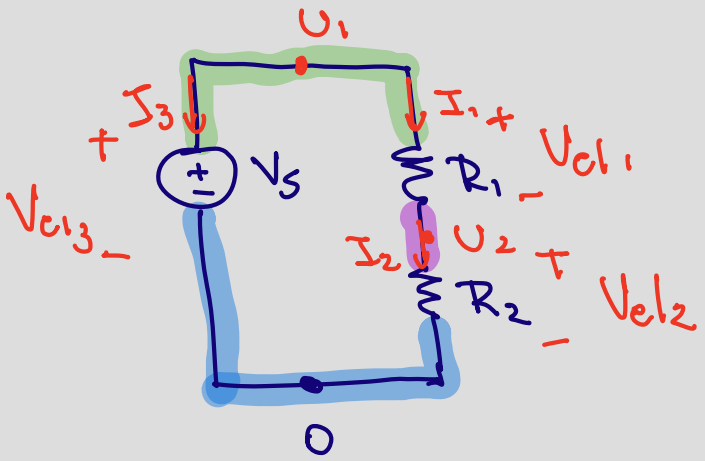
Step 3 – Label the current through every non-wire element in the circuit with I_n.



Node Voltage Analysis – Voltage Divider

Requires some thinking

Step 4 – Add +/- labels on each non-wire element, following the passive sign convention.



* Important!

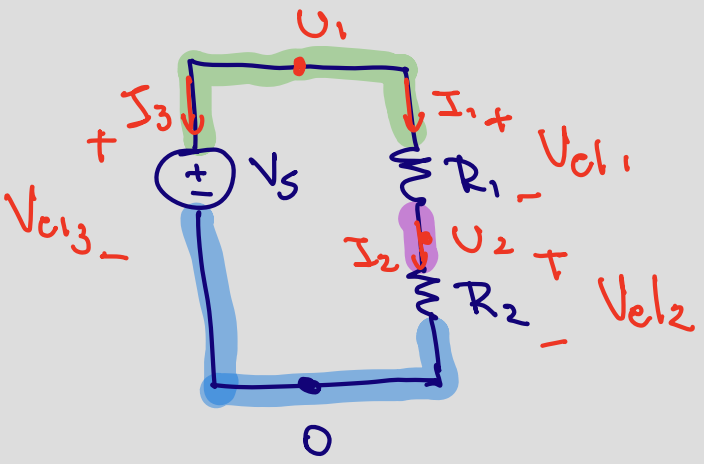
Passive sign convention: the current enters at the positive terminal and exits are the negative terminal.

Node Voltage Analysis – Voltage Divider

$A\vec{x} = \vec{b}$

Step 5 – Set up the relationship A consists of the unknown currents and potentials.

Identify the unknowns.

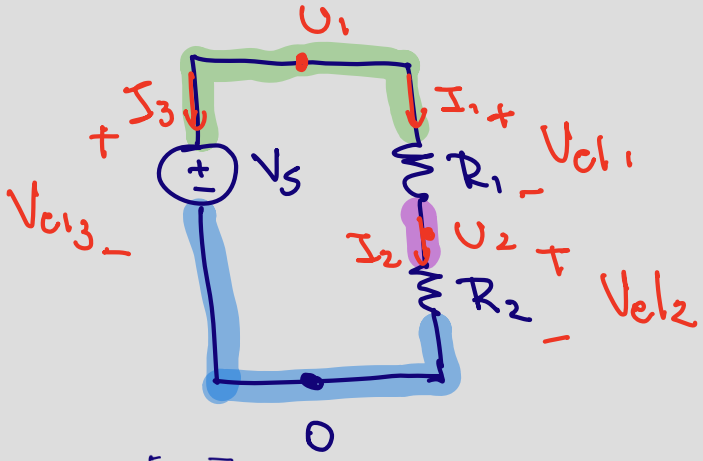


$$\vec{x} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ v_1 \\ v_2 \end{bmatrix}$$

Passive sign convention: the current enters at the positive terminal and exits are the negative terminal.

Node Voltage Analysis – Voltage Divider

Step 6 – Use KCL to fill in as many linearly independent rows in A and $\vec{b}$



$$\vec{x} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ V_1 \\ V_2 \end{bmatrix}$$

For $V_1 \Rightarrow 0 = I_1 + I_3$ (1)

For $V_2 \Rightarrow I_1 = I_2$

$I_1 - I_2 = 0$ (2)

KCL: the current flowing into a junction must equal the current flowing out of that junction.

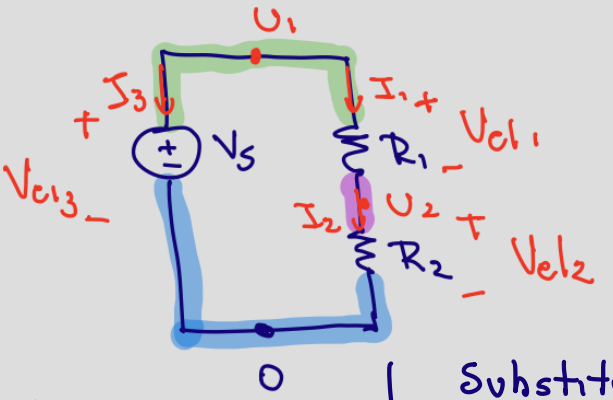
Node Voltage Analysis – Voltage Divider

Step 7 – Use the IV relationships of each of the non-wire elements to fill in the remaining rows of A and

the remaining rows of A ar

$= 0$ (1)

$= 0$ (2)



Voltage Def.

$V_{el_1} = V_1 - V_2$

$V_{el_2} = V_2 - 0 = V_2$

$V_{el_3} = V_1 - 0 = V_1$

Element IV

$V_{el_1} = R_1 I_1$

$V_{el_2} = R_2 I_2$

$V_{el_3} = V_S$

Substitution:

$El_1 \therefore V_1 - V_2 = R_1 I_1 \Rightarrow R_1 I_1 - V_1 + V_2 = 0$ (3)

$El_2 \therefore V_2 = R_2 I_2 \Rightarrow R_2 I_2 - V_2 = 0$ (4)

$El_3 \therefore V_1 = V_S$ (5)

Node Voltage Analysis – Voltage Divider

Step 8 – Solve the system of equations to determine values of unknown variables.

$$I_1 + I_3 = 0 \quad (1)$$
$$-I_1 + I_2 = 0 \quad (2)$$
$$R_1 I_1 - U_1 + U_2 = 0 \quad (3)$$
$$R_2 I_2 - U_2 = 0 \quad (4)$$
$$U_1 = V_S \quad (5)$$

$$A \cdot \vec{x} = \vec{b}$$

$$\begin{bmatrix} 1 & 0 & 1 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 \\ R_1 & 0 & 0 & -1 & 1 \\ 0 & R_2 & 0 & 0 & -1 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ U_1 \\ U_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ V_S \end{bmatrix}$$

$$I_1 = \frac{V_S}{R_1 + R_2}, \quad I_2 = \frac{V_S}{R_1 + R_2}, \quad I_3 = -\frac{V_S}{R_1 + R_2}$$

$$U_1 = V_S$$

$$U_2 = \frac{R_2}{R_1 + R_2} \cdot V_S$$

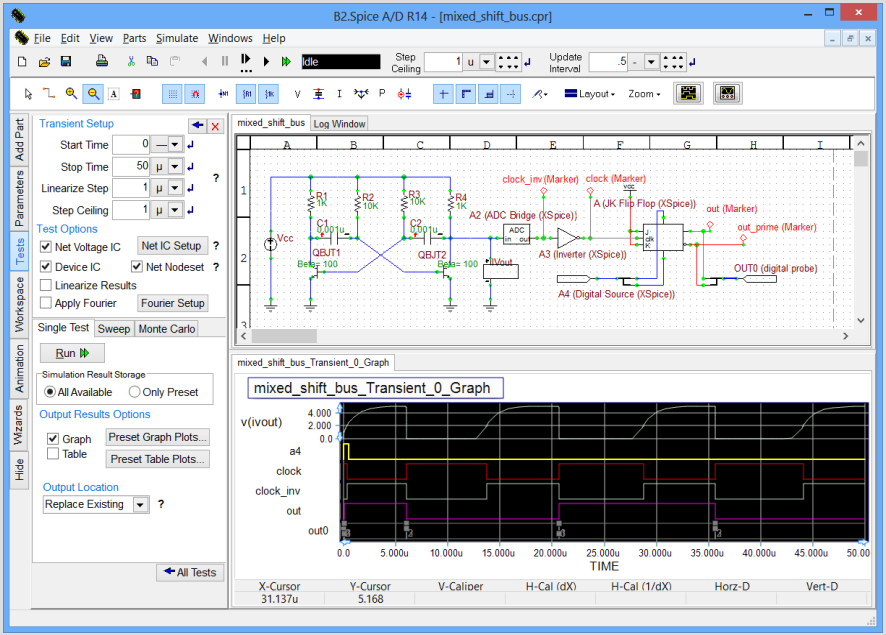
$\alpha < 1$

α is an operator

Electrical Circuit Analysis Algorithm (tool)

SPICE (Simulation Program with Integrated Circuit Emphasis): started as a student project at Berkeley!

Now the basis for open-source electronic circuit simulation, to design and model device characteristics and check circuit boards



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Electrical Circuit Analysis Algorithm (tool)