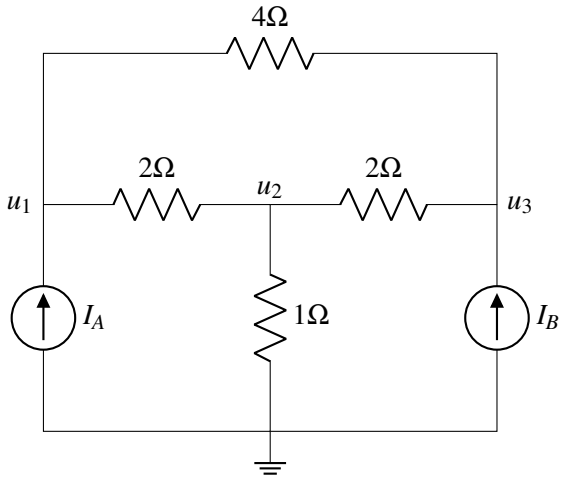
EECS 16A Designing Information Devices and Systems I
Spring 2023 Exam Prep 9A

1. Superposition (Fall 2020 Midterm 2 Question 7)

For this question, we will analyze the circuit shown below with the two current sources of strength I_A and I_B as inputs. It may be observed that the network of resistors shown in the circuit is symmetric. We will first solve this circuit for symmetric inputs $I_A = I_B$, and then for anti-symmetric inputs $I_A = -I_B$. Using these two results, we we will solve the circuit for arbitrary inputs I_A, I_B.



(a) Consider the circuit above with symmetric inputs, $I_A = I_B = 1\text{A}$. Using superposition, solve for the node voltages at the nodes marked u_1, u_2 and u_3.

(b) Consider the same circuit as before with anti-symmetric inputs, $I_A = 1\,\text{A}$ and $I_B = -1\,\text{A}$. Using superposition solve for the node voltages at the nodes marked u_1, u_2 and u_3.

(c) Now consider the same circuit, but this time with $I_A = 2\,\text{A}$ and $I_B = 2\,\text{A}$; in other words, we double the current sources from part (a). Here, as well as in the earlier circuits, the node voltages u_1, u_2 and u_3 can be represented by the vector $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$.

Assume that when $I_A = 1\,\text{A}$ and $I_B = 1\,\text{A}$ as part (a), the solution was given by $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \alpha \\ \beta \\ \alpha \end{bmatrix}$.

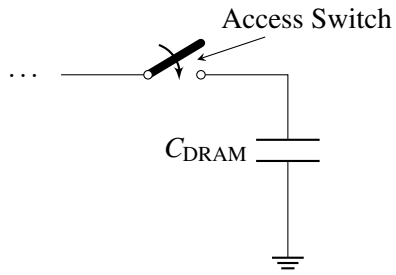
What are the new node voltages, $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$ when $I_A = 2\,\text{A}$ and $I_B = 2\,\text{A}$? Write your answer in terms of α and β. You do not need to use any of the work from parts (a) and (b) to solve this part.

(d) Assume that when $I_A = 1\,\text{A}$ and $I_B = 1\,\text{A}$ (also known as "common mode"), the node voltages were given by $\vec{u}_{cm} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \alpha \\ \beta \\ \alpha \end{bmatrix}$. Also, assume that when $I_A = 1\,\text{A}$ and $I_B = -1\,\text{A}$ (also known as "differential mode"), the node voltages were given by $\vec{u}_{dm} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \gamma \\ 0 \\ -\gamma \end{bmatrix}$.

Consider the same circuit as before, but now with current sources of strengths $I_A = 6\text{A}$ and $I_B = 2\text{A}$. Find the node voltages, $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$, in terms of α, β and γ. You do not need to use any of the work from parts (a) and (b) to solve this part. Show your work and justify your answer. You do not have to use to NVA to solve this part, there is an easier solution.

2. DRAM (Dynamic Random Access Memory) Cell (Fall 2020 Midterm 2 Question 8)

You are on a research team investigating the design of Dynamic Random Access Memory (DRAM) cells to improve their performance!

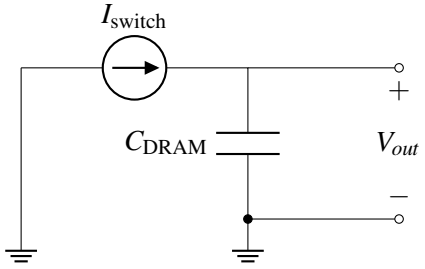


(a) You are making a capacitor with a new insulating material between the DRAM capacitor plates. The DRAM capacitor has the following properties:

- C_{DRAM} plate area, $A = 1\,\mu\text{m} \times 10\,\mu\text{m} = 10^{-11}\text{m}^2$,
- Distance between C_{DRAM} plates, $d = 40\,\text{nm} = 4 \times 10^{-8}\text{m}$,
- Permittivity of the material between the C_{DRAM} plates, $\varepsilon = 40\varepsilon_0$ F/m, where ε_0 is the permittivity of free space.

What is the capacitance of a DRAM capacitor, C_{DRAM}, in terms of ε_0 and other numerical values. You do not need to substitute the value of ε_0.

(b) Now let's consider the case in the figure below, which is the setup after the switch in Figure is closed at time $t = 0$. When the switch is closed it starts conducting a current I_{switch}, as shown in Figure (b).
Assume that C_{DRAM} has no charge stored on it at $t = 0$ seconds, i.e. it has no initial charge. Let $I_{\text{switch}} = 90\,\text{pA} = 9 \times 10^{-11}\text{A}$, and $C_{\text{DRAM}} = 90\,\text{fF} = 9 \times 10^{-14}\text{F}$.
Find the value of V_{out} at $t = 1\,\text{ms} = 10^{-3}\text{s}$.



(c) Unfortunately, in reality, our access switch is not ideal and has a *parasitic capacitance* C_{switch}, which gets added to the circuit when the switch is closed. C_{switch} affects the DRAM write speed, i.e. how fast C_{DRAM} can be charged.

Find rate of change of V_{out}, i.e. $\frac{dV_{out}}{dt}$, as a function of C_{DRAM}, C_{switch} and I_{switch} for both (i) the ideal circuit circuit without C_{switch}, as shown in the left side of Figure 1 and (ii) the non-ideal circuit circuit with C_{switch}, as shown in the right side of Figure 1.

Then compare $\frac{dV_{out}}{dt}$ values for both circuits. A larger $\frac{dV_{out}}{dt}$ means faster write speed.

Which circuit has faster write speed? Justify your answer.

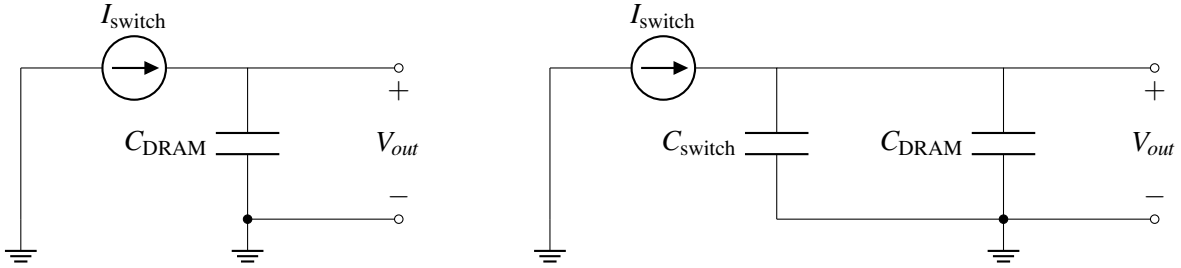
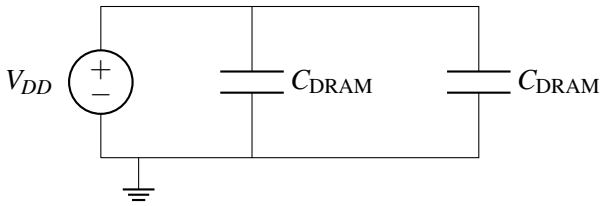


Figure 1: Left: Circuit without parasitic capacitance. Right: Circuit with parasitic capacitance.

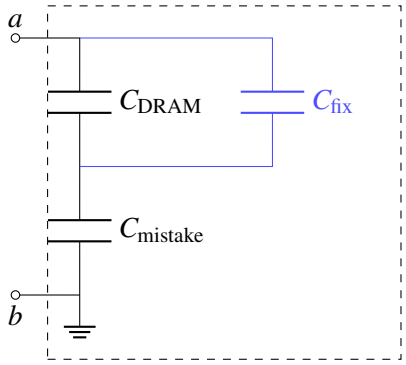
(d) Assume you want to build an array of DRAM capacitors. You start by connecting two DRAM capacitors in parallel and charging them with a voltage source with value V_{DD}, as shown in the figure below. Each DRAM capacitor has a capacitance value of C_{DRAM}.



When the capacitors are charged, how much total energy is going to be stored in both DRAM capacitors together? Your answer should be a function of C_{DRAM} and V_{DD}.

(e) Finally! You make it to the lab! Unfortunately, you accidentally wind up introducing an additional capacitive component, C_{mistake}.

Before your grad student mentor finds out your mistake, you'd like to quickly add an additional capacitor C_{fix}, as shown in the figure below, so that the equivalent capacitance between nodes a and b becomes the same as C_{DRAM}.



Find the expression for C_{fix} so that the equivalent capacitance between nodes a and b is C_{DRAM}. Assume $C_{\text{mistake}} > C_{\text{DRAM}}$. Your answer should be in terms of C_{DRAM} and C_{mistake}.