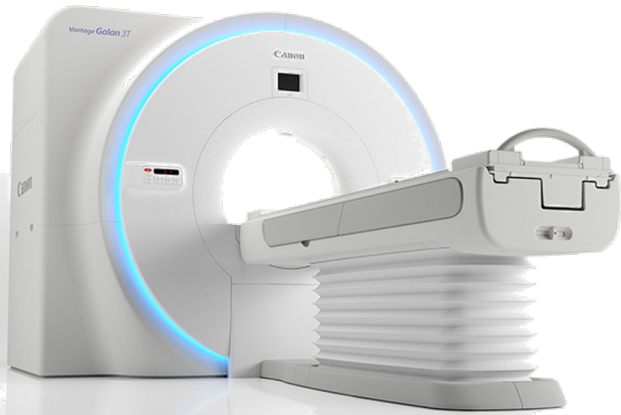
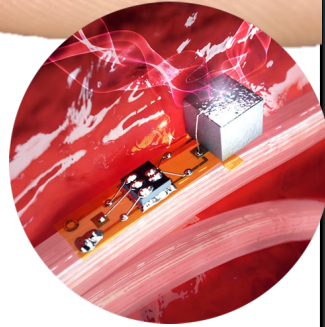
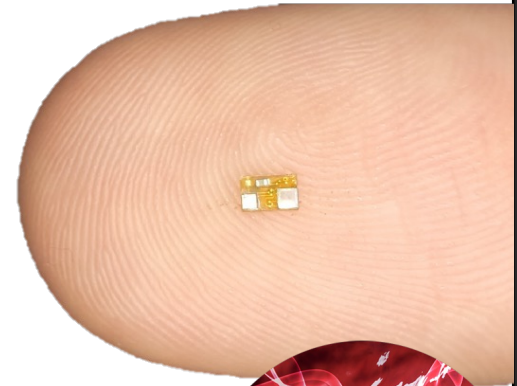


Welcome to EECS 16A!

Designing Information Devices and Systems I

Prof. Laura Waller
Prof. Rikky Muller
Spring 2023





**all of these extract information from
the real world and interact with it;**

**we will learn how to design and
analyze such devices and systems**



Instructors



Prof. Laura Waller
waller@berkeley.edu



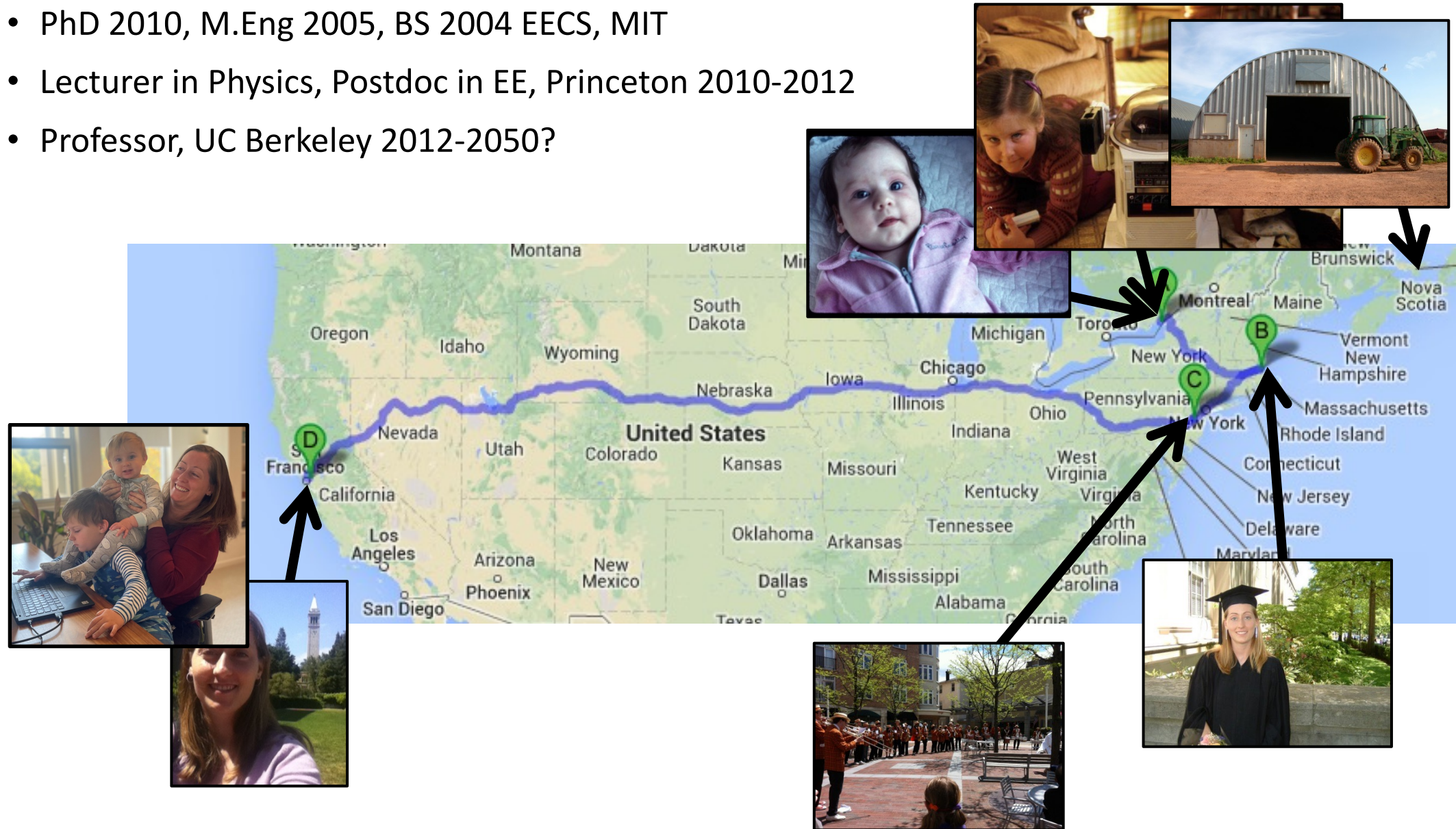
Prof. Rikky Muller
rikky@berkeley.edu

**Office Hours: 11am Wednesdays, Cory Hall room 504
(starts next week)**

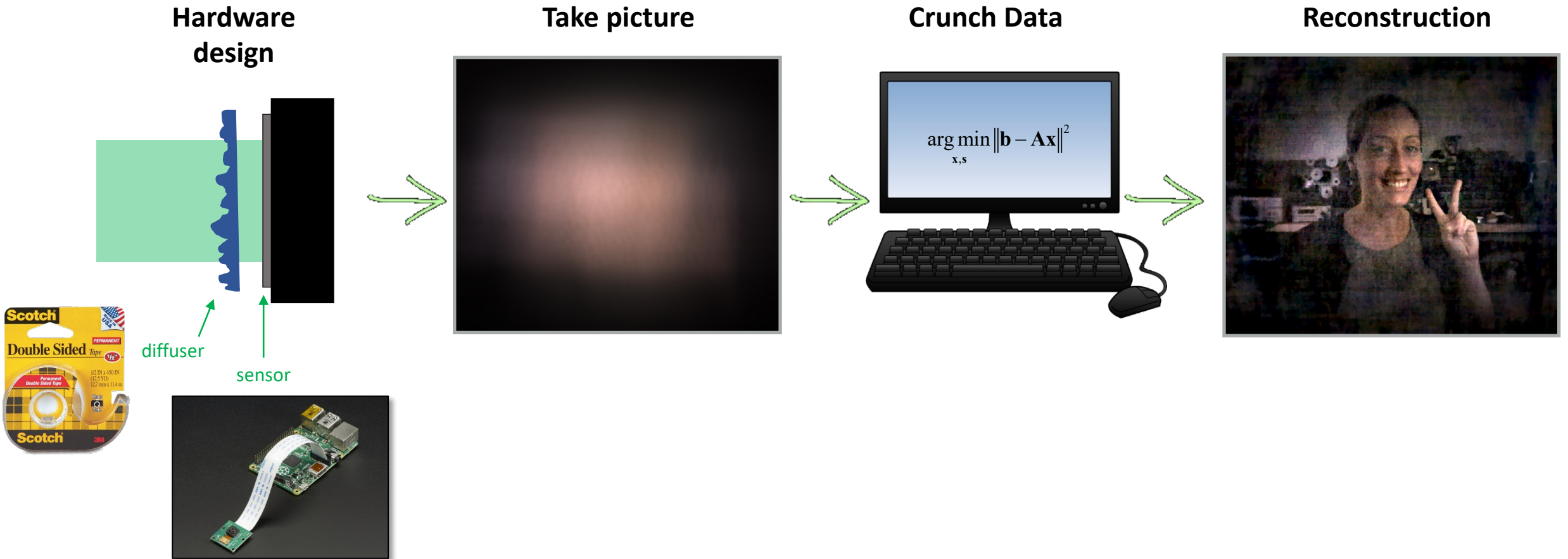
- Other contributors to 16: Vladimir Stojanovic, Anant Sahai, Gireeja Ranade, Ali Niknejad, Claire Tomlin, Michel Maharbiz, Miki Lustig, Vivek Subramanian, Thomas Courtade, Babak Ayazifar, Ana Arias

Laura: About me

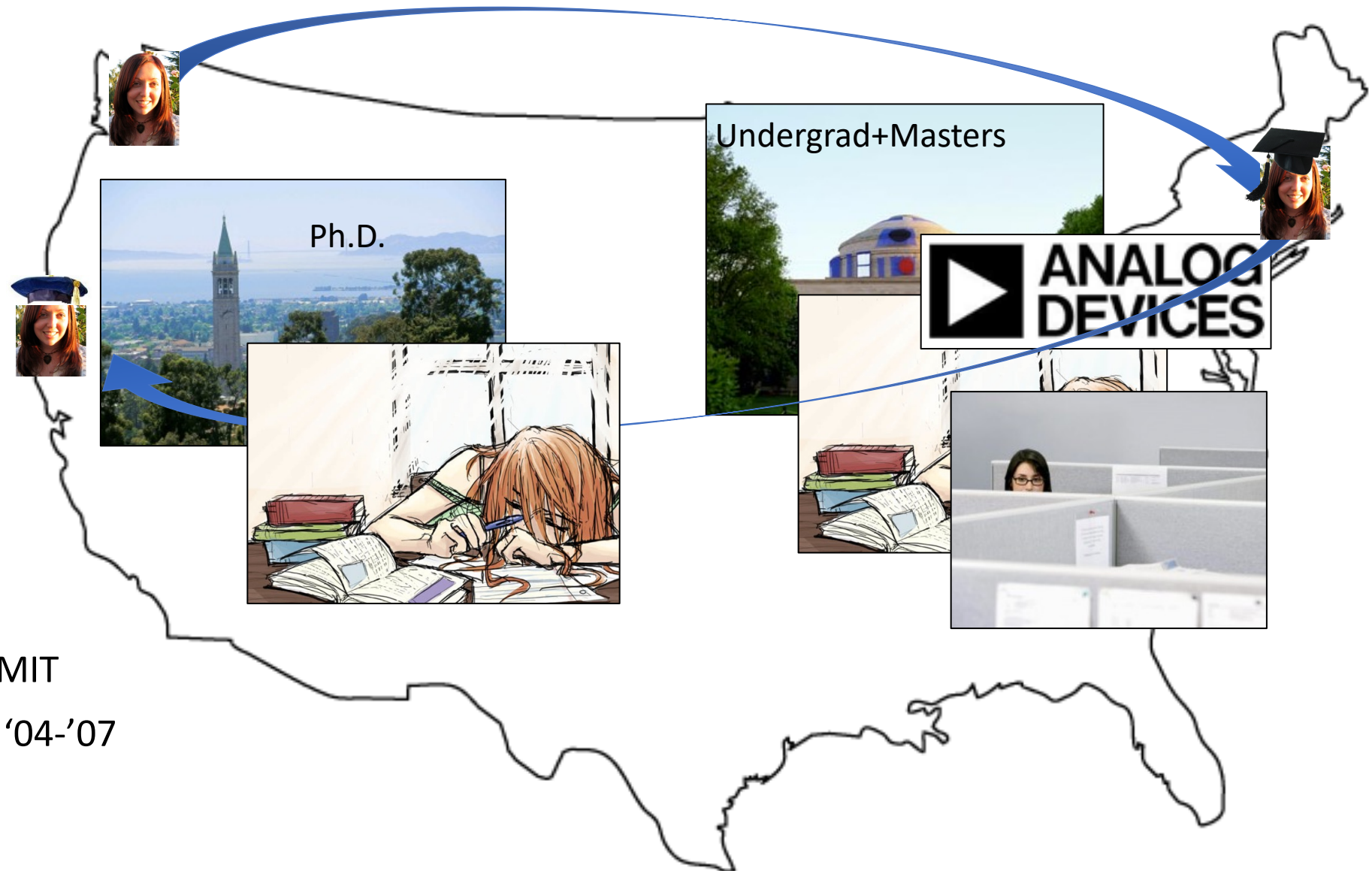
- PhD 2010, M.Eng 2005, BS 2004 EECS, MIT
- Lecturer in Physics, Postdoc in EE, Princeton 2010-2012
- Professor, UC Berkeley 2012-2050?



Laura: Research in Computational Imaging



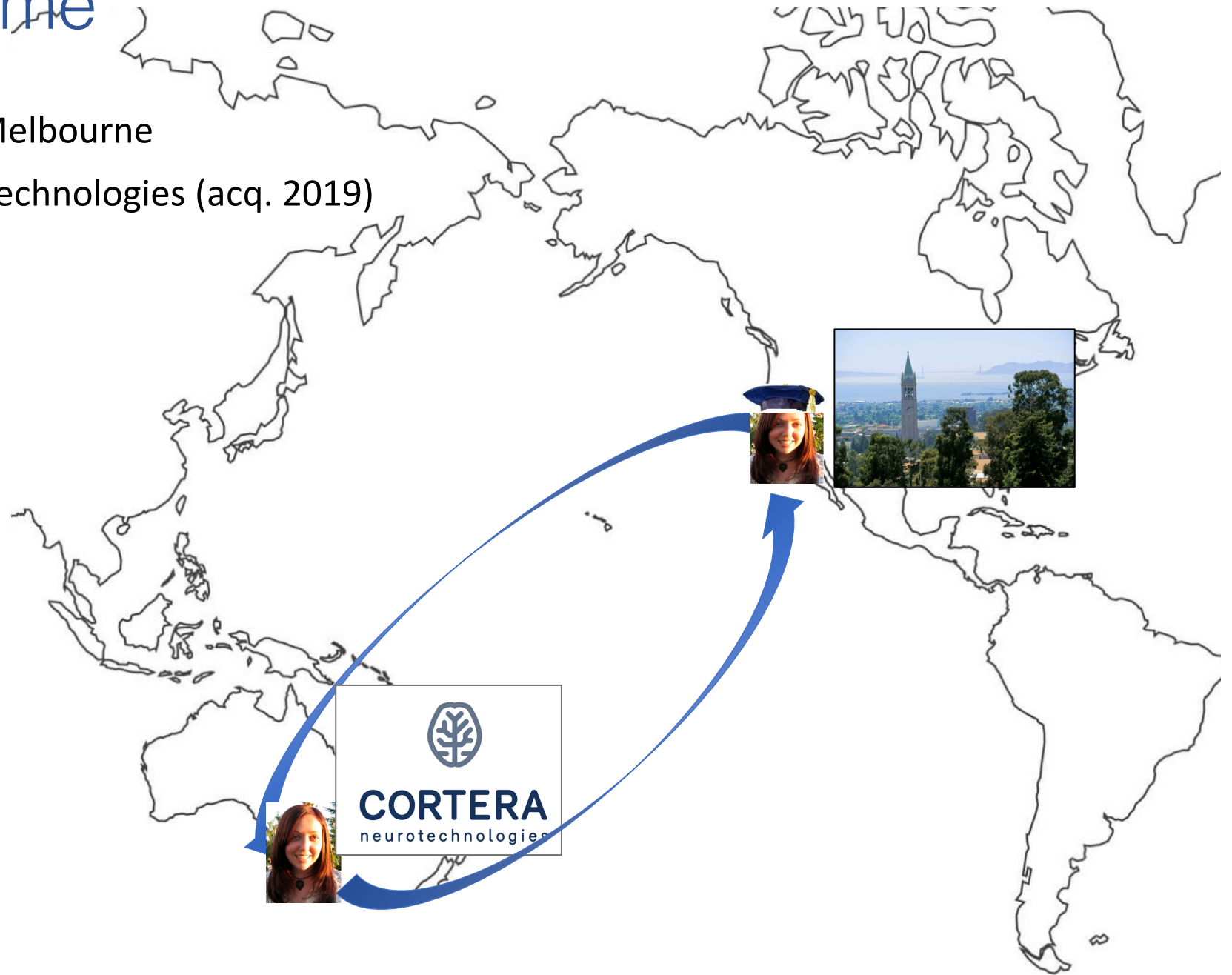
Rikky: About me



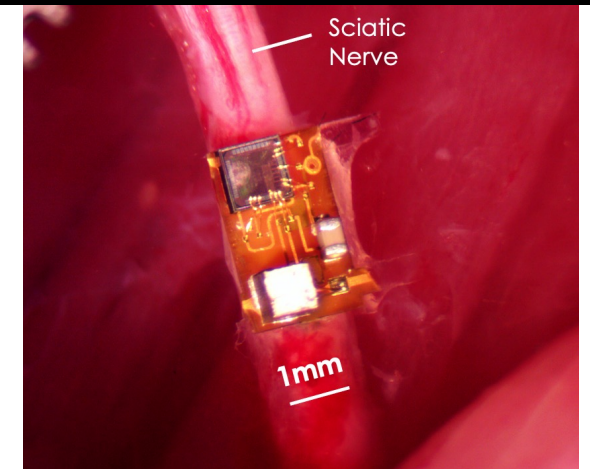
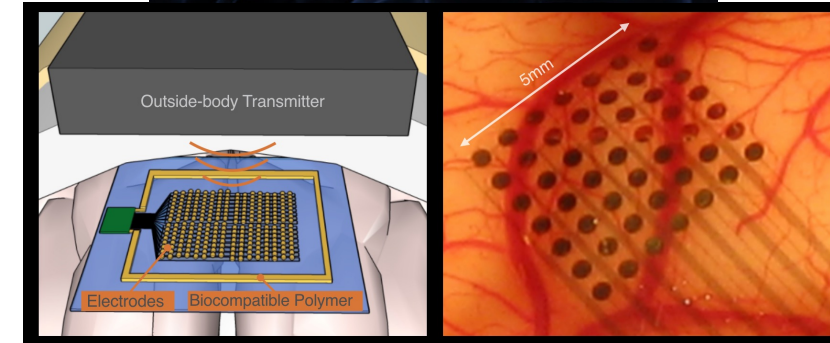
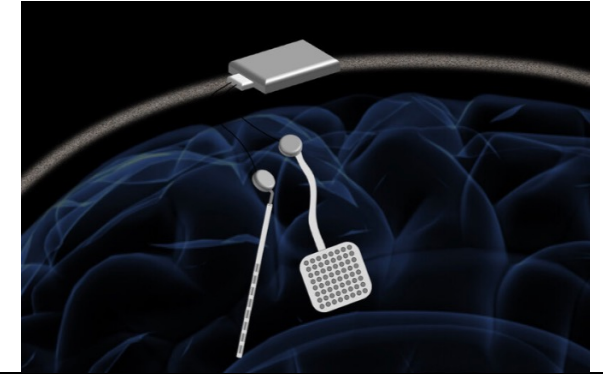
- M.Eng 2004, BS 2003 EECS, MIT
- IC Designer Analog Devices, '04-'07
- PhD 2013, UC Berkeley!

Rikky: About me

- Lecturer/Postdoc University of Melbourne
- Startup founder: Cortera Neurotechnologies (acq. 2019)
- Professor since 2016



Rikky: Research in Neurotechnology



Sources: Muller Lab Publications

Course Staff

Head GSIs



Aniruddh
Khanwale



Austin Patel

Head GSIs:

eeecs16a@Berkeley.edu

Email with:

Questions not for Ed,
conflicts, accommodations,
emergencies,
administrative questions



Course Staff

Head GSIs



Aniruddh
Khanwale



Austin Patel

Head Lab GSIs



Anastasia
Simonova



Shreyash
Iyengar

Head GSIs:

eeecs16a@Berkeley.edu

Email with:

Questions not for Ed,
conflicts, accommodations,
emergencies,
administrative questions



Krystle Simon

Course manager

Great resource for 1-1 concerns
Krystle@eeecs.Berkeley.edu

Course Staff

Head GSIs



Aniruddh
Khanwale

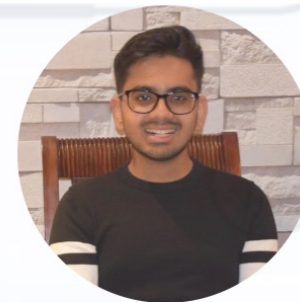


Austin Patel

Head Lab GSIs



Anastasia
Simonova



Shreyash
Iyengar



Click to Toggle Bio!

Ayah Ahmad
HW/Dis

eeecs16a.homework@
ayahahmad@



Click to Toggle Bio!

Dahlia Saba
Dis

she/they
dahliasaba@



Click to Toggle Bio!

Shuming Xu
Lab

he/him/his
smxu@



Click to Toggle Bio!

Joyce Zhu
Lab

she/her/hers
jzhu0226@



Click to Toggle Bio!

Carol Li
Lab

she/her/hers
carol.li@



Click to Toggle Bio!

Kanav Mittal
Dis/Software

he/him/his
kanavmittal@



Click to Toggle Bio!

Vivian Wu
Dis

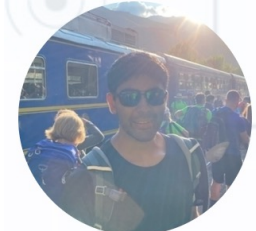
she/her/hers
vivianwuc25@



Click to Toggle Bio!

Anvitha Kachinthaya
Dis

she/her/hers
anvitha@



Click to Toggle Bio!

Ayush Pancholy
Lab

he/him/his
ayush.pancholy@



Click to Toggle Bio!

Jared Cheng
Lab

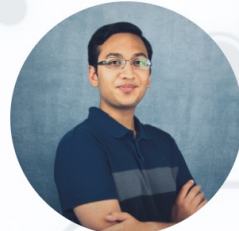
he/him/his
jaredcheng@



Click to Toggle Bio!

Anish Dhanashekar
Dis/Content

he/him/his
aeroanish@



Click to Toggle Bio!

Avikam Chauhan
Dis

he/him/his
avikam@



Click to Toggle Bio!

Amit Kohli
Content

he/him/his
apkohli@



Click to Toggle Bio!

Tiffany Chien
Dis/Content

she/her/hers
tiffany_chien@



Click to Toggle Bio!

Youbin Kim
Dis/Content

he/him/his
youbin_kim@



Click to Toggle Bio!

Nathan Brooks
Dis/Content

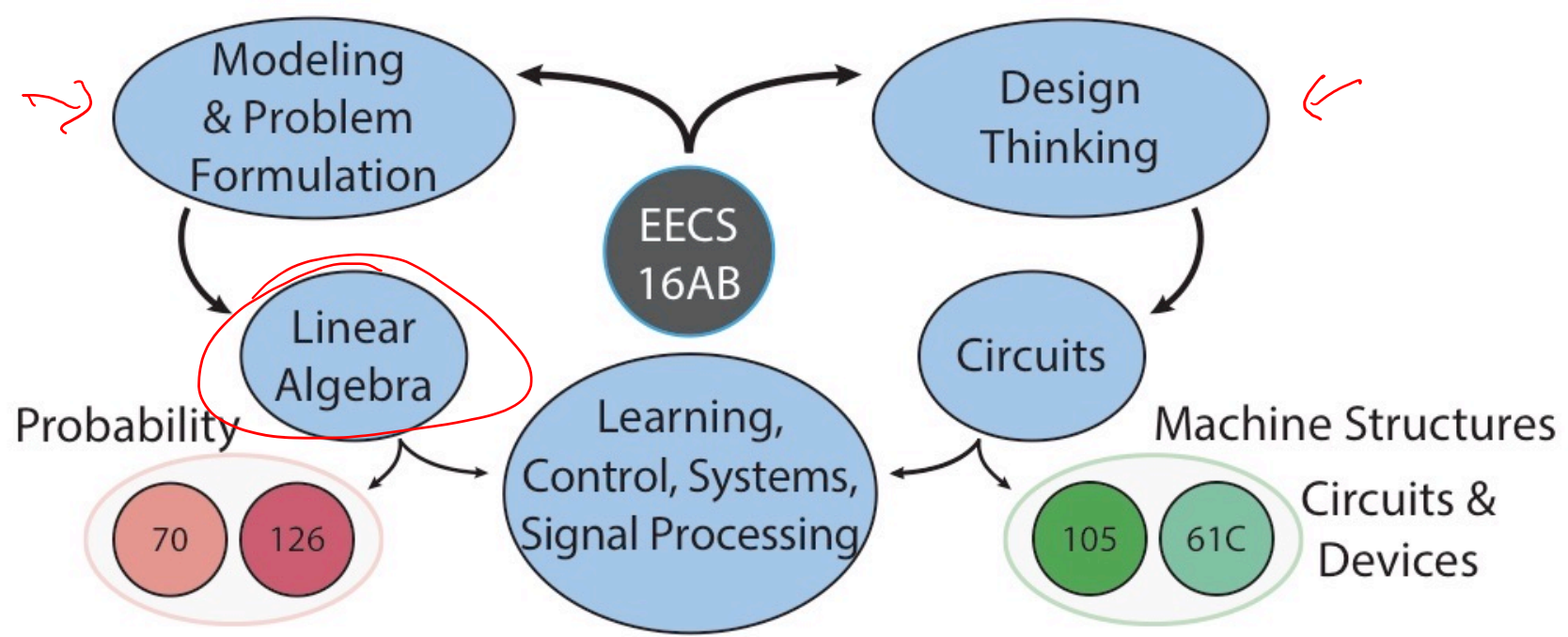
he/him/his
nathanbrooks@

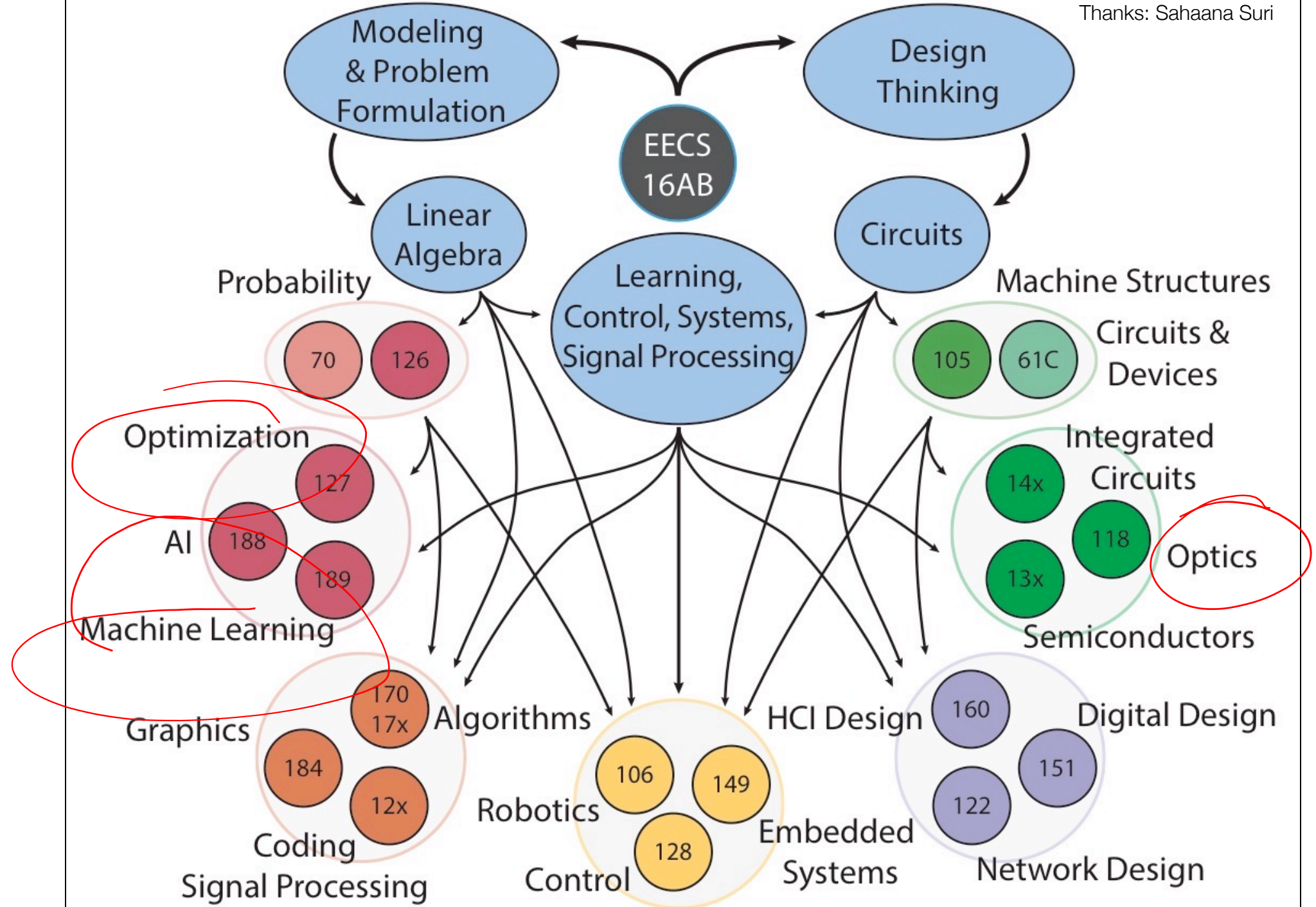


Pathway to becoming like us!

- if you do well in class — you can apply to:
 - Become an ASE
 - Grade homework, assist in labs, tutor and help with office hours
 - Become a uGSI
 - Lab / Discussion / content
 - Become head TA...
 - Go to grad school, get a PhD
 - Become faculty
 - Teach 16A!







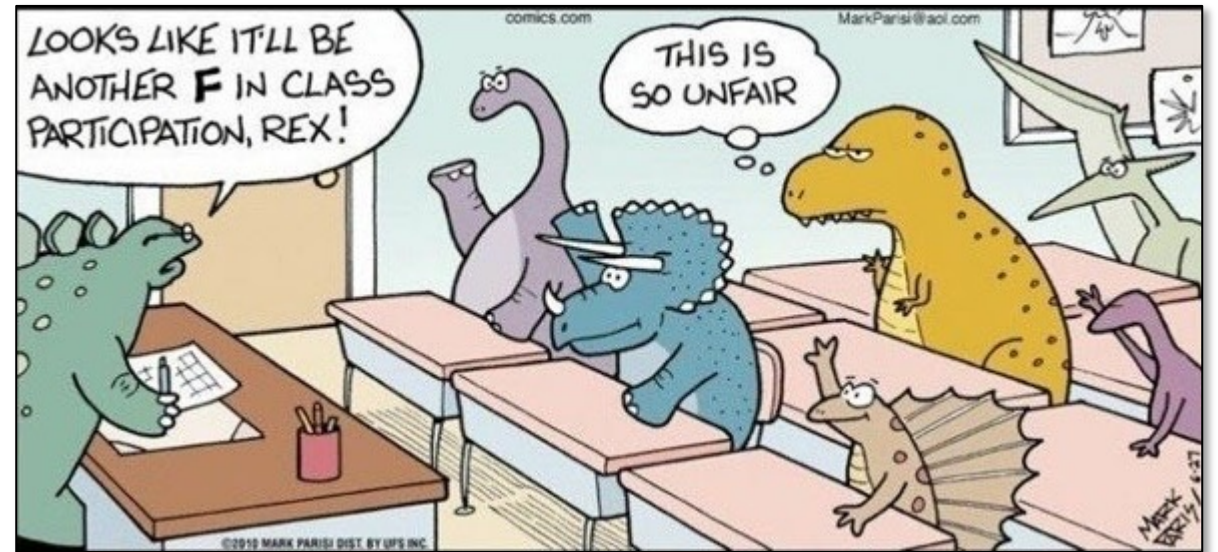
Course policies

- Syllabus is on the course website: <https://eecs16a.org/>
 - You are responsible for reading and following all course policies listed
- Ed: edstem.org
 - a resource for you to help each other out
- Questions? Ask eecs16a@berkeley.edu

Grading Policies

- Midterm 1, Midterm 2 (55 points each)
- Final (100 points)
- Lab – mandatory (55 points)*
- Homework (35 points)

- Exam second-chance policy based on optional Midterm Redo



*signup instructions coming tomorrow on Ed

Homework (HW)

- Due Fridays at 11:59pm
- HW Party: Fri 9-11am in 'the Woz'
- Office Hours: see course calendar
- HW0 due Friday
- You grade, we check!
 - Self-grades due the next Friday
 - 2 HW drops, 6 'slip days'

Note: Self-grading is not just about us being lazy!!
(it is also to help you learn)



Academic Honesty

We treat all our students with utmost trust and respect and expect students to return the same trust and respect. We will have **zero-tolerance** for academic dishonesty. **No excuses or special circumstances will be considered.**

Always seek help, never cheat.

You are here to learn!

- Learning can be hard and fun
- Collaborate and build community on Ed/HW Party/Study Groups
- Encourage different perspectives – this is Berkeley!
- Everyone here is smart
 - Students have different backgrounds
 - (some) Professors make mistakes – feedback helps
 - If you are struggling, ask for help!



How to succeed in 16A

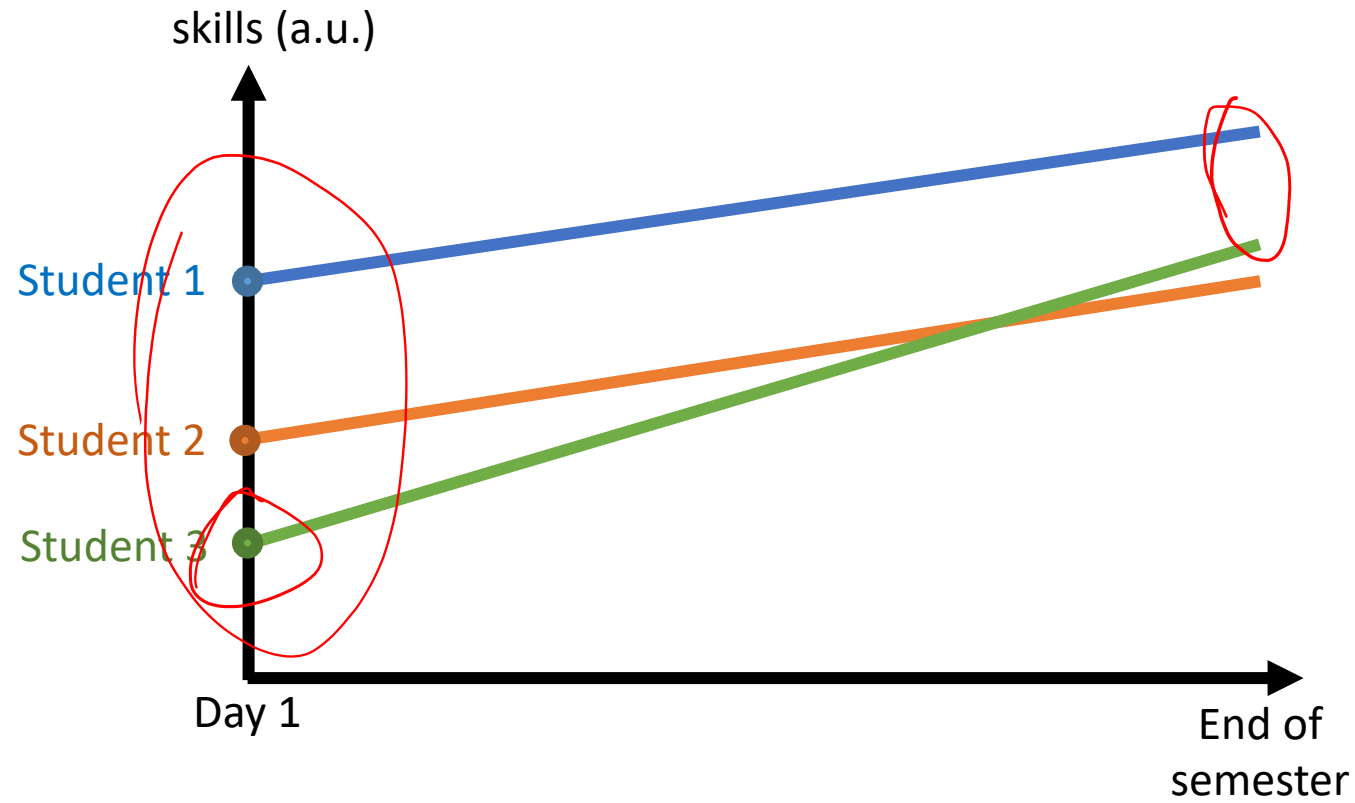
- Get enough sleep
- Attend lecture and discussion
- Do not do the above two at same time
- Actively read notes
- Try HW on your own, early
- Discuss problems with study group and/or at HW Party
- Study with others as well as alone
- Seek and offer help

study

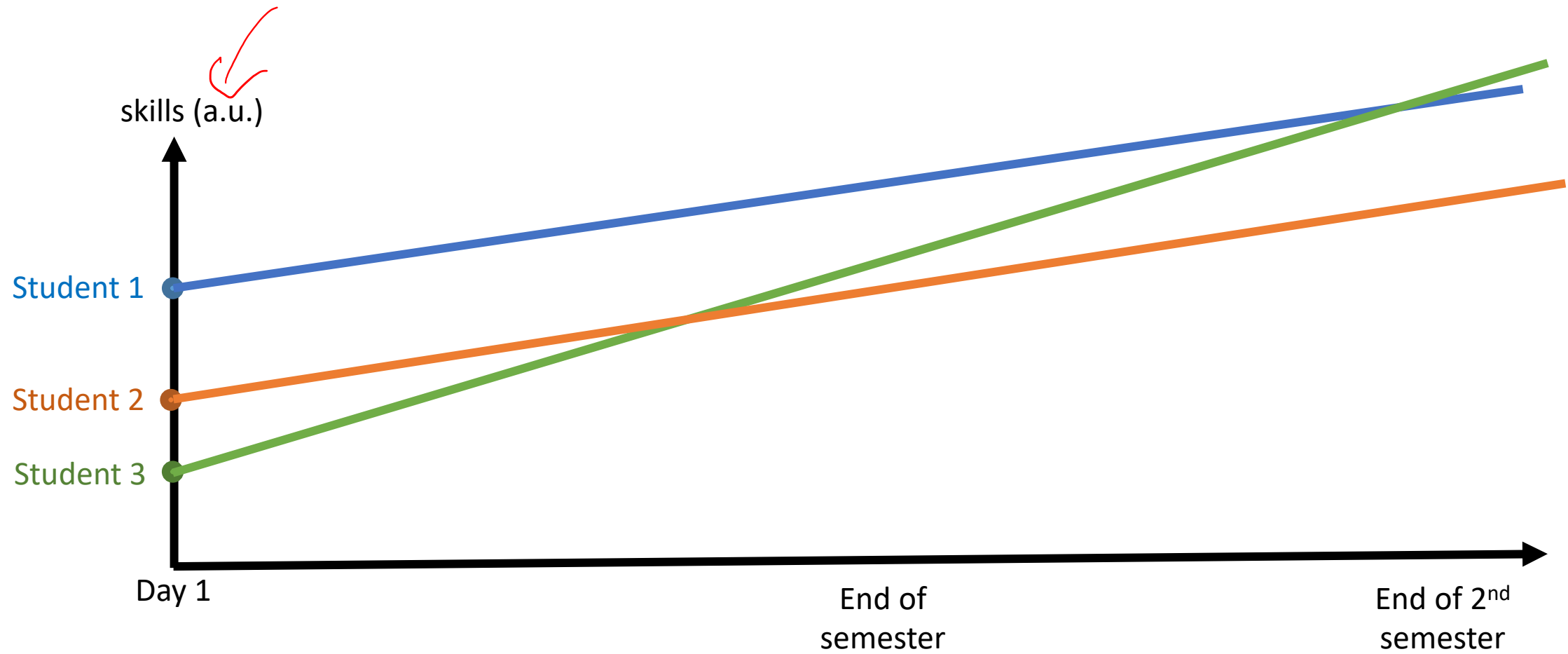
(verb)

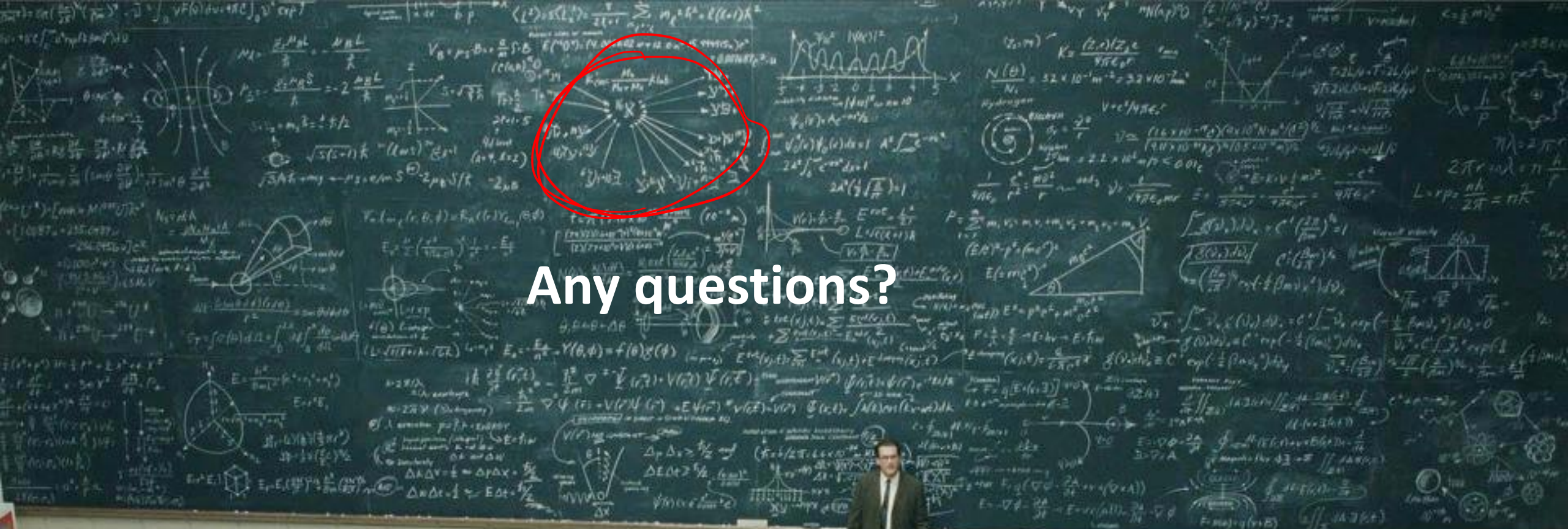
The act of texting, eating
and watching TV with an
open textbook nearby.

Slope is more important than intercept



Slope is more important than intercept



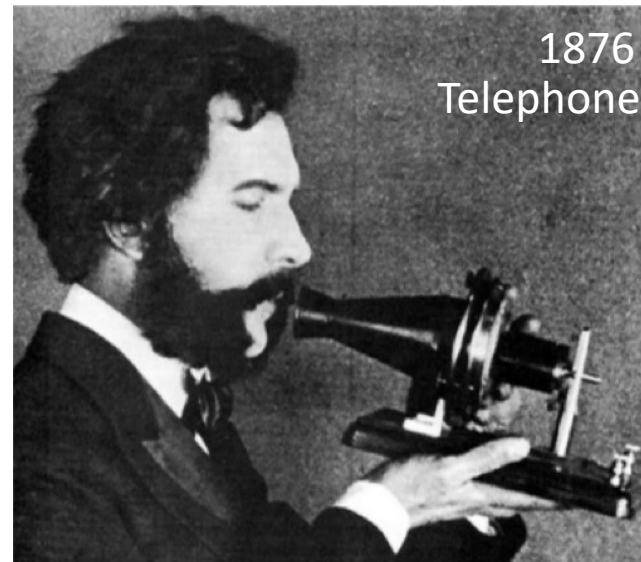


Any questions?



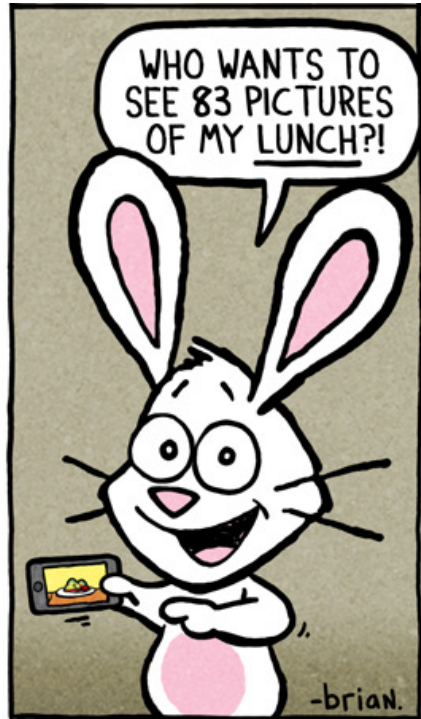


How did we get from this...



Flight of the Conchords S01E03 (HBO)

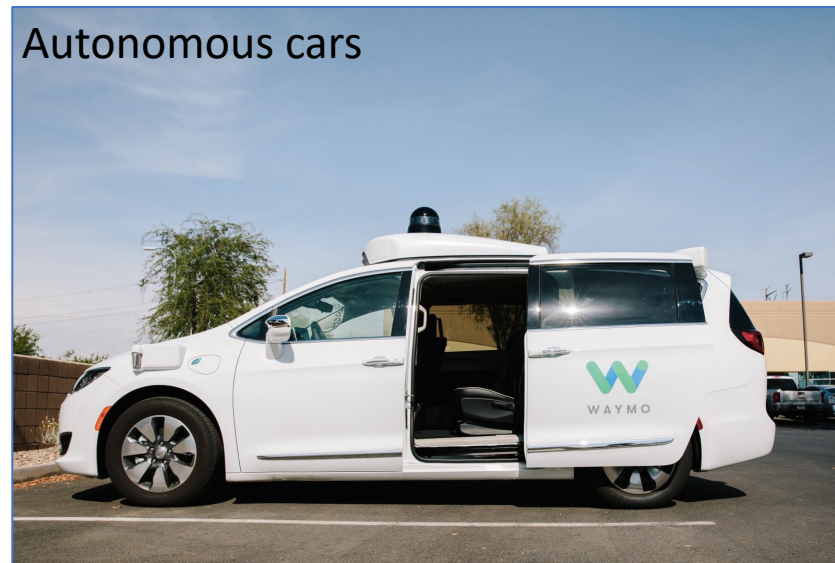
To this...



BEANS FACEBOOK.COM/SHOEBOXBLOG

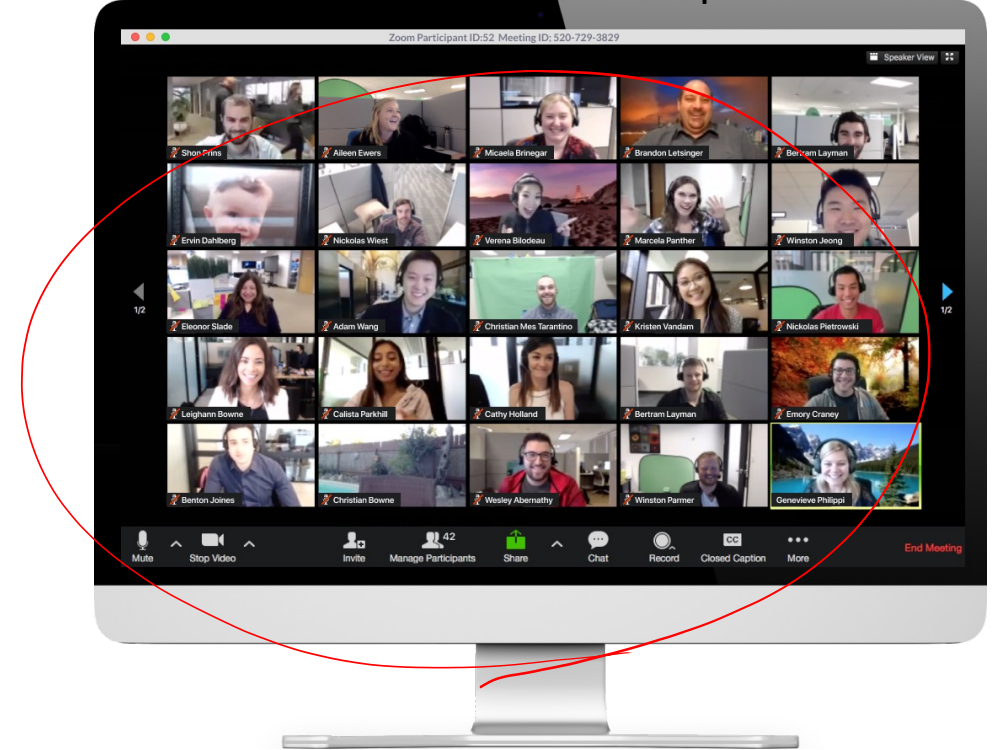


Drone delivery

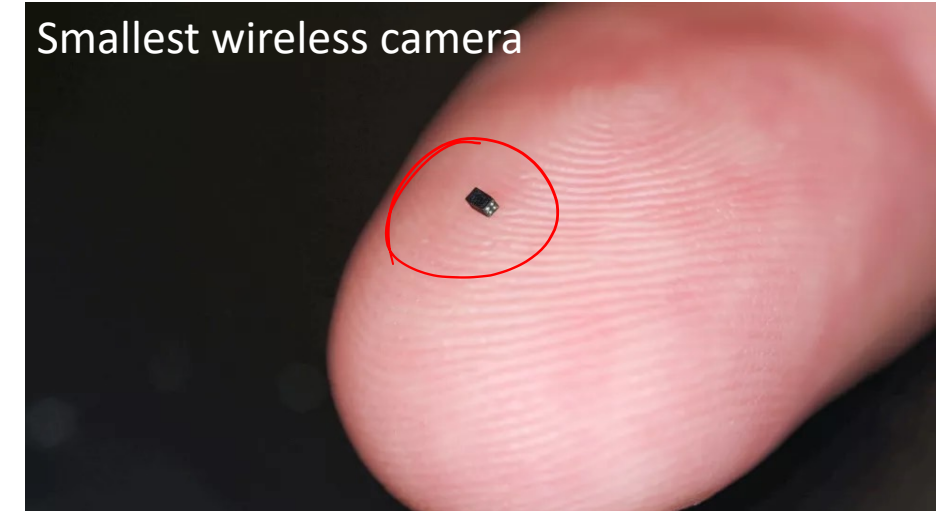


Autonomous cars

A 1000 student class on a computer screen



Smallest wireless camera



Learning Goals

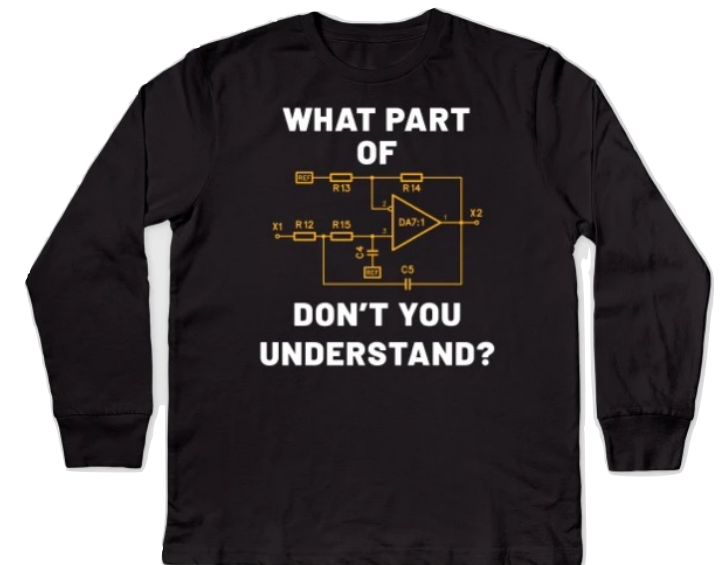
To help you understand many nerd jokes:

EECS 16A

- Module 1: Introduction to linear systems
- Module 2: Introduction to circuits and design
- Module 3: Introduction Signal Processing and Machine Learning

EECS 16B

- Module 4: Advanced circuit design / analysis
- Module 5: Introduction to control and robotics
- Module 6: Introduction to data analysis and signal processing



In the Lab



Imaging Module

- photodiodes
- systems of linear equations
- matrix analysis



Touchscreen Module

- resistance
- capacitance
- circuit analysis

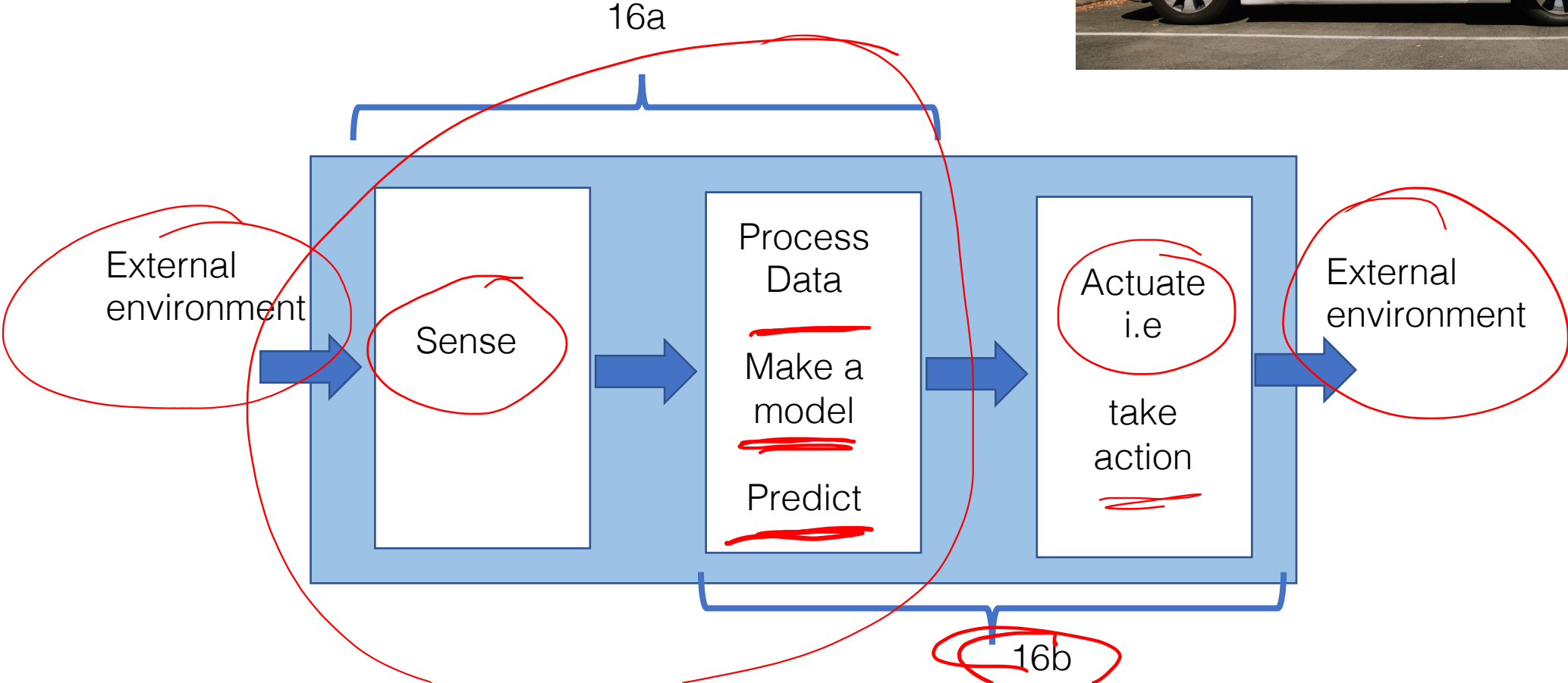


Acoustic Positioning Module

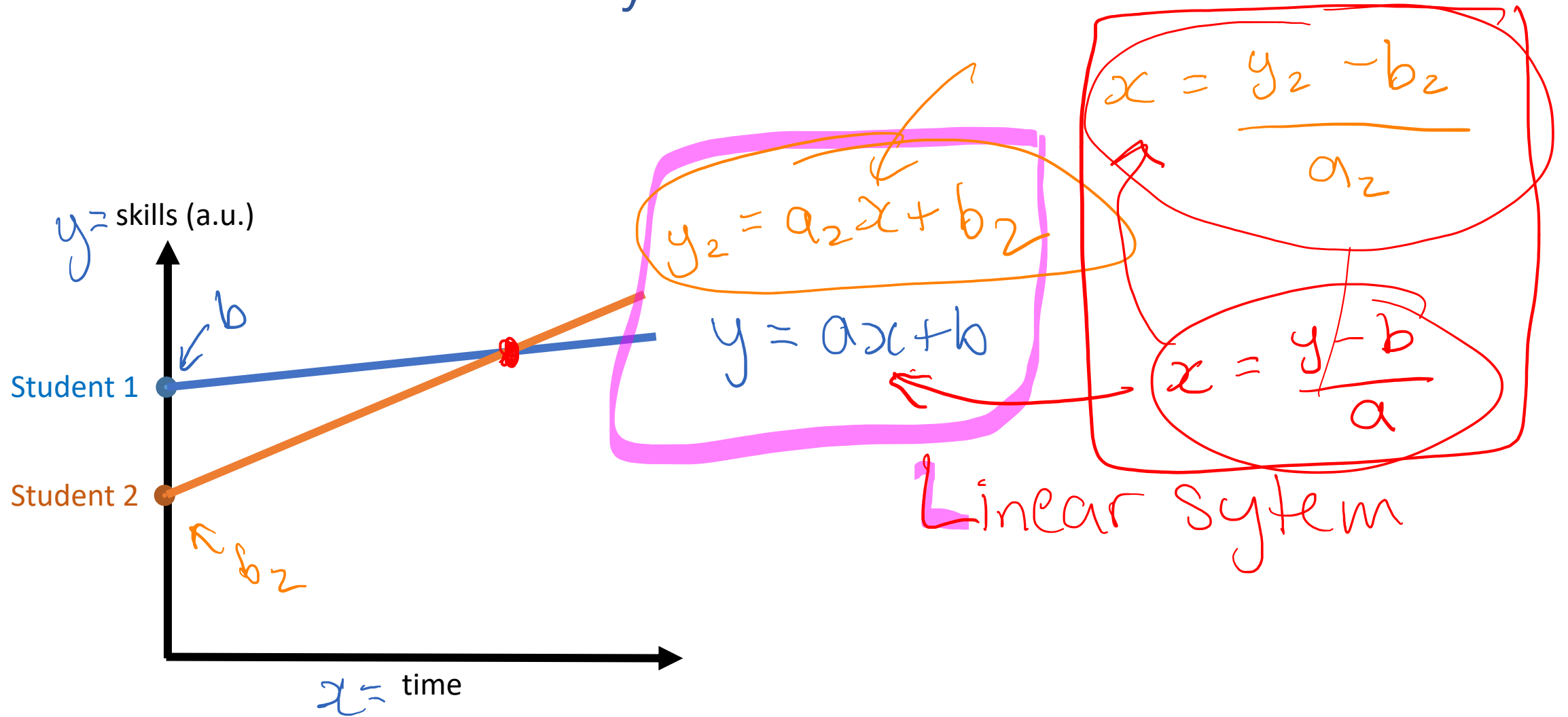
- cross-correlation
- optimization



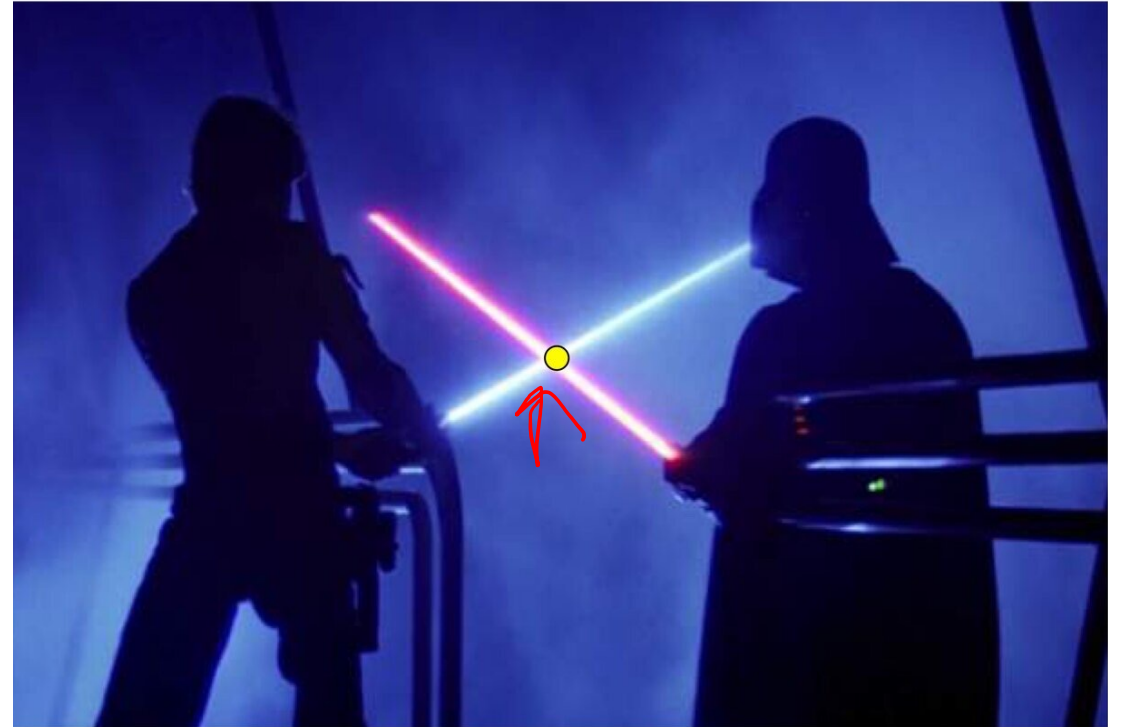
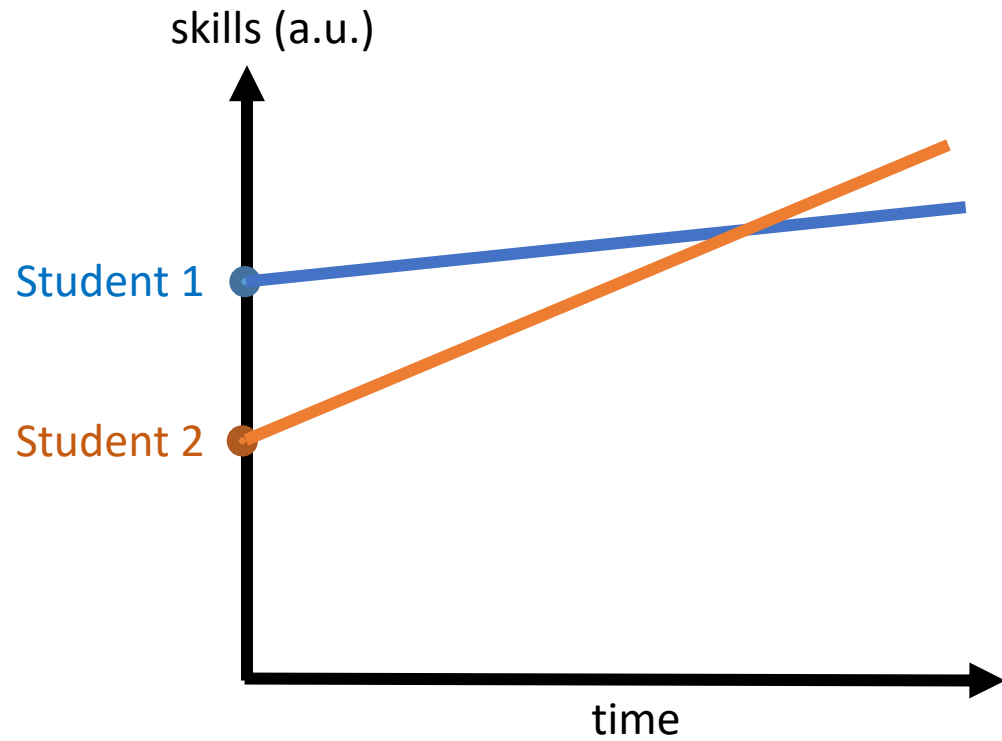
Systems thinking example: self-driving cars



What is a Linear System?



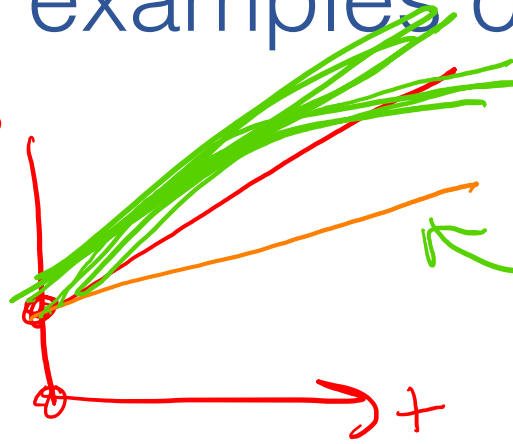
How do we solve linear systems of equations?



What are some examples of linear systems?

- race

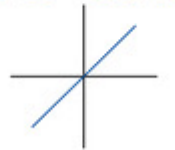
pos



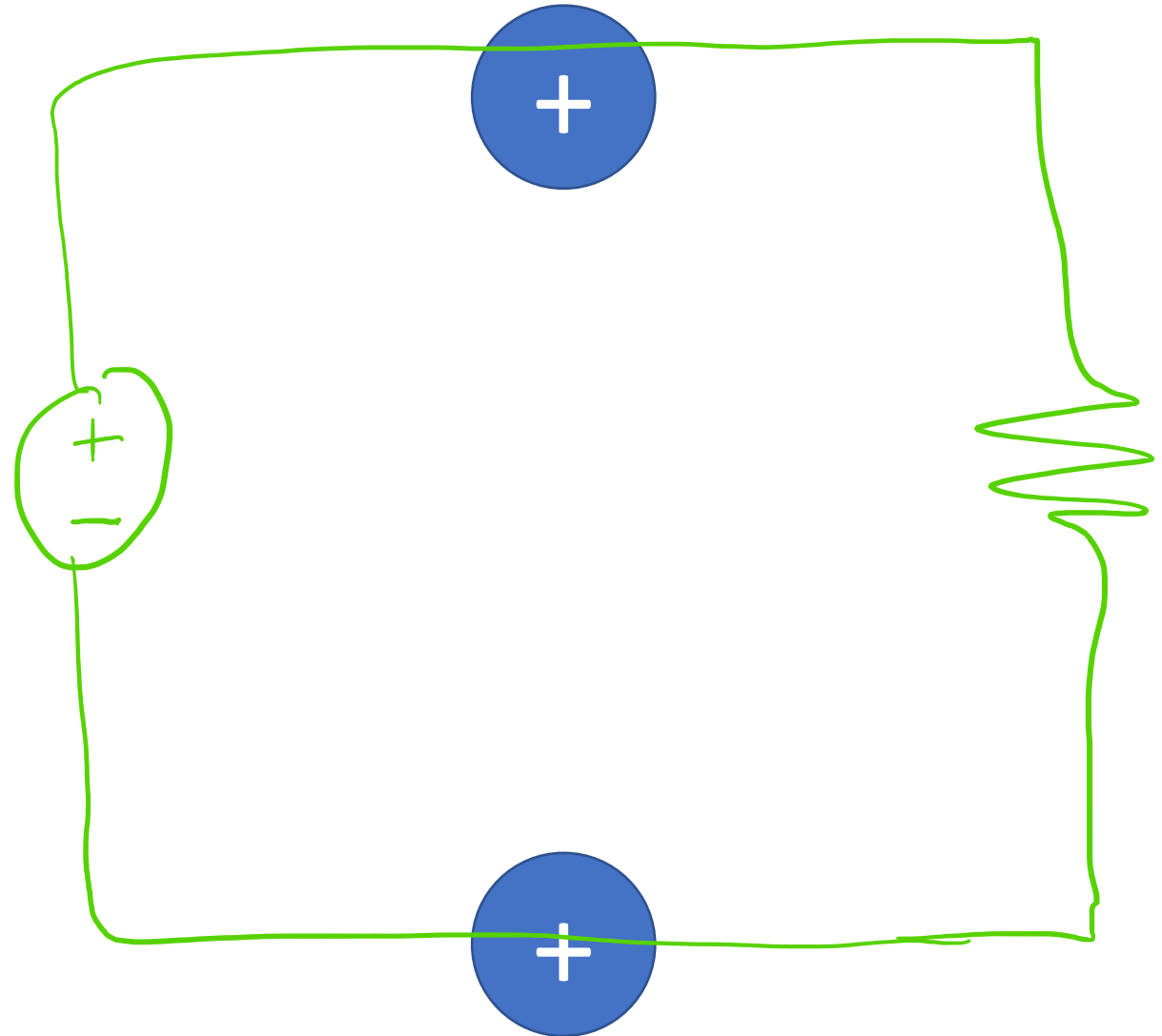
$$\text{pos} = at + s$$

$$y = ax + b$$

V = IR
is my
favorite
one-liner



Electronic Devices Depend on the Movement of Charge

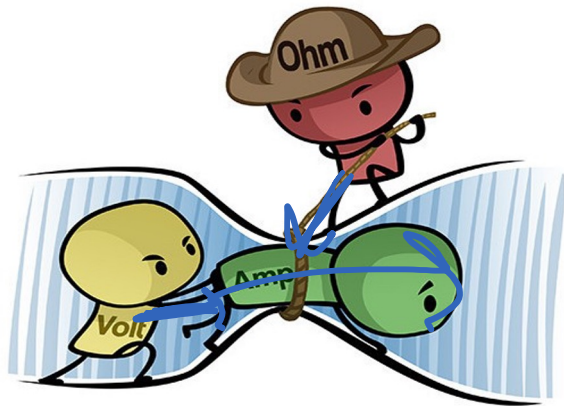


Electrical Quantities

$$V = IR$$

Ohm's Law

Quantities	Analytical Symbol	Units
Current	I	Amperes (A)
Voltage	V	Volts (V)
Resistance	R	Ohms (Ω)

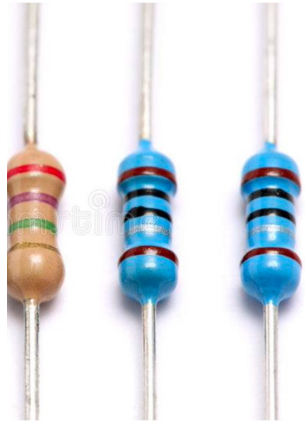


$I \rightarrow$ flows through an element

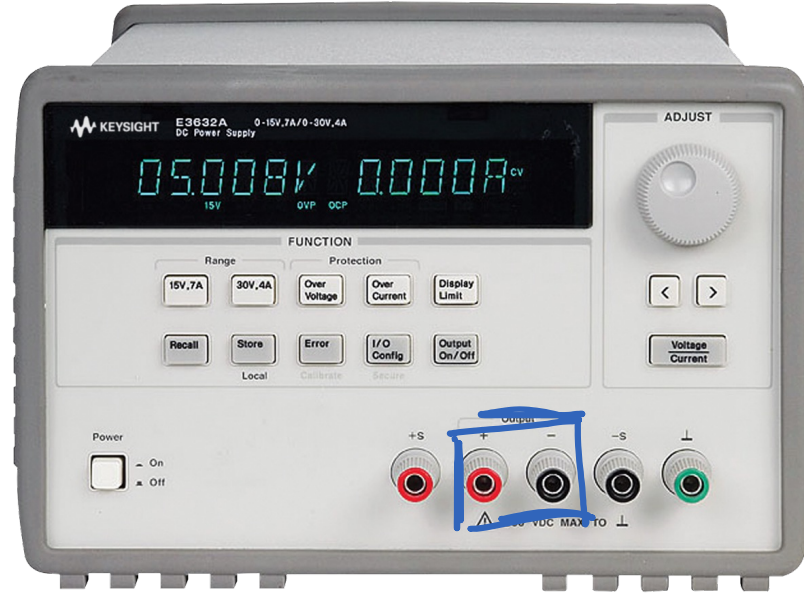
$V \rightarrow$ force applied across the element

$R \rightarrow$ opposition to current flow

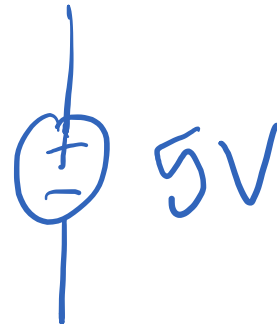
In the Lab!



resistor



voltage source

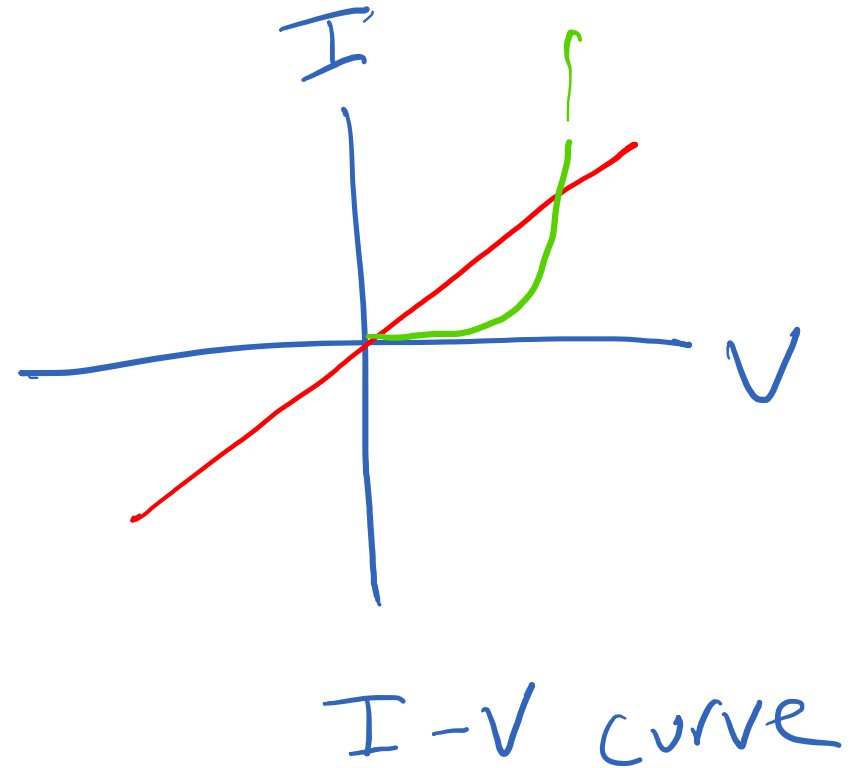
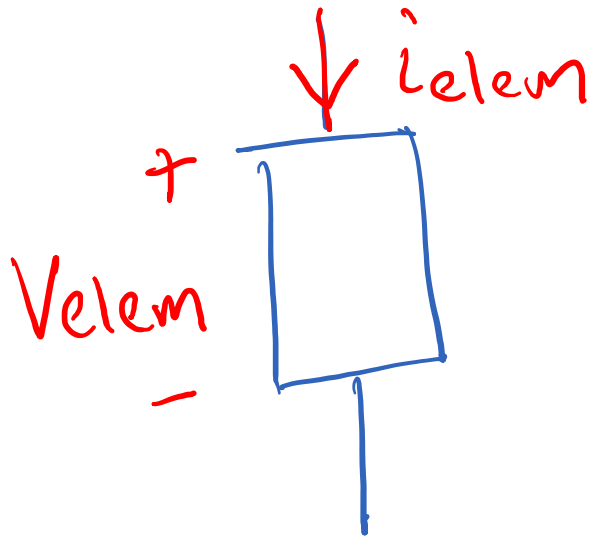


wire



Circuit Diagram Elements

Each element has some voltage across it and some current through it

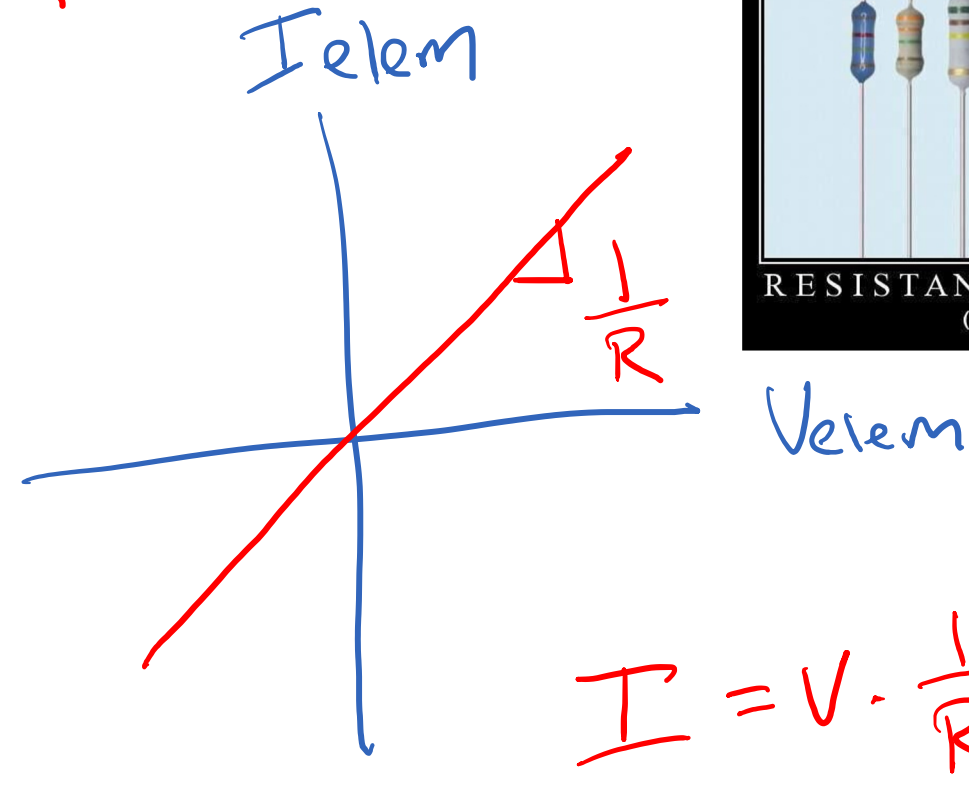
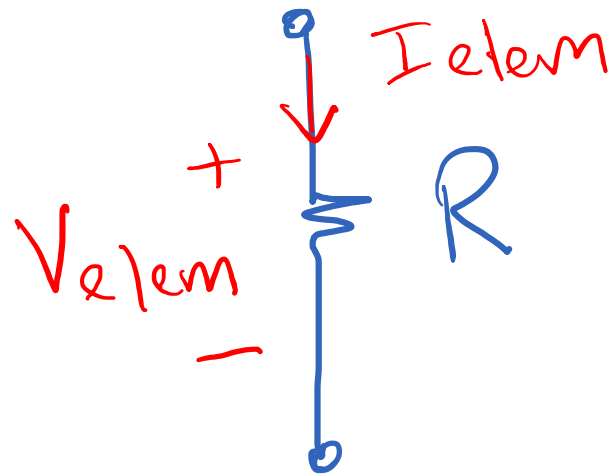


V_{elem} : Voltage across element

i_{elem} : Current through element

Key circuit elements: Resistor

$$V = IR$$

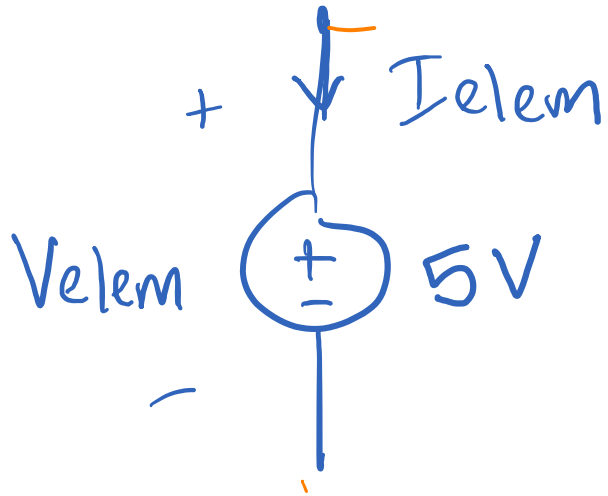


$$I = V \cdot \frac{1}{R}$$

$$V_{elem} = R \cdot I_{elem}$$



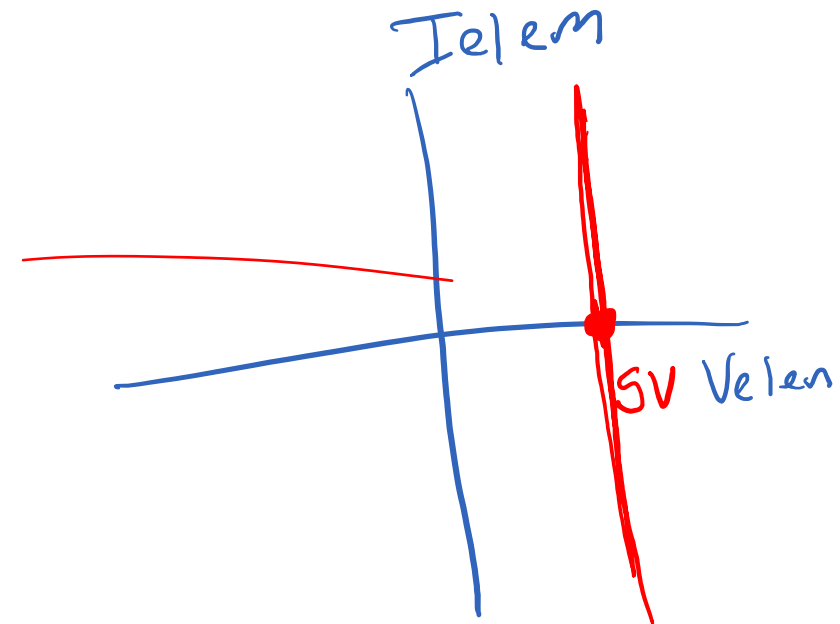
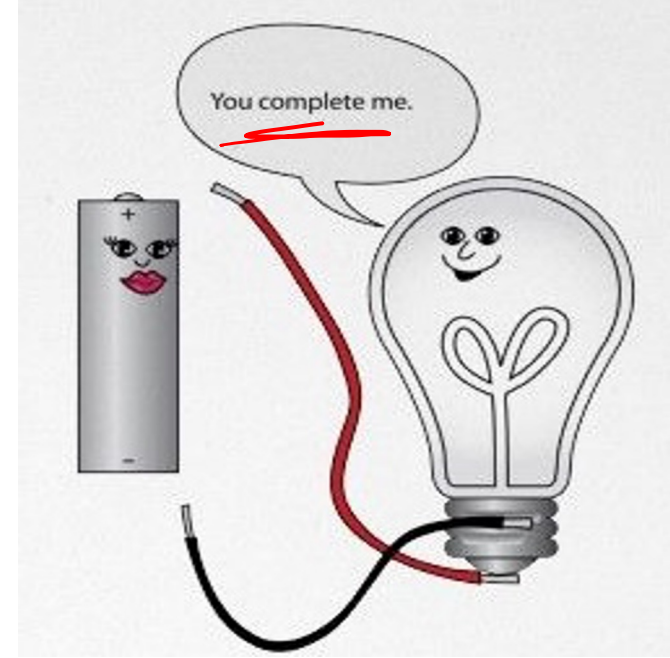
Key circuit elements: Voltage Source



$$V_{elem} = 5V$$

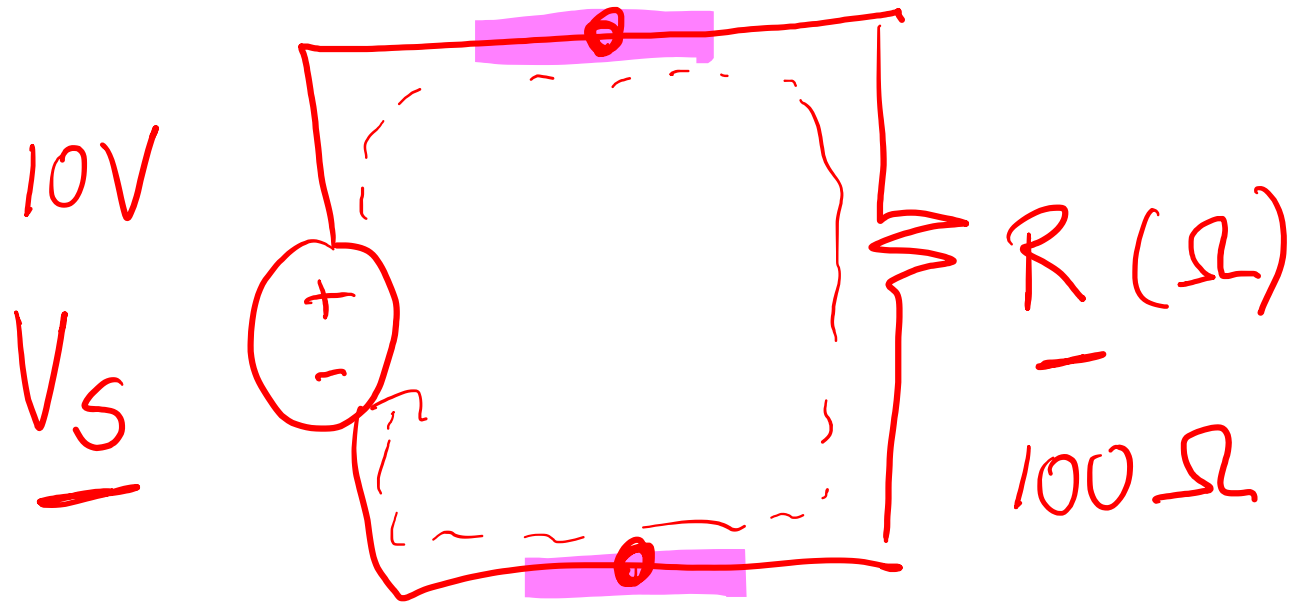
$$I_{elem} = ?$$

I is set by external circuit



Circuit Diagram

Collection of elements, where each element has some voltage across it and some current through it



$$V = IR$$

$$10V = I \cdot 100\Omega$$

$$I = 0.1A$$

Nodes: points where elements meet

Devices as part of a system

Discrete Components



Resistor



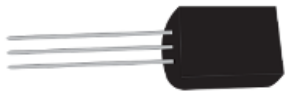
Capacitor



Inductor

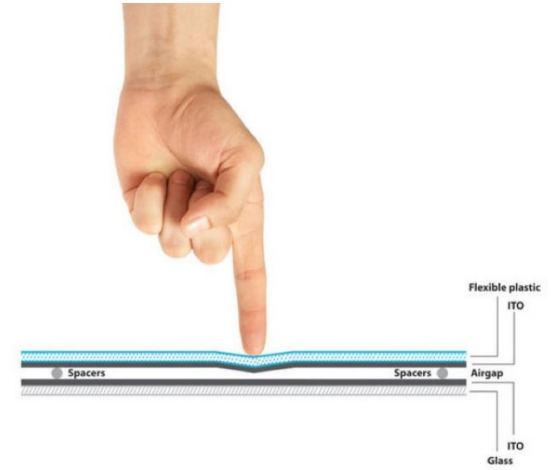
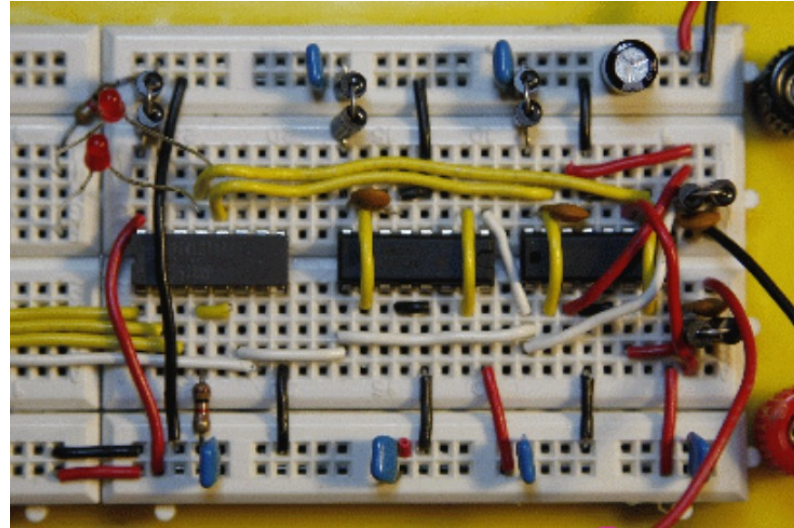


Diode

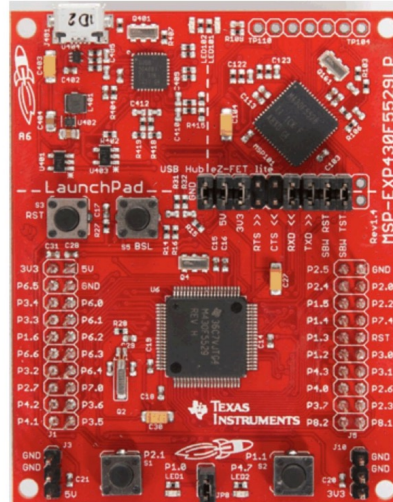


Transistor

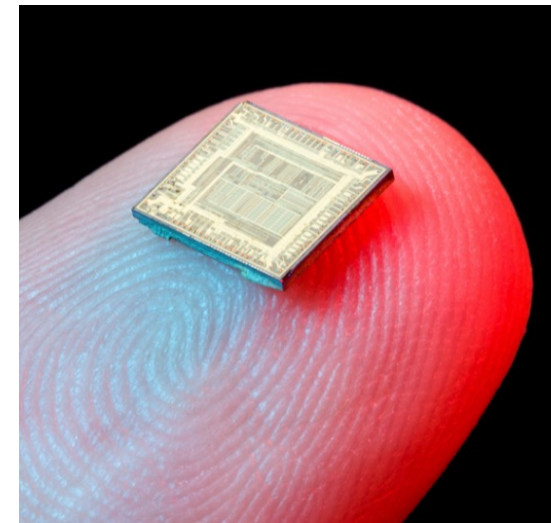
elemains.com



Resistive touchscreen




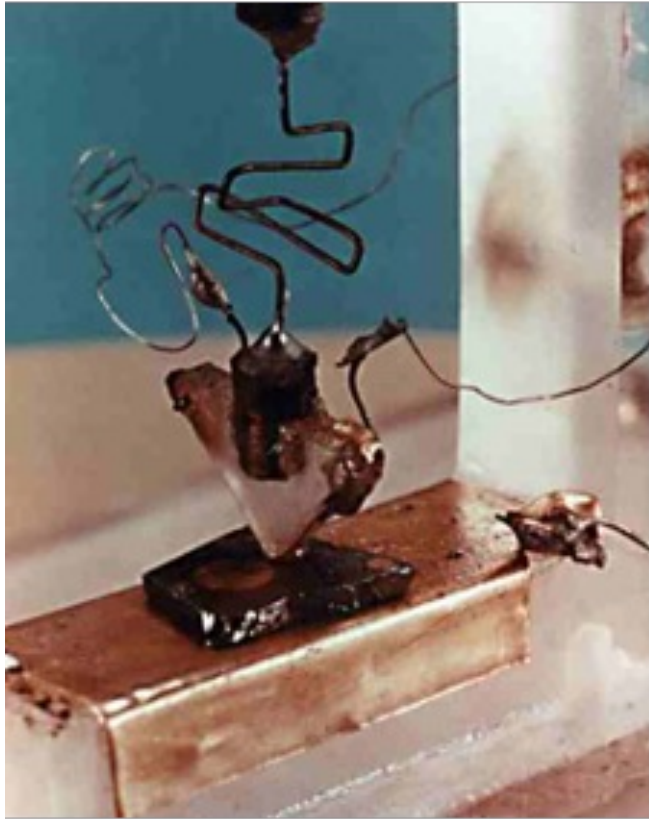
→ Printed Circuit Board
⇒ Surface Mount Components



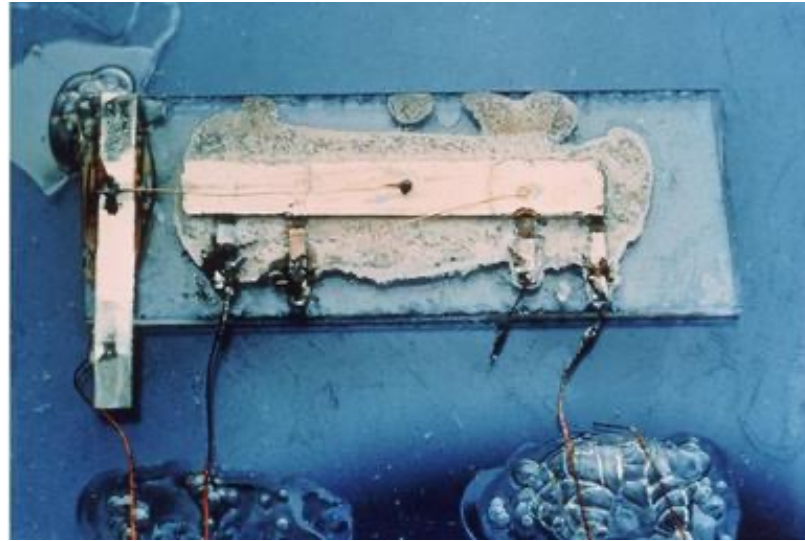
Integrated Circuit

Transistor

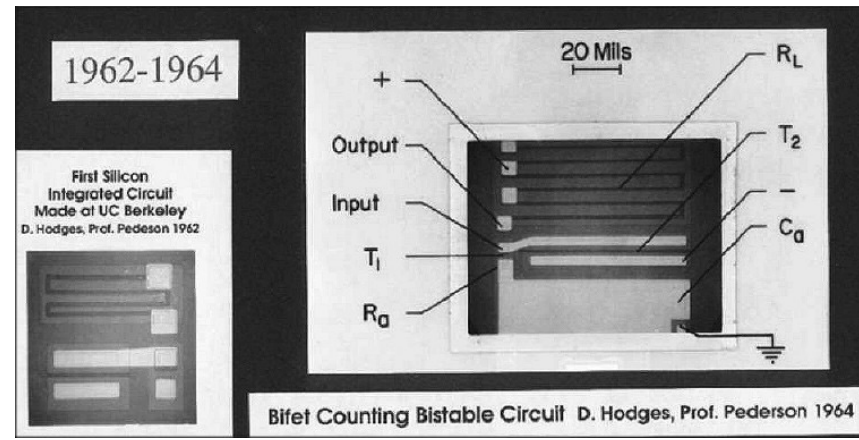
Modern IC: 
2022: Apple M1 Ultra Processor
5nm transistors, 114 billion of them!



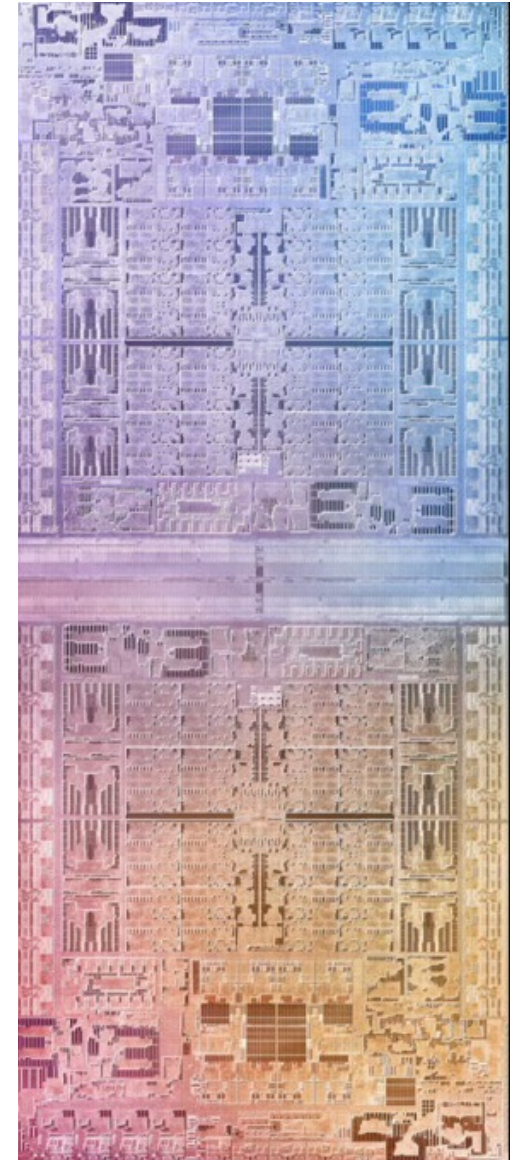
First transistor - Dec 1947



First integrated circuit 1958



Go Bears!



Computational advances due to fabrication advances

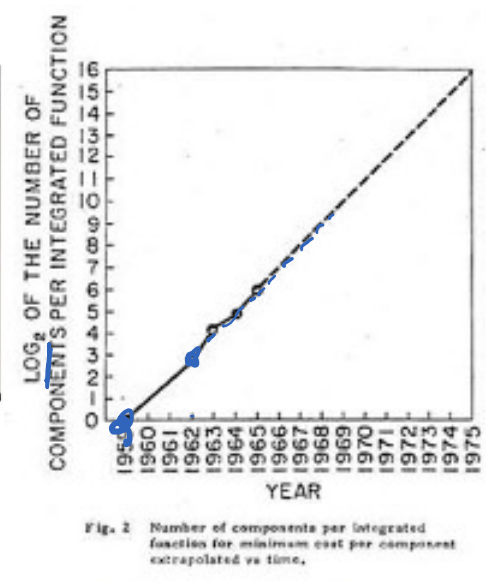
Moore's Law: # of transistors in a dense integrated circuit doubles ~every two years.



Gordon Moore

Intel Cofounder

B.S. Cal 1950!



Electronics Magazine, 1965

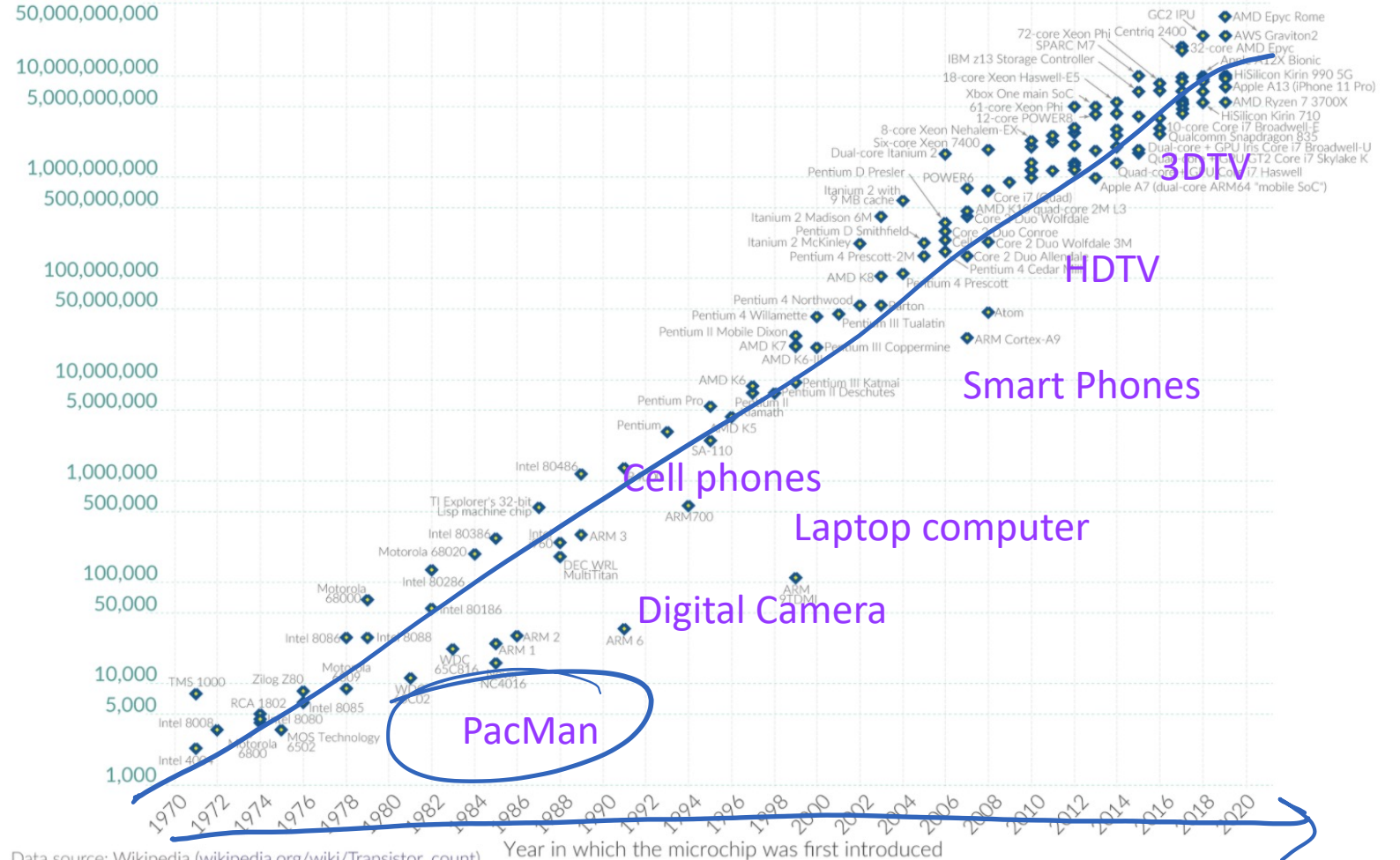
Go Bears!



Moore's Law: The number of transistors on microchips doubles every two years

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

Transistor count



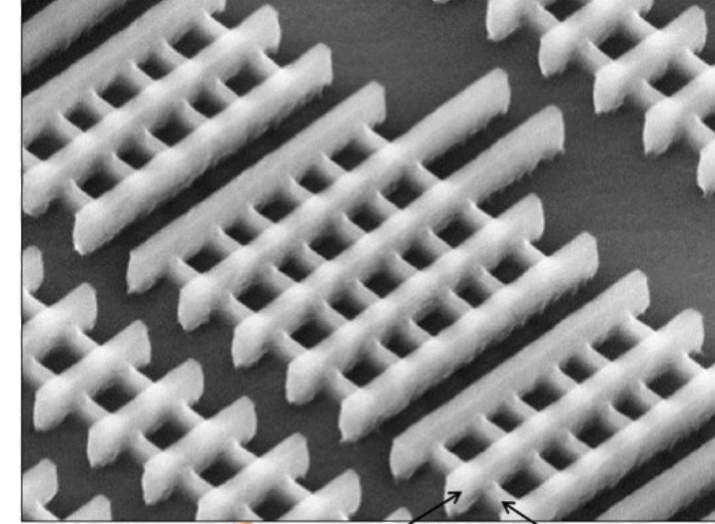
Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)

OurWorldinData.org – Research and data to make progress against the world's largest problems.

Licensed under CC-BY by the authors Hannah Ritchie and Max Roser.

Sense of Scale

**Transistors!
As small as 5nm!**



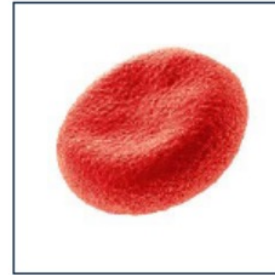
Laura
1.73m



Fly
7 mm



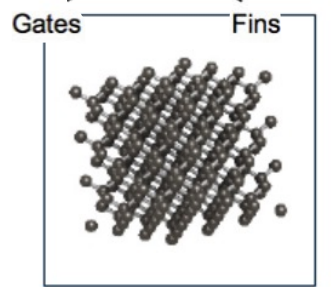
Mite
300 μm



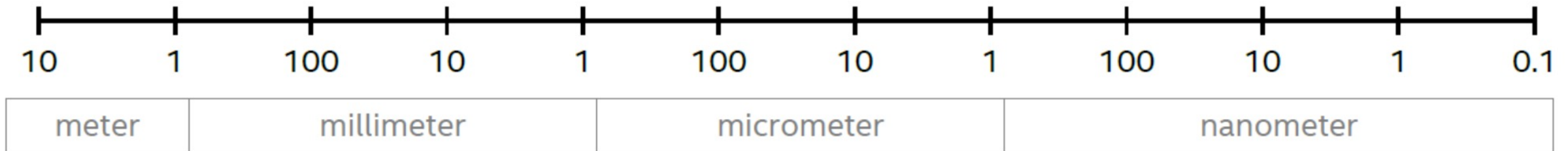
Blood Cell
7 μm



Virus
100 nm



Silicon Atom
0.24 nm



LOG SCALE

FinFET

2320 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 47, NO. 12, DECEMBER 2000

FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm

Digh Hisamoto, *Member, IEEE*, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, *Member, IEEE*, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, *Fellow, IEEE*, and Chenming Hu, *Fellow, IEEE*

Abstract—MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped $\text{Si}_{0.4}\text{Ge}_{0.6}$ as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.

Index Terms—Fully depleted SOI, MOSFET, poly SiGe, short-channel effect.

I. INTRODUCTION

TO DEVELOP sub-50-nm MOSFETs, the double-gate structure has been widely studied. This is because

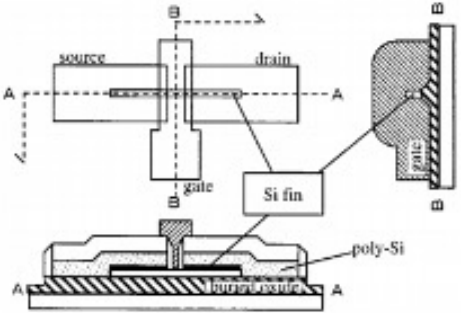


Fig. 1. FinFET typical layout and schematic cross sectional structures.



Prof. Tsu-Jae King Liu

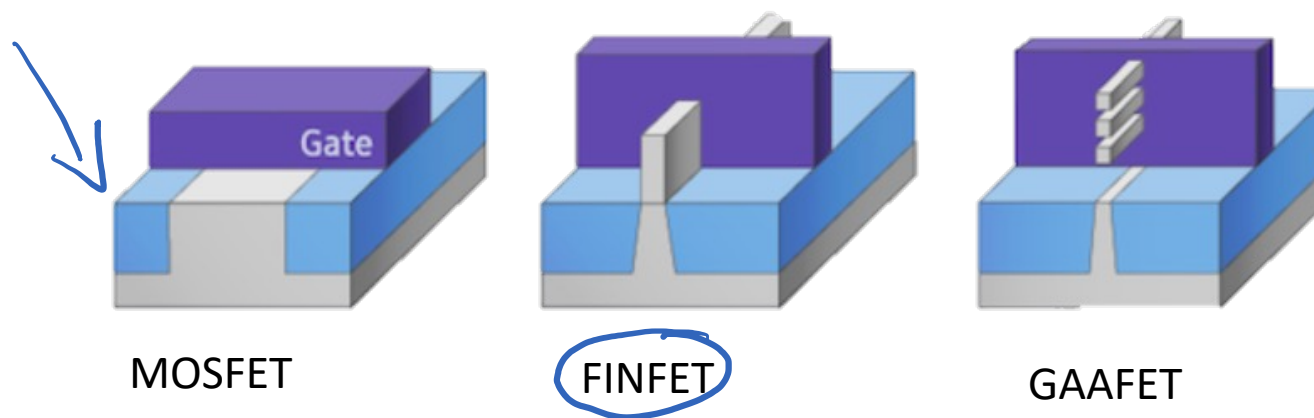


Prof. Jeff Bokor



Prof. Chenming Hu (left)

Go Bears!



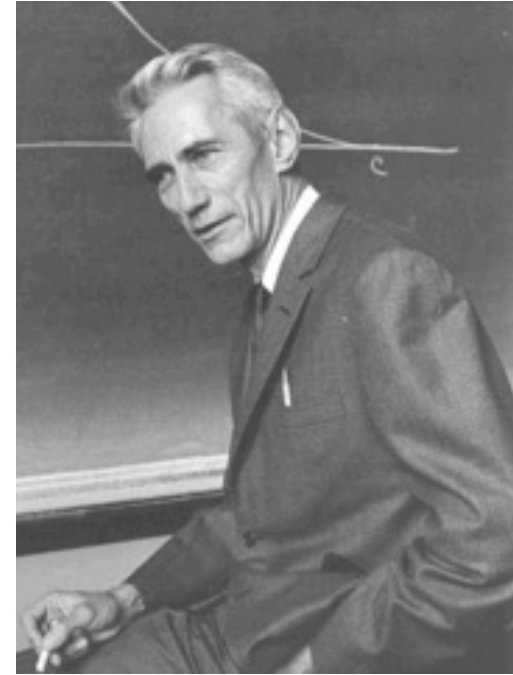
Completing the puzzle... coding!



Ada Lovelace
wrote the first
computer program



Alan Turing
figured out how to
build a computer to
execute programs



Claude Shannon
Information theorist

Module 1: Imaging

