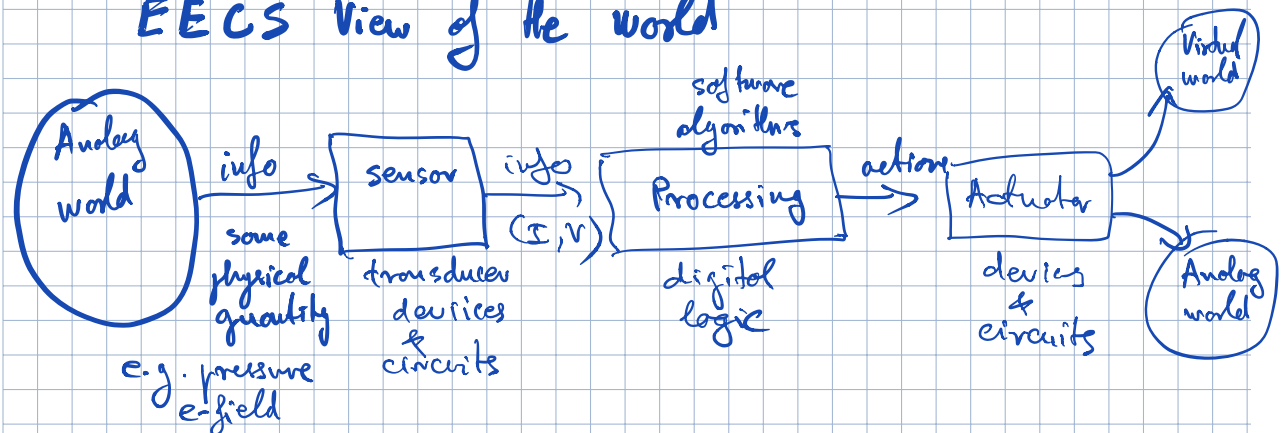
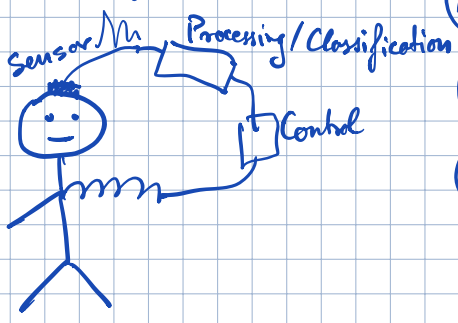
Lecture 1

* EECS 16B Intro
* Computing: Transistors & logic
* RC models
* Solving RC circuits

EECS View of the world



16B examples:

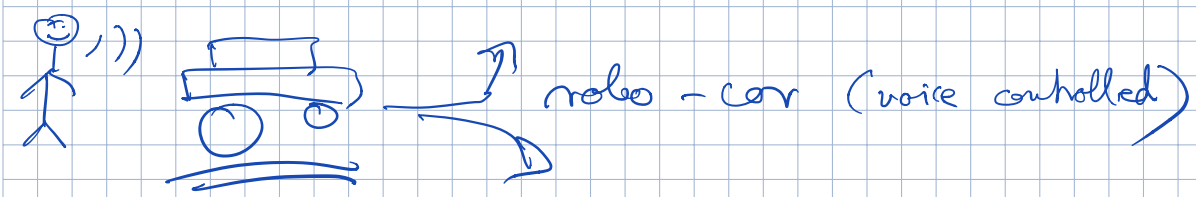


(M1) Sensor: Interface circuits / Diff. eqns

(M2) Control: Feedback

(M3) Processing: Classification SVD/PCA

↓ Lab



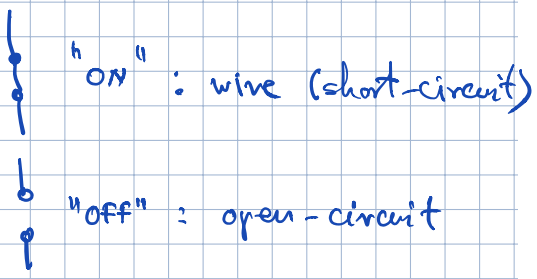
Processing — How do we implement computation?

digital logic → distinct voltage levels (e.g. binary)

logic 0 & logic 1

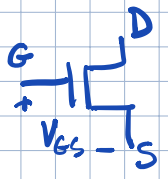
V_0 V_1

16A: Switch

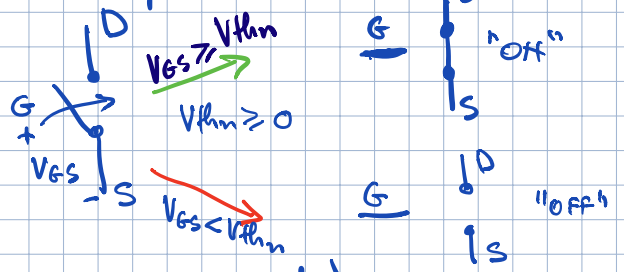


16B: Transistor

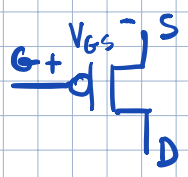
NMOS:

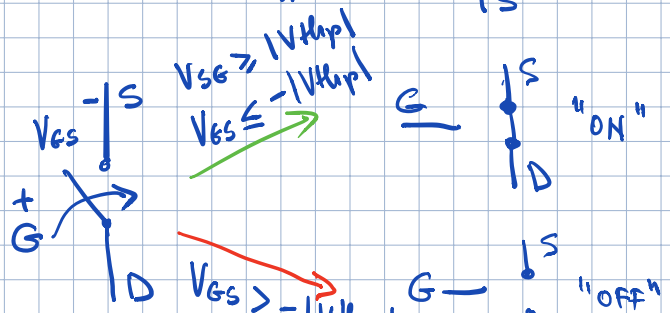


Simple model:



PMOS:



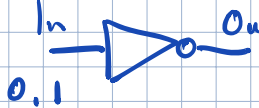


$V_{GS} = -V_{SG}$

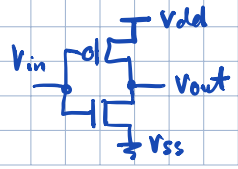
$V_{GS} = V_G - V_S$; $V_{SG} = V_S - V_G$

Simplest logic gate: an **inverter**

"logic symbol"

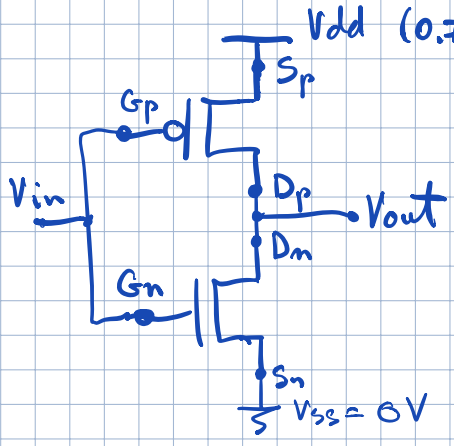


schematic:



(p3)

How does it work?

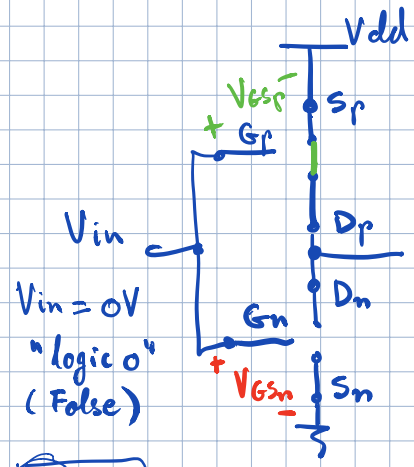


$V_{thn} + |V_{thp}| \geq V_{dd}$ (1GB assumption)

$0 \leq V_{thn} \leq V_{dd}$

$0 \leq |V_{thp}| \leq V_{dd}$

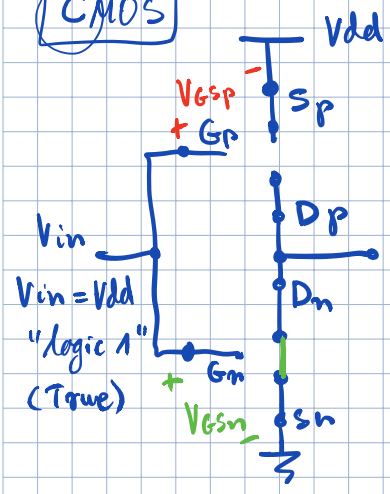
Model:



$V_{GSp} = \underbrace{0V}_{V_{Gp}=V_{in}} - \underbrace{V_{dd}}_{V_{sp}=V_{dd}} = -V_{dd} \leq -|V_{thp}|$ → ON PMOS

$V_{GSn} = \underbrace{0V}_{V_{in}=V_{Gn}} - \underbrace{0V}_{V_{Sn}=0V=V_{SS}} = 0V < V_{thn} \Rightarrow$ OFF NMOS

CMOS



$V_{GSp} = \underbrace{V_{Gp}}_{V_{in}=V_{dd}} - V_{dd} = V_{dd} - V_{dd} = 0V > -|V_{thp}|$

$\Rightarrow$ OFF PMOS

$V_{GSn} = \underbrace{V_{Gn}}_{V_{in}=V_{dd}} - \underbrace{V_{Sn}}_{=V_{SS}=0V} = V_{dd} - 0V = V_{dd} \geq V_{thn} \Rightarrow$

ON NMOS

Truth table:

	Vin	Vout
"logic 0"	0V	Vdd (logic 1)
"logic 1"	Vdd	0V (logic 0)

Boolean math

In	Out
0	1
1	0

inverter

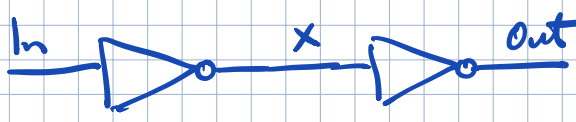
$Out = \overline{In}$

NAND , NOR

$Out = \overline{A \cdot B}$ $\quad$ $Out = \overline{A + B}$

Let's make a processor: Cascading logic

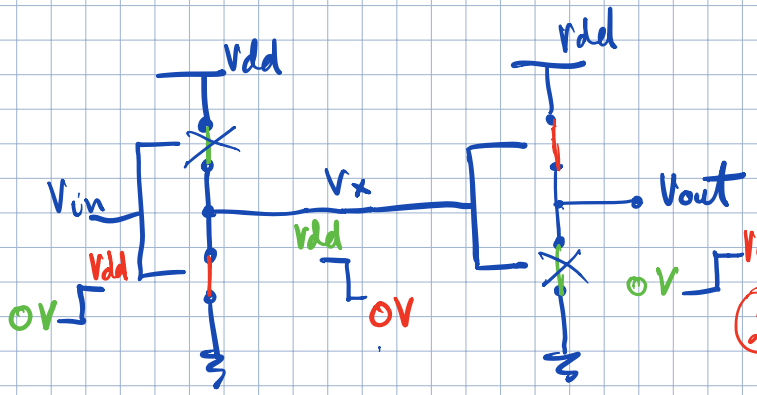
Simple model:



$x = \overline{In}$

$Out = \overline{x}$

$Out = \overline{\overline{In}} = In$



State:

① $Vin = 0V \Rightarrow Vx = Vdd \Rightarrow Vout = 0V$

② $Vin = Vdd \Rightarrow Vx = 0V \Rightarrow$

$\Rightarrow Vout = Vdd$

It looks like this process is instantaneous ▽ o

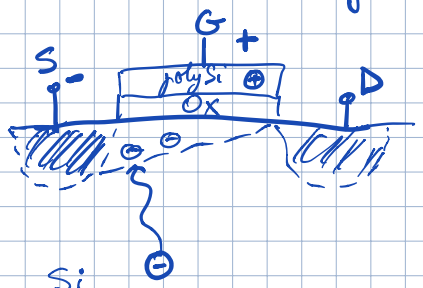
Would make a super-fast processor & super cool ▽ !

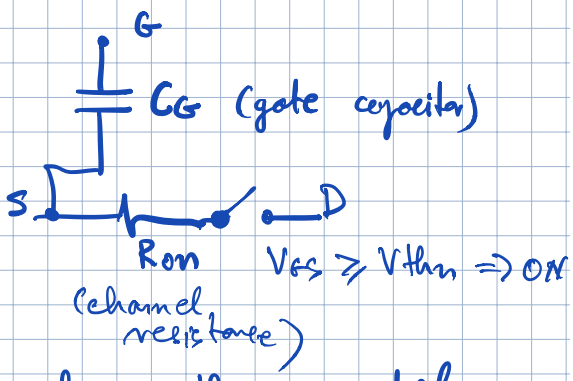
Not real ▽ o 

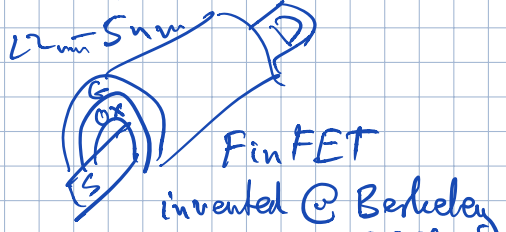
Need to look at how a device is made to make a better model.

p5

NMOS (n-channel metal-oxide semiconductor field effect transistor)







FinFET
invented @ Berkeley EECS

To analyze this model need to understand RC circuits.