Discussion 5A

1. **Series Resonant Circuit (Hambley Example 6.5)**

   Consider the following series resonant circuit.
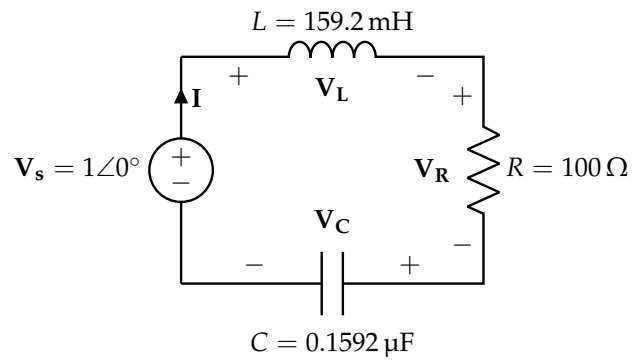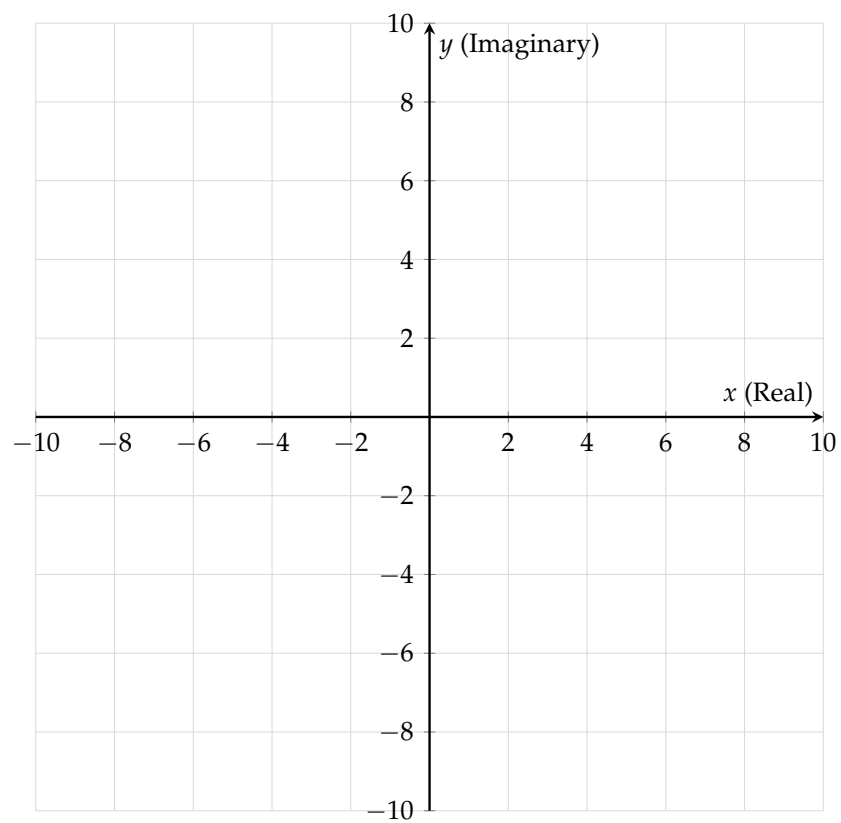

Figure 1

   (a) **Compute the resonant frequency, the bandwidth, and the half-power frequencies.**

(b) Assuming that the frequency of the source is the same as the resonant frequency, **find the phasor voltages across the elements**

(c) **Sketch the phasors from part (b).**

2. (PRACTICE) Parallel Resonant Circuit (Hambley Example 6.6)

Find the L and C values for a parallel resonant circuit that has $R = 10\,\text{k}\Omega$, $f_0 = 1\,\text{MHz}$, and $B = 100\,\text{kHz}$. You are also told that $\mathbf{I} = 10^{-3}\angle 0°$ A.
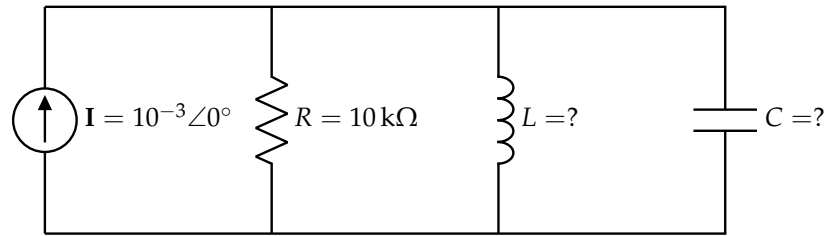

Figure 2: Parallel Resonant Circuit

(a) **Calculate the current phasors through each of the elements at resonance.**

(b) **Draw a phasor diagram for the current phasors calculated in part (a).**

3. **Introducing the Transistor Switch Model**

As seen in lecture, we can model the behavior of a transistor with a capacitor and resistor. In this model, the gate capacitances C_{GN} and C_{GP} represent the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.
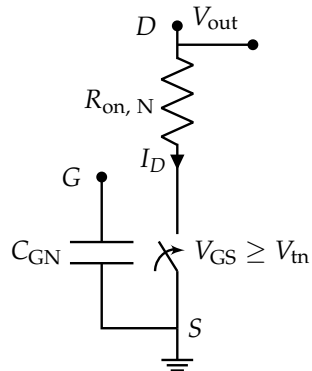
(a) NMOS Resistor-switch-capacitor model
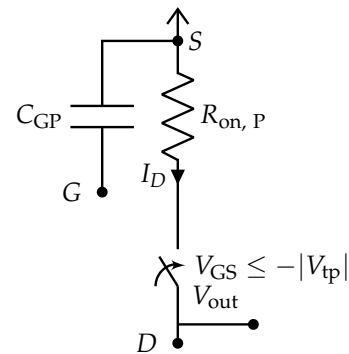
(b) PMOS Resistor-switch-capacitor model

In the configuration below, you have two CMOS inverters made from NMOS and PMOS devices. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (Figure 4).

Both NMOS and PMOS devices have an "on resistance" of $R_{on, N} = R_{on, P} = 1\text{ k}\Omega$, and each has a gate capacitance (input capacitance) of $C_{GN} = C_{GP} = 1\text{ fF}$ (fF = femto-Farads = 1×10^{-15} F).

We assume the "off resistance" (the resistance when the transistor is off) is infinite (i.e., the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V.
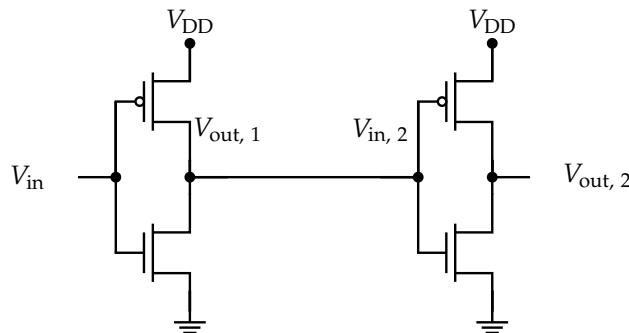

Figure 4: CMOS Inverter chain

If we redraw our CMOS inverter chain with the transistor resistor-switch models provided in Figure 3a and Figure 3b, we get the following circuit:
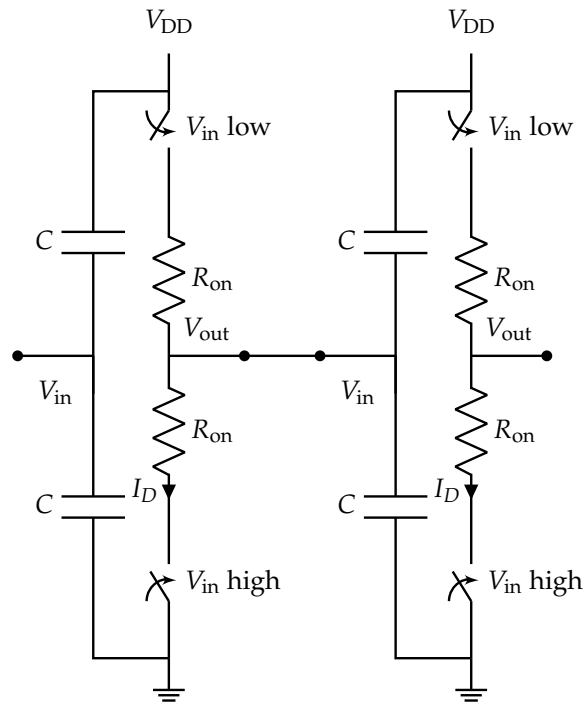

Figure 5: CMOS Inverter Chain w/ Transistor Resistor-switch model

(a) Assume the input to the first inverter has been low ($V_{in} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{in} = V_{DD}$).

Draw an RC circuit for the output voltage of the first inverter ($V_{out, 1}$) for time $t \geq 0$.

(HINT: Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.)

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(b) **Using the RC circuit from part (a), write a differential equation describing the output voltage of the first inverter ($V_{\text{out, 1}}$) for time $t \geq 0$.**

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