Discussion 5A

1. Series Resonant Circuit (Hambley Example 6.5)

Consider the following series resonant circuit.

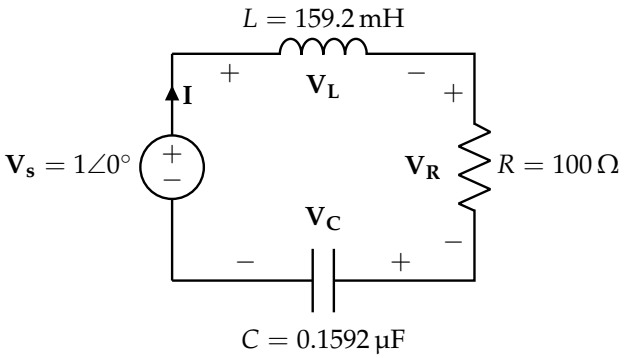


Figure 1

(a) **Compute the resonant frequency, the bandwidth, and the half-power frequencies.**

Solution: First, we can solve for the resonant frequency using the formula:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.1592 \times 0.1592 \times 10^{-6}}} = 1000\,\text{Hz} \tag{1}$$

Next, we will solve for the bandwidth which is given by the following:

$$B = \frac{f_0}{Q_s} \tag{2}$$
$$= \frac{f_0}{\frac{2\pi f_0 L}{R}} \tag{3}$$
$$= \frac{R}{2\pi L} \tag{4}$$
$$= \frac{100}{2\pi 0.1592} \tag{5}$$
$$= 100\,\text{Hz} \tag{6}$$

We will approximate the half-power frequencies as shown below:

$$f_H \cong f_0 + \frac{B}{2} = 1000 + \frac{100}{2} = 1050\,\text{Hz} \tag{7}$$
$$f_L \cong f_0 - \frac{B}{2} = 1000 - \frac{100}{2} = 950\,\text{Hz} \tag{8}$$

(b) Assuming that the frequency of the source is the same as the resonant frequency, **find the phasor voltages across the elements**

Solution: Let's start by calculating the impedances of the inductance and the capacitance at resonance:

$$Z_L = \mathrm{j}2\pi f_0 L \tag{9}$$
$$= \mathrm{j}2\pi \times 1000 \times 0.1592 \tag{10}$$
$$= \mathrm{j}1000\,\Omega \tag{11}$$
$$Z_C = -\mathrm{j}\frac{1}{2\pi f_0 C} \tag{12}$$
$$= -\mathrm{j}\frac{1}{2\pi \times 1000 \times 0.1592 \times 10^{-6}} \tag{13}$$
$$= -\mathrm{j}1000\,\Omega \tag{14}$$

As we expected, the reactances are equal in magnitude at the resonant frequency. The total impedance of the circuit is:

$$Z_s = R + Z_L + Z_C = 100 + \mathrm{j}1000 - \mathrm{j}1000 = 100\,\Omega \tag{15}$$

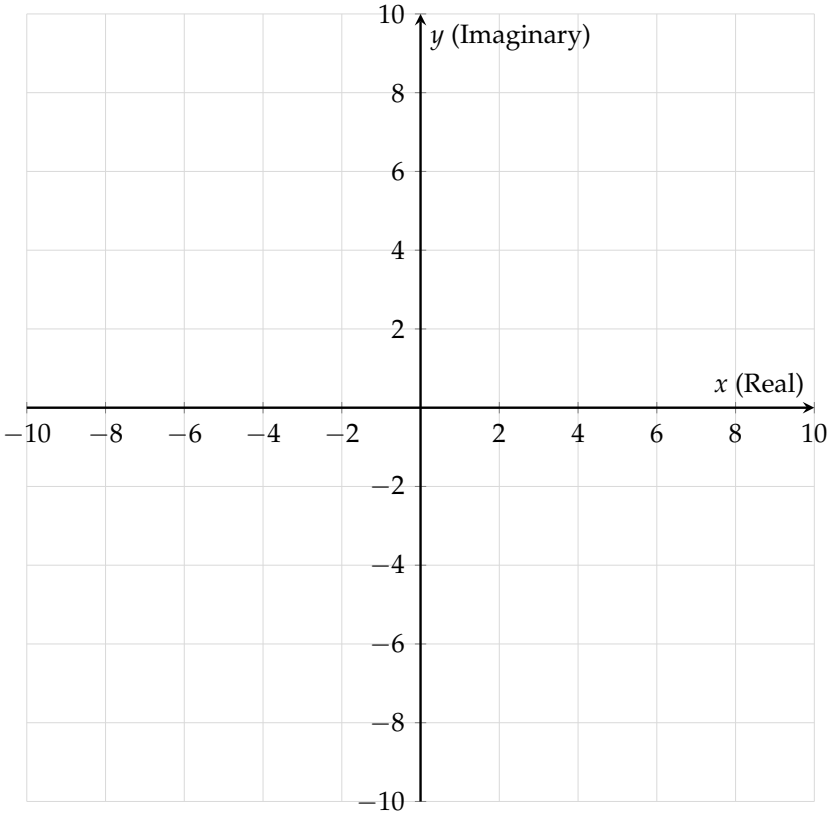
Now, calculating the phasor current we have:

$$\mathbf{I} = \frac{\mathbf{V_s}}{Z_s} = \frac{1\angle 0^\circ}{100} = 0.01\angle 0^\circ \tag{16}$$

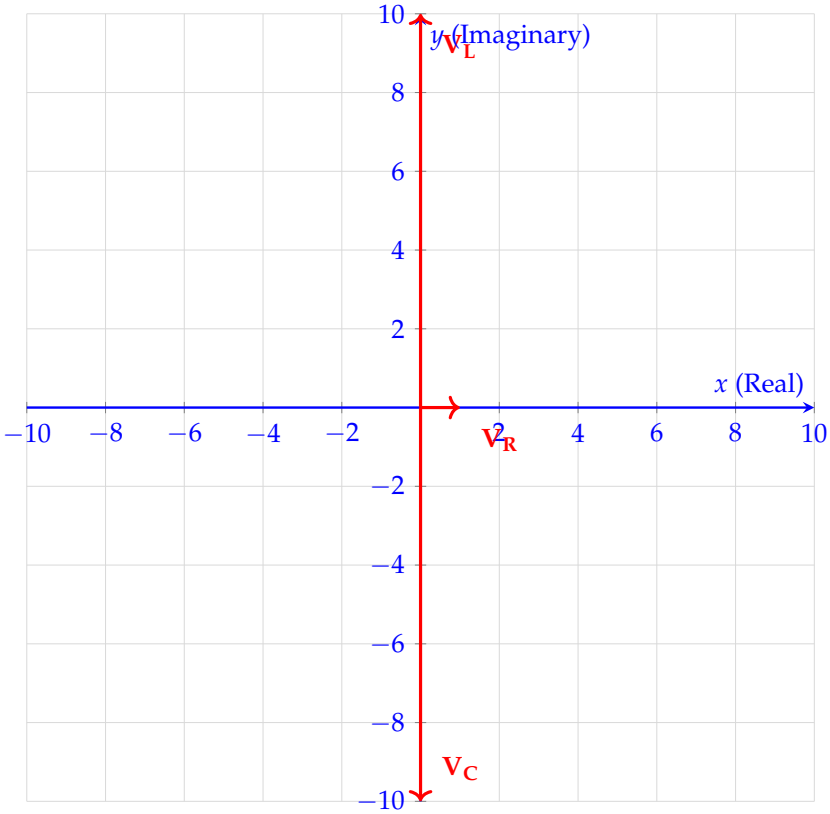
The voltages across the elements are:

$$\mathbf{V_R} = R\mathbf{I} = 100 \times 0.01\angle 0^\circ = 1\angle 0^\circ \tag{17}$$
$$\mathbf{V_L} = Z_L\mathbf{I} = \mathrm{j}1000 \times 0.01\angle 0^\circ = 10\angle 90^\circ \tag{18}$$
$$\mathbf{V_C} = Z_C\mathbf{I} = -\mathrm{j}1000 \times 0.01\angle 0^\circ = 10\angle -90^\circ \tag{19}$$

(c) **Sketch the phasors from part (b).**



Solution:



2. (PRACTICE) Parallel Resonant Circuit (Hambley Example 6.6)

Find the L and C values for a parallel resonant circuit that has $R = 10\,\text{k}\Omega$, $f_0 = 1\,\text{MHz}$, and $B = 100\,\text{kHz}$. You are also told that $\mathbf{I} = 10^{-3}\angle 0^\circ$ A.

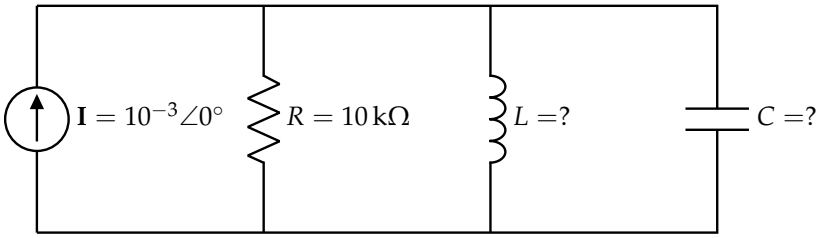


Figure 2: Parallel Resonant Circuit

(a) **Calculate the current phasors through each of the elements at resonance.**

Solution: First, we compute the quality factor of the circuit.

$$Q_p = \frac{f_0}{B} = \frac{10^6}{10^5} = 10 \tag{20}$$

Using the equation:

$$Q_p = \frac{R}{2\pi f_0 L} \tag{21}$$

and rearranging, we can solve for inductance:

$$L = \frac{R}{2\pi f_0 Q_p} = \frac{10^4}{2\pi \times 10^6 \times 10} = 159.2\,\mu\text{H} \tag{22}$$

Similarly, rearranging the equation:

$$Q_p = 2\pi f_0 C R \tag{23}$$

we can solve for C:

$$C = \frac{Q_p}{2\pi f_0 R} = \frac{10}{2\pi \times 10^6 \times 10^4} = 159.2\,\text{pF} \tag{24}$$

At resonance, the voltage is given by:

$$\mathbf{V}_{\text{out}} = \mathbf{I}R = \left(10^{-3}\angle 0^\circ\right) \times 10^4 = 10\angle 0^\circ\ \text{V} \tag{25}$$

and currents can be solved using the impedances:

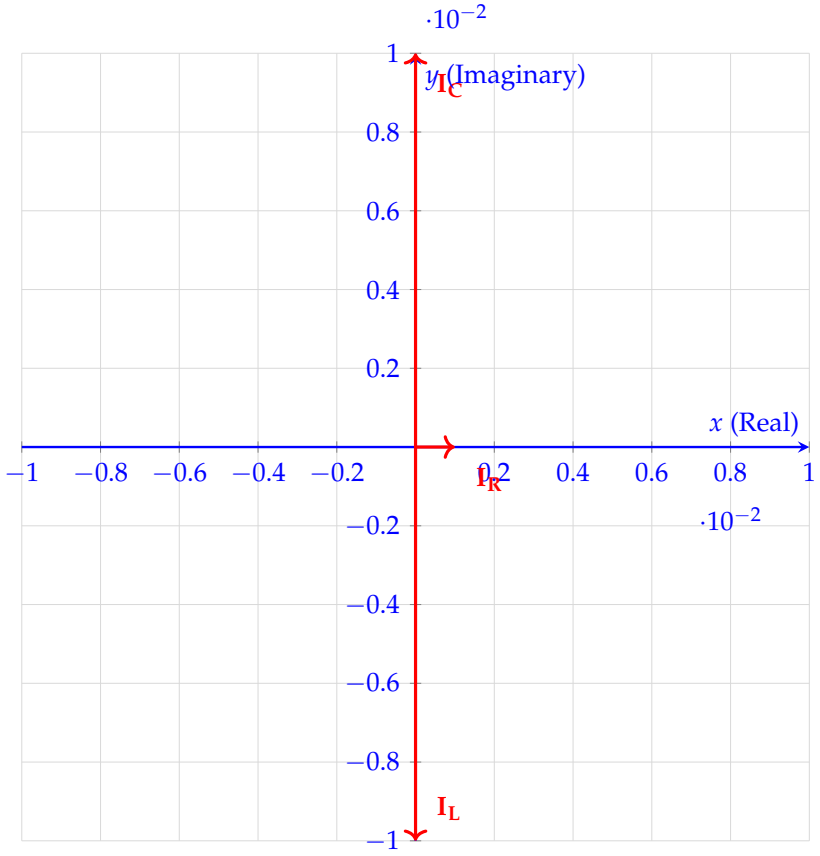
$$\mathbf{I_R} = \frac{\mathbf{V}_{\text{out}}}{R} = \frac{10\angle 0^\circ}{10^4} = 10^{-3}\angle 0^\circ\ \text{A} \tag{26}$$

$$\mathbf{I_L} = \frac{\mathbf{V}_{\text{out}}}{\text{j}2\pi f_0 L} = \frac{10\angle 0^\circ}{\text{j}10^3} = 10^{-2}\angle -90^\circ\ \text{A} \tag{27}$$

$$\mathbf{I_C} = \frac{\mathbf{V}_{\text{out}}}{\frac{-\text{j}}{2\pi f_0 C}} = \frac{10\angle 0^\circ}{-\text{j}10^3} = 10^{-2}\angle 90^\circ\ \text{A} \tag{28}$$

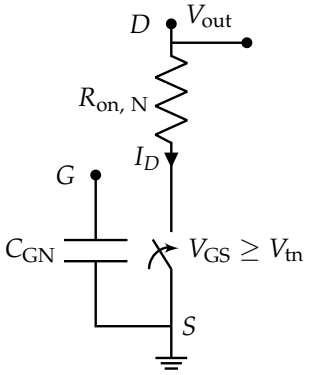
(b) **Draw a phasor diagram for the current phasors calculated in part (a).**

Solution:

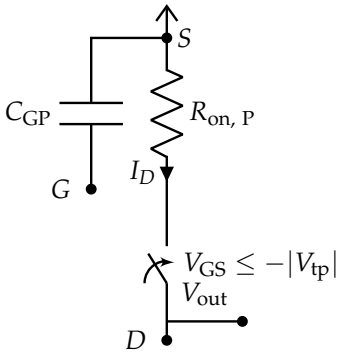


3. Introducing the Transistor Switch Model

As seen in lecture, we can model the behavior of a transistor with a capacitor and resistor. In this model, the gate capacitances C_{GN} and C_{GP} represent the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.



(a) NMOS Resistor-switch-capacitor model



(b) PMOS Resistor-switch-capacitor model

In the configuration below, you have two CMOS inverters made from NMOS and PMOS devices. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (Figure 4).

Both NMOS and PMOS devices have an "on resistance" of $R_{on,\,N} = R_{on,\,P} = 1\ \text{k}\Omega$, and each has a gate capacitance (input capacitance) of $C_{GN} = C_{GP} = 1\ \text{fF}$ (fF = femto-Farads = 1×10^{-15} F).

We assume the "off resistance" (the resistance when the transistor is off) is infinite (i.e., the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V.

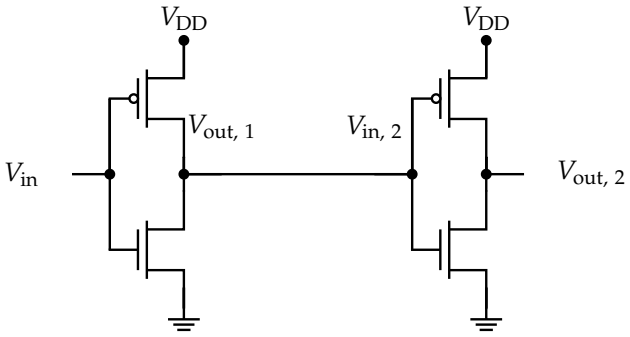


Figure 4: CMOS Inverter chain

If we redraw our CMOS inverter chain with the transistor resistor-switch models provided in Figure 3a and Figure 3b, we get the following circuit:

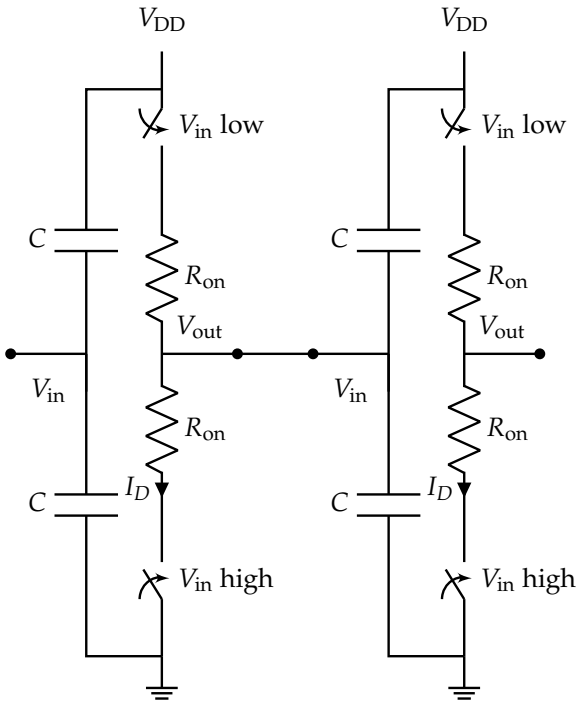


Figure 5: CMOS Inverter Chain w/ Transistor Resistor-switch model

(a) Assume the input to the first inverter has been low ($V_{in} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{in} = V_{DD}$).

Draw an RC circuit for the output voltage of the first inverter ($V_{out,\,1}$) for time $t \geq 0$.

(HINT: Don't forget that the second inverter is "loading" the output of the first inverter — you need to think about both of them.)

Solution: To analyze this circuit as an RC circuit we can recall the transistor switch model. Using this we can see that the first inverter's output appears as a resistor connected to V_{DD} when the input is low (NMOS off, PMOS on), or a resistor connected to ground when the input turns high (NMOS on, PMOS off).

Before $t = 0$, the input to the first inverter was low for a long time. This means that for $t < 0$, the output of the inverter ($V_{out,\,1}$) had been held at V_{DD} for a long time.

At $t = 0$, the input goes high, which means that the input inverter's NMOS device turns on, connecting $V_{out,\,1}$ to ground through a resistance of R_{on}.

The second inverter "loads" the output of the first inverter. From the notes in the problem, we can model the gates of the transistors as capacitors. These gates together form our capacitive load. The gate of the PMOS acts as a capacitor to V_{DD} and the gate of the NMOS acts as a capacitor to ground.

Using this we can draw the following RC circuit:

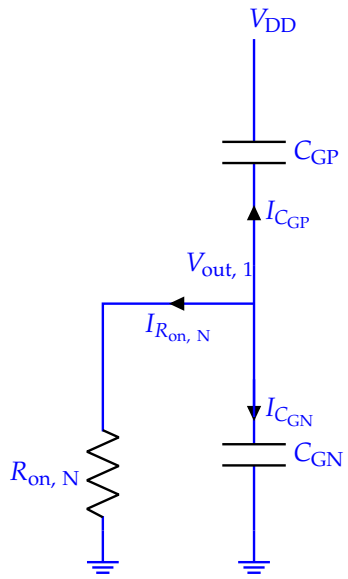


Figure 6: First inverter output at 0

(b) **Using the RC circuit from part (a), write a differential equation describing the output voltage of the first inverter ($V_{out,\,1}$) for time $t \geq 0$.**

Solution: To get the differential equation describing the output of the first inverter at time $t \geq 0$ let us first think about the behavior of the circuit at and after $t = 0$.

Before $t = 0$ we know that the output $V_{out,\,1} = V_{DD}$. This means that C_{GN} is charged, while C_{GP} is not as there is no voltage difference across it.

At $t = 0$, when the input to the first inverter changes (input switches to high), the NMOS will turn on, discharging the $V_{out,\,1}$ node. Thus $V_{out,\,1}$ will eventually discharge to zero in steady state.

We know the voltage across C_{GP} is $V_{out,\,1}(t) - V_{DD}$ and the voltage across C_{GN} is $V_{out,\,1}(t)$. Using this information we can set up a differential equation to solve for $V_{out}(t)$.

Writing the expressions for the three branch currents yields:

$$I_{C_{GP}} = C_{GP}\frac{d}{dt}(V_{out,\,1}(t) - V_{DD}) \tag{29}$$

$$I_{C_{GN}} = C_{GN}\frac{d}{dt}V_{out,\,1}(t) \tag{30}$$

$$I_{R_{on,\,N}} = \frac{V_{out,\,1}(t)}{R_{on,\,N}} \tag{31}$$

Writing KCL at the single node yields:

$$I_{C_{GP}} + I_{C_{GN}} + I_{R_{on,\,N}} = 0 \tag{32}$$

in other words:

$$I_{C_{GP}} + I_{C_{GN}} = -I_{R_{on,\,N}} \tag{33}$$

Expanding the branch currents with their expressions:

$$C_{GP}\frac{d}{dt}(V_{out,\,1}(t) - V_{DD}) + C_{GN}\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t)}{R_{on,\,N}} \tag{34}$$

$$C_{GP}\frac{d}{dt}V_{out,\,1}(t) + C_{GN}\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t)}{R_{on,\,N}} \tag{35}$$

$$(C_{GP} + C_{GN})\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t)}{R_{on,\,N}} \tag{36}$$

Re-writing as a first-order differential equation for $V_{out,\,1}$ yields:

$$\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t)}{R_{on,\,N}(C_{GP} + C_{GN})} \tag{37}$$

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