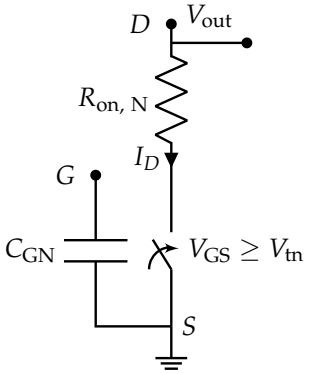
Discussion 5B

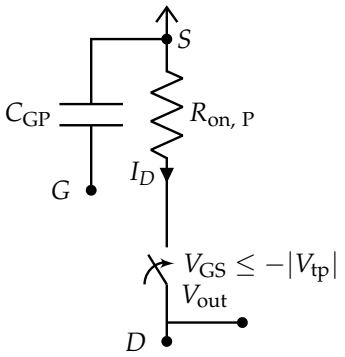
This discussion is a continuation of Discussion 5A.

1. Transistor Switch Model

(Repeated from Discussion 5A) As seen in lecture, we can model the behavior of a transistor with a capacitor and resistor. In this model, the gate capacitances C_{GN} and C_{GP} represent the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.



(a) NMOS Resistor-switch-capacitor model



(b) PMOS Resistor-switch-capacitor model

In the configuration below, you have two CMOS inverters made from NMOS and PMOS devices. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (Figure 2).

Both NMOS and PMOS devices have an "on resistance" of $R_{on,\,N} = R_{on,\,P} = 1\ \text{k}\Omega$, and each has a gate capacitance (input capacitance) of $C_{GN} = C_{GP} = 1\ \text{fF}$ (fF = femto-Farads = 1×10^{-15} F).

We assume the "off resistance" (the resistance when the transistor is off) is infinite (i.e., the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V.

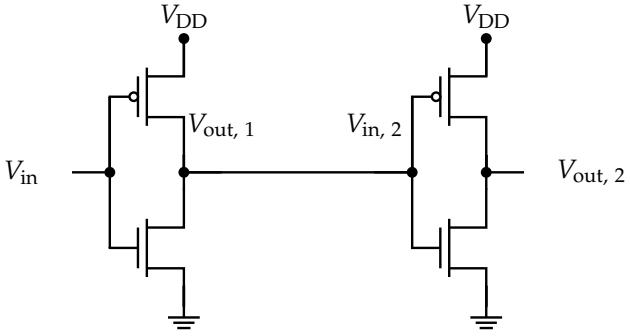


Figure 2: CMOS Inverter chain

(a) Recall that in the previous discussion, we derived that the RC circuit for the output of the first inverter was:

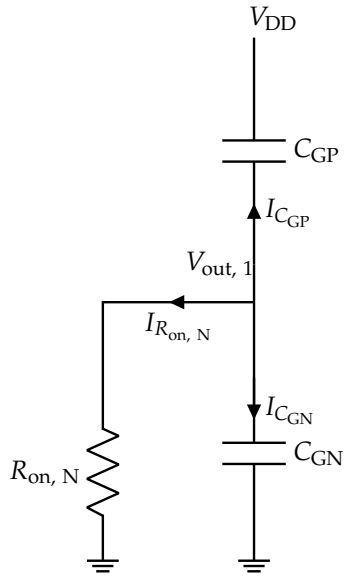


Figure 3: First inverter output at 0

The corresponding differential equation for the output of the first inverter was

$$\frac{\mathrm{d}}{\mathrm{d}t} V_{\text{out, 1}}(t) = -\frac{V_{\text{out, 1}}(t)}{R_{\text{on, N}}(C_{\text{GP}} + C_{\text{GN}})} \tag{1}$$

This was assumimg that the input to the first inverter has been low ($V_{\text{in}} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{\text{in}} = V_{\text{DD}}$).

Using these initial conditions, **solve for** $V_{\text{out, 1}}(t)$**.**

(b) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the initial slope, (3) the asymptotic value, and (4) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.**

(c) A long time later, the input to the first inverter switches low again.

Draw the new RC circuit and set up another differential equation for $V_{\text{out},\,1}(t)$. *(HINT: This should look very similar to what we solved for Discussion 5A. What is different about our circuit?)*

(d) **Solve for $V_{\text{out, 1}}(t)$.**

(e) **(PRACTICE) Sketch the output voltage of the first inverter ($V_{\text{out, 1}}$), showing clearly (1) the initial value, (2) the initial slope, and (3) the asymptotic value.**

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