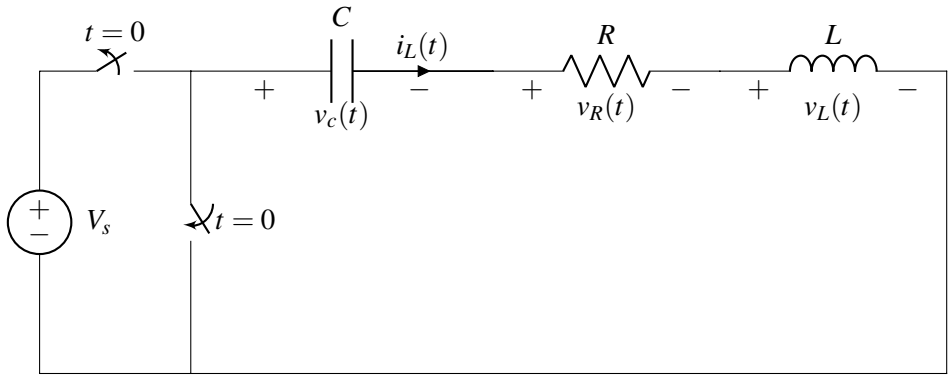
EECS 16B Designing Information Devices and Systems II
Summer 2020 UC Berkeley Circuits Review

1. Circuits State Space (X pts)

Consider the following series RLC circuit from homework.



We used the state vector $\vec{x}(t) = \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix}$ to derive the following state equation for the circuit:

$$\frac{d}{dt}\vec{x}(t) = A\vec{x}(t) = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \vec{x}(t)$$

The eigenvalues of A are

$$\lambda = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

(a) Let's define a new state vector $\vec{\tilde{x}}(t) = \begin{bmatrix} i_L(t) + v_c(t) \\ v_L(t) \end{bmatrix}$.

Find an invertible matrix T, such that $\tilde{x}(t) = T\vec{x}(t)$. Assume that $R \neq 1\,\Omega$.

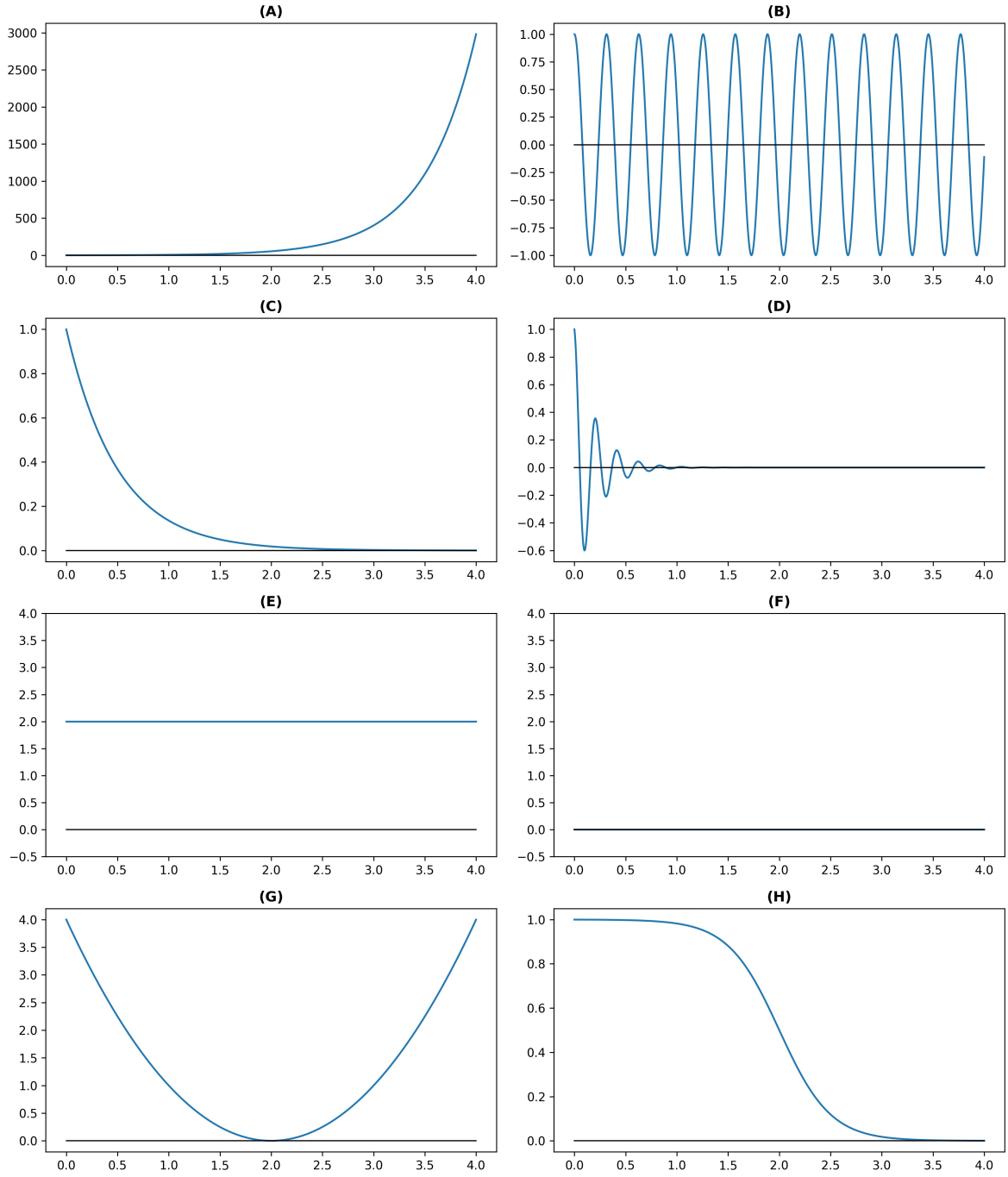
(b) **Find the matrix $\tilde{A}$, such that $\frac{d}{dt}\vec{\tilde{x}}(t) = \tilde{A}\vec{\tilde{x}}(t)$.**

(c) **What are the eigenvalues of $\tilde{A}$?**

(d) Now let $\vec{\tilde{x}}(t) = \begin{bmatrix} i_L(t) \\ v_C(t) \\ v_L(t) \end{bmatrix}$.

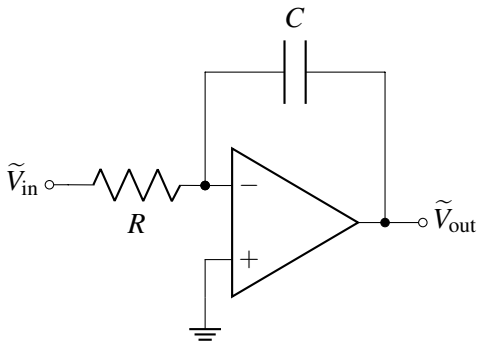
Find a 3×3 matrix $\tilde{A}$ such that $\frac{d}{dt}\vec{\tilde{x}}(t) = \tilde{A}\vec{\tilde{x}}(t)$. Also, what are the eigenvalues of $\tilde{A}$?

(e) Assume that we measure $v_c(t)$. **Which of the following are possible graphs of $v_c(t)$?**



2. Derive the Integrator (X pts)

Consider the following circuit:



(a) **Find the transfer function of this circuit** $H(\omega) = \frac{\tilde{V}_{\text{out}}}{\tilde{V}_{\text{in}}}$**.**

(b) **Draw the Bode magnitude and phase plots of the transfer function.** Assume that $RC = 10^{-2}$. *Hint:* Try plotting the magnitude and phase for $\omega = 1, 10, 100, \ldots$ and look for a pattern.

(c) **Find $v_{\text{out}}(t)$ for the following inputs $v_{\text{in}}(t)$.** You can assume that any transients have died out.

i. $v_{\text{in}}(t) = 10\sin(100t)$

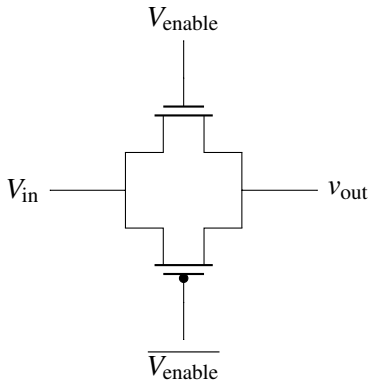
ii. $v_{\text{in}}(t) = -5\cos\left(10^3 t + \frac{\pi}{2}\right)$

(d) **Find $v_{\text{out}}(t \to \infty)$ if $v_{\text{in}}(t) = 5\,\text{V}$.** *Hint:* What is ω?

(e) Assume that $v_{\text{out}}(0) = 0\,\text{V}$ and that $v_{\text{in}}(t) = 5\,\text{V}$. **Find an expression for $v_{\text{out}}(t)$ for $t \geq 0$.**

3. The Old Switcheroo (X pts)

Consider the following circuit that implements a switch using transistors.



V_{enable} and V_{in} are digital signals that can be either at 0 V or 1 V. If $V_{\text{enable}} = 1\,\text{V}$, the switch is closed and V_{in} is connected to V_{out}. Otherwise, if $V_{\text{enable}} = 0\,\text{V}$, the switch is open.

The threshold voltage of the NMOS is $V_{t,n} = 0.3\,\text{V}$, and the threshold voltage of the PMOS is $V_{t,p} = -0.3\,\text{V}$. You may approximate $0.3 \approx e^{-1}$.

Assume that at time $t = 0$, $V_{\text{in}} = 1\,\text{V}$, $v_{\text{out}}(0) = 0\,\text{V}$, and $V_{\text{enable}} = 1\,\text{V}$. We want to know how $v_{\text{out}}(t)$ behaves over time for $t \geq 0$.

(a) **Draw the equivalent circuit of the switch for $t \geq 0$ using the resistor-capacitor model of the transistor. Determine which transistors are on and off.**

(b) **Write down a differential equation for $V_{\text{out}}(t)$ that describes the behavior for some time after $t \geq 0$.** Assume that both the NMOS and PMOS transistors have an on-resistance of R_{on} and a gate-source capacitance of C_{gs}.

(c) **Solve for $V_{\text{out}}(t)$. Assume that $R_{\text{on}}C_{\text{gs}} = 1 \times 10^{-9}\,\text{s}$.**

(d) **Until what time $T \geq 0$ is your differential equation valid?**

4. Simulated Inductor - Gyrator (X pts)

Resistors, capacitors, inductors, and transistors make up the basic building blocks for many interesting and useful circuits. However, for certain applications, the size of the inductance would require very large inductors which may not feasibly fit on a small chip.

One way to work around this constraint is to simulate an inductor using a circuit called a gyrator. A simulated inductor can be implemented using a capacitor, two resistors, and one op-amp connected as in Fig. 1.

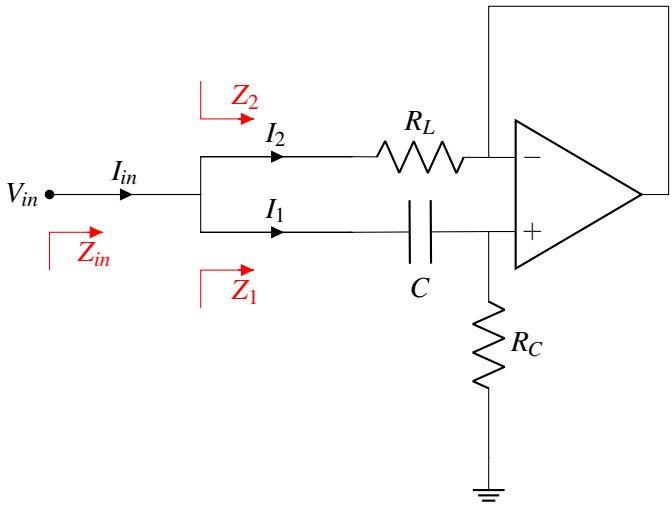


Figure 1: Gyrator

We will show that at low frequencies the simulated inductor in Fig. 1 behaves the same as the equivalent RL circuit in Fig 2.

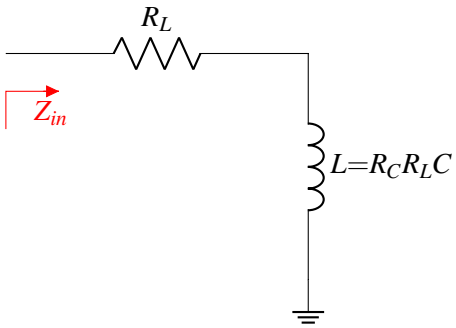


Figure 2: Gyrator - Equivalent RL circuit

The input impedance for the RL circuit in Fig. 2 is given by

$$Z_{in} = R_L + j\omega R_C R_L C = R_L + j\omega L_{eq} \tag{1}$$

where $L_{eq} = R_C R_L C$ is the desired effective inductance of the gyrator circuit.

We will work through the steps to see that these two circuits are equivalent by showing that, under certain conditions, their impedances are the same. In addition, we will show some cases where the gyrator fails.

We can determine the total input impedance Z_{in} in Fig. 1 by solving for the impedance of each branch (Z_1 and Z_2) separately. We then will find Z_{in} by recognizing that the two branches appear in parallel, and thus the input impedance is the parallel of the two branch impedances.

(a) **First, determine the impedance Z_1, which is the impedance of the lower branch**.

(b) **Determine the impedance** Z_2. Hint: Use the properties of an op-amp you have learned. You should find that your answer is of the form $Z_2 = a + b \cdot L_{eq}$ (recall $L_{eq} = R_C R_L C$ is the desired effective inductance).

(c) For the impedance

$$Z_{in} = Z_1 || Z_2$$

what is the approximate effective impedance of Z_{in} **if** $Z_1 \gg Z_2$? Keep the answer in terms of the variables Z_1 and Z_2.

(d) We would ideally like to design the gyrator circuit so that its impedance is given by equation:

$$Z_{in,desired} = R_L + j\omega L_{eq} \tag{2}$$

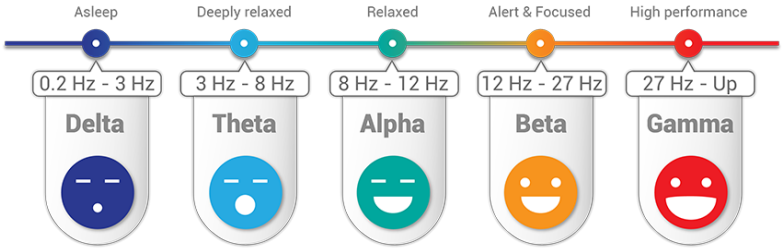
However, we note that Z_{in} is the parallel of Z_1 and Z_2. Using the intuition above, **what design choices can we make for components C, R_C, and/or R_L to ensure that $Z_{in} \approx R_L + j\omega L_{eq}$? What component values can we still freely choose to set the desired L_{eq}?**

(e) Now, let us check under which conditions the two circuits are equivalent (i.e. under which conditions the approximation that $Z_{in} \approx Z_2$ holds). Let V_{in} be a DC voltage, i.e. its frequency is 0. **Are the input impedances for the two circuits equivalent? If not, what is the input impedance for each circuit?**

(f) Let V_{in} be an oscillating cosine with an infinitely large frequency. **Are the input impedances for the two circuits equivalent? If not, what is the input impedance for each circuit?**

5. Biomedical Filter Design (X pts)

Maxwell has been hired to design a biomedical sensor that can detect and output recordings of Alpha brainwaves in the frequency range 8 Hz to 12 Hz. Unfortunately, our sensor is faulty: it is also picking up Gamma brainwaves in the frequency range 40 Hz to 100 Hz, interfering with our ability to get clean recordings of alpha brainwaves. Therefore, he wants to create a new design for our sensor that can remove this interference, giving us a clearer signal.



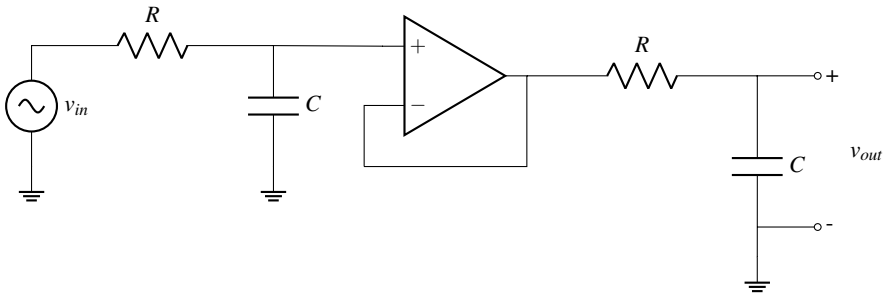
(a) Assuming Max only has access to resistors and capacitors, let us design a filter to remove the Gamma brainwave interference. **Sketch the corresponding circuit and write out its transfer function.**

(b) Max can set the cutoff frequency to 10 Hz, 20 Hz, 32 Hz, 100 Hz, or 120 Hz. Which is the best cutoff frequency, and why?

(c) There is only a 3.3 kΩ resistor in our workstation. **What capacitor value should Max use for our filter?**

(d) Plot the magnitude and phase response of this filter. **How much have we attenuated the Gamma waves at** $f = 40\,\text{Hz}$?

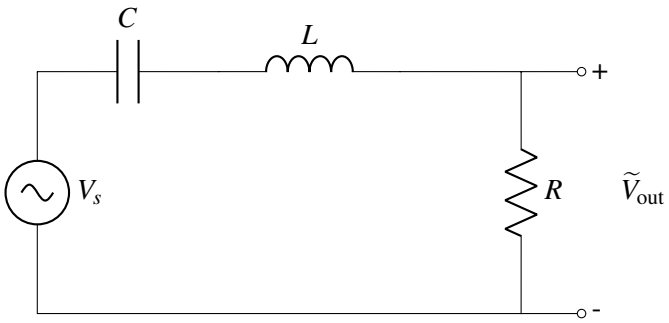
(e) Max consults his friend Taejin for some advice and he suggests to cascade two low-pass filters with the same resistor and capacitor values, with a buffer as shown below:



What is the magnitude of the transfer function $H(\omega)$? In addition, what would happen if we cascaded a large number of filters together?

6. Attack of the Deltas

Maxwell successfully designed his Biomedical sensor to capture the Alpha brainwaves while filtering out the Gamma waves. However, he now notices that there is a another source of interference–Delta brainwaves–in the frequency range 0.5Hz to 4Hz. To combat this, he decides to use a resonance filter.



(a) **What is the transfer function of this filter?**

(b) **Where should Max set the cutoff frequencies?**

(c) **What are the cutoff frequencies of this filter in terms of $R, L,$ and C?**

(d) Let's pick values of $R, L,$ and C to set our cutoff frequencies to those picked in part (b) Suppose you have a $500\,\Omega$ resistor. **What values should you pick for your capacitior and inductor?**

(e) **Plot the frequency response of the filter designed above using the resistor, capacitor and inductor values picked in the previous part.**

(f) Max notices again that while the filter is attenuating the necessary frequencies, it isn't doing that good of a job. **Try plotting the responses using Taejin's idea from the previous question of cascading multiple filters with buffers in between.**

7. Powering a Clock

Taejin is trying to design a clock using a series of inverters made up of transistors. He is currently thinking of two the approaches for a single inverter.

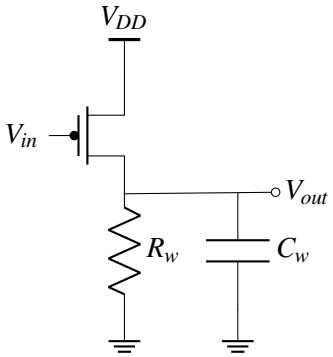


Figure 3: Single PMOS Model

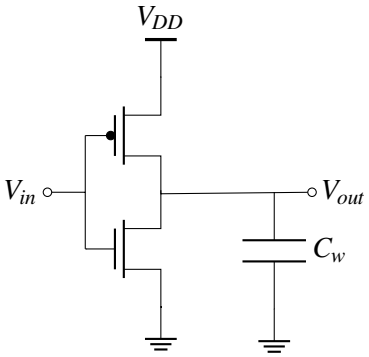
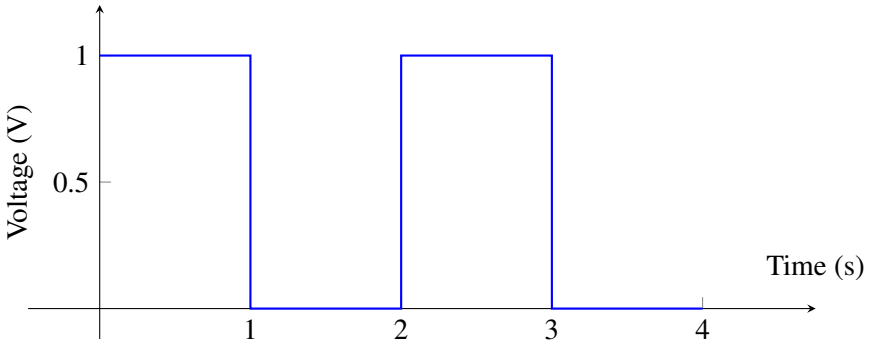


Figure 4: CMOS Inverter Model

Unfortunately both models contain parasitic wire resistance and capacitance $R_w = 500\,\Omega$ and $C_w = 3\,\mu\text{F}$. Both PMOS and NMOS transistors have voltage threshold of $|V_{th}| = 0.7$ and $V_{DD} = 1\,\text{V}$.

To test both models, Taejin decides to give the following square wave input.



(a) Suppose Model A has switch resistance $R_p = 1\,\text{k}\Omega$ and gate capacitance $C_p = 5\,\mu\text{F}$.
Assuming $v_{out}(0) = V_{DD}$, **solve for** $v_{out}(t)$ **for** $T \in [0,2]$ **and plot the response.**

(b) Now suppose Model B has the same PMOS switch resistances and gate capacitances as model A. The NMOS transistor has switch resistance $R_n = 1\,\text{k}\Omega$ and gate capacitance $C_n = 2\,\mu\text{F}$.
Assuming $v_{out}(0) = 0\,\text{V}$, **solve for** $v_{out}(t)$ **for** $T \in [0,2]$ **and plot the response.**

(c) Compare the energy dissipation of both models for $t \in [0,2)$. **Which model dissipates more energy?**

(d) **Compare the individual delays of each inverter over one cycle ($t \in [0,2)$.)**

(e) Taejin now builds his clock by implementing a ring oscillator for both models. He starts both clocks by setting $V_{DD} = 1\,\text{V}$ and $V_{in}(0) = 0\,\text{V}$. For Model A however, he notices that his clock is stuck at a certain value. **Explain why this is the case and how he can fix his clock.**

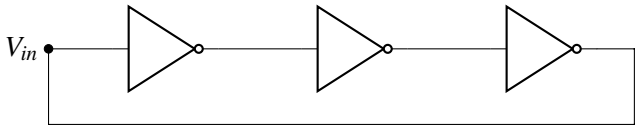


Figure 5: Ring oscillator with 3 inverters

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