Intel to acquire Tower Semiconductor in $5.4 bln deal

Intel Corp agreed to acquire Tower Semiconductor Ltd (TSEM.TA) for an enterprise value of $5.4 billion, the companies said on Tuesday.

Intel will acquire Tower for $53 per share in cash, the statement added.
Recap

• FinFET and FDSOI processes deployed now
  • Expected to be replaced by nanosheets

• Lithography and manufacturing restrict design rules
  • Need to be aware of implications on design
  • EUV entering production

• More changes coming: forksheets, buried power rails, chiplets – 2.5D and 3D
  • Plurality of interconnect standards
MOS Transistor and Gate Delay Models
Modeling Goals

• Models that traverse design hierarchy
• Start with transistor models
• Gate delay models
• Use models to time the design
• Modeling variability

• Based on 251A, approach
  • Start simple
  • Increase accuracy, when needed
Device Models

• Transistor models
  • I-V characteristics
  • C-V characteristics

• Interconnect models
  • R, C, L
  • Covered in EE240A
Transistor Modeling

- Different levels:
  - Hand analysis
  - Computer-aided analysis (e.g. Matlab, Python, Excel,...)
  - Switch-level simulation (some flavors of ‘fast Spice’)
  - Circuit simulation (Hspice)

- These levels have different requirements in complexity, accuracy and speed of computation

- We are primarily interested in delay and energy modeling, rather than current modeling

- But we have to start from the currents...
Transistor Modeling

• DC
  • Accurate I-V equations
  • Well behaved conductance for convergence (not necessarily accurate)

• Transient
  • Accurate I-V and Q-V equations
  • Accurate first derivatives for convergence
  • Conductance, as in DC

• Physical vs. empirical

from BSIM group
Goal for Today

• Develop velocity-saturated model for $I_{on}$ and apply it to sizing and delay calculation
  • Similar approach as in 251A, just use an analytical model
Transistor I-V Modeling

- BSIM
  - Superthreshold and subthreshold models
  - Need smoothening between two regions

- EKV/PSP
  - One continuous model based on channel surface potential
Announcements

• Assignment 1 posted this week
  • No new lab this week

• Project proposals due next Thursday

• No class on Tuesday
Project proposals

• Title: Pick a meaningful title

• Authors, contact e-mail

• ½-page abstract

• 5 references
Long-Channel MOS On-Current
MOS I-V (BSIM)

Start with the basics:

\[ I_{DS} = W C_{ox} (V_{GS} - V_{Th} - V_C(x)) \mu E \]
MOS Currents (32nm CMOS with $L >> 1 \mu m$)

Currents according to the quadratic model
Correct for long channel devices ($L \sim \mu m$)

$I_{DS}[A]$

$V_{DS}[V]$

Quadratic
Simulated 32nm Transistor

$L = 32\text{nm}$

$V_{DS}[\text{V}]$ 

$I_{DS}[\text{A}]$ 

$\sim \text{Linear}$
Simulation vs. Model

Major discrepancies:
  • shape
  • saturation points
  • output resistances
Velocity Saturation
Velocity Saturation

\[ E_C = 2 \frac{v_{sat}}{\mu_{eff}} \]

\[ v_{sat} = 10^5 \text{ m/s} \]

\[ E_C = 1.5 \]

Constant mobility (slope = \( \mu \))

Constant velocity
Modeling Velocity Saturation

• Fit the velocity-dependence curve

\[ v = \frac{\mu_{\text{eff}} E}{\left(1 + \left(\frac{E}{E_C}\right)^n\right)^{1/n}} \]

NMOS: \( n = 2 \)
PMOS: \( n = 1 \)
Modeling Velocity Saturation

• A few approximations: (a) $n \to \infty$, (b) $n = 1$, (c) piecewise
Short-Channel MOS On-Current
Approximation $n \rightarrow \infty$

1) $v = \mu_{eff}E, \quad E < E_C$

$$I_{DS} = \mu_{Cox} \frac{W}{L} \left( (V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2} \right)$$

2) $v = v_{sat}, \quad E > E_C$

$$I_{Dsat} = \mu_{Cox} \frac{W}{L} \left( (V_{GS} - V_{Th})V_{Dsat} - \frac{V_{Dsat}^2}{2} \right)$$

$V_{Dsat} = ?$

Can be reduced to Rabaey DIC model by making $V_{Dsat} = \text{const}$

Is this physically justified?
$I_D = 0$ for $V_{GT} \leq 0$

$I_D = k' \frac{W}{L} \left( V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS})$ for $V_{GT} \geq 0$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma \left( \sqrt{-2\Phi_F + V_{SB}} - \sqrt{-2\Phi_F} \right)$

$\gamma$ - body effect parameter

From Rabaey, 2nd ed.
Unified MOS Model

• Model presented is compact and suitable for hand analysis.

• Still have to keep in mind the main approximation: that $V_{DSat}$ is constant. When is it going to cause largest errors?
  • When does $E$ scale? – Transistor stacks.

• But the model still works fairly well.
  • Except for stacks
Approximation $n = 1$, piecewise

- $n = 1$ is solvable, piecewise closely approximates

\[
v = \begin{cases} 
\frac{\mu_{\text{eff}} E}{1 + E/E_C}, & E < E_C = \frac{2 v_{\text{sat}}}{\mu_{\text{eff}}} \\
v_{\text{sat}}, & E > E_C
\end{cases}
\]

Velocity, $v$: 

Sodini, Ko, Moll, TED’84
Toh, Ko, Meyer, JSSC’88
BSIM model
Drain Current

• We can find the drain current by integrating $I_{DS}$

\[ I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_C(x)) \] v

Linear:

\[ I_{DS} = \frac{\mu C_{ox}}{1 + (V_{DS}/E_C L) \frac{W}{L}} \left( (V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2} \right) \]

In saturation:

\[ I_{DSat} = C_{ox} W \nu_{sat} (V_{GS} - V_{Th} - V_{Dsat}) \]

\[ I_{Dsat} = \frac{\mu C_{ox}}{1 + (V_{Dsat}/E_C L) \frac{W}{L}} \left( (V_{GS} - V_{Th})V_{Dsat} - \frac{V_{Dsat}^2}{2} \right) \]
Drain Current in Velocity Saturation

• Solving for $V_{Dsat}$

\[ V_{Dsat} = \frac{(V_{GS} - V_{Th})E_CL}{(V_{GS} - V_{Th}) + E_CL} \]

And saturation current

\[ I_{Dsat} = \frac{W \mu_{eff}C_{ox}E_CL}{L} \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_CL} \]
Velocity Saturation

\[ I_{DS}[\text{A}] \]

\[ V_{DS}[\text{V}] \]
Velocity Saturation

- $E_C L$ is $V_{GS}$-dependent
- Can calculate $V_{DSat}$ ($V_{Th} \sim 0.4 V$ in 28nm)

<table>
<thead>
<tr>
<th>$V_{GS}$ [V]</th>
<th>0.5</th>
<th>0.6</th>
<th>0.7</th>
<th>0.8</th>
<th>0.9</th>
<th>1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DSat}$ [V]</td>
<td>0</td>
<td>0.05</td>
<td>0.11</td>
<td>0.18</td>
<td>0.25</td>
<td>0.33</td>
</tr>
</tbody>
</table>

- For $V_{GS} - V_{Th} \ll E_C L$, $V_{DSat}$ is close to $V_{GS} - V_{Th}$
- For large $V_{GS}$, $V_{DSat}$ bends upwards toward $E_C L$
- Therefore, $E_C L$ can be sometimes approximated with a constant term
  - But also need to understand the limitation of the approximation
Application of I-V Models
Application of Models: NAND Gate

• 2-input NAND gate

Sizing for equal transitions:
• P/N ratio ($\beta$-ratio): 1 for $L < 20\text{nm}$, 1.6 for $20\text{nm} < L < \sim 65\text{nm}$, 2 for $L > 90\text{nm}$
• Upsizing stacks by a factor proportional to the stack height
Transistor Stacks

• With transistor stacks, $V_{DS}$, $V_{GS}$ reduce.
• Unified model assumes $V_{DSat} = \text{const.}$
• For a stack of two, appears that both have exactly double $R_{ekv}$ of an inverter with the same width
• Therefore, doubling the size of each, should make the pull-down $R$ equivalent to an inverter
Velocity Saturation

• As \((V_{GS} - V_{Th})/E_CL\) changes, the depth of saturation changes

\[
I_{DSat} = \frac{W \mu_{eff} C_{ox} E_CL}{L} \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_CL}
\]

• For \(V_{GS}, V_{DS} = 1.0V, E_CL\) is ~0.75V
• With double length, \(E_CL\) is 1.5V (in this model in 28nm)
• Stacked transistors are less saturated
• \(V_{GS} - V_{Th} = 0.6V, I_{DSat} \sim 2/3\) of inverter \(I_{DSat}\) (64%)
• Therefore NAND2 should have pull-down sized 1.5X
• Check any library NAND2’s
• Current halved in a stack of 3
Note about FinFETs

- Widths are quantized
Example: Logical Effort

• Older CMOS (>90nm)

\[ g_{\text{inv}} = 1 \]

\[ g_{\text{NAND2}} = \]

\[ g_{\text{NOR2}} = \]

• Planar CMOS (~28nm, bulk, FDSOI)

\[ g_{\text{inv}} = 1 \]

\[ g_{\text{NAND2}} = \]

\[ g_{\text{NOR2}} = \]

• FinFET (7nm)

\[ g_{\text{inv}} = 1 \]

\[ g_{\text{NAND2}} = \]

\[ g_{\text{NOR2}} = \]
Other Velocity Saturation Models
Other Models: Alpha Power Law Model

• Simple model, sometimes useful for hand analysis

\[ I_{DS} = \frac{W}{2L} \mu C_{ox} (V_{GS} - V_{Th})^\alpha \]

Parameter \( \alpha \) is between 1 and 2.

Sakurai, Newton, JSSC 4/90
Alpha Power Law Model

• This is not a physical model

• Simply empirical:
  • Can fit (in minimum mean squares sense) to variety of $\alpha$’s, $V_{Th}$
  • Need to find one with minimum square error – fitted $V_{Th}$ can be different from physical
  • Can also fit to $\alpha = 1$
    • What is $V_{Th}$?
$K(V_{GS} - V_{THZ})$ Model ($\alpha = 1$)

Drain current vs. gate-source voltage
# Saturation Current Models

## Model Usage

<table>
<thead>
<tr>
<th>Model</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DS} = K \frac{W}{L} (V_{GS} - V_{TH})$</td>
<td>Delay estimates with $V_{DD} \gg V_{TH}$</td>
</tr>
<tr>
<td>$I_{DS} = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_{TH})^2$</td>
<td>Long channel devices (rare in digital)</td>
</tr>
<tr>
<td>$I_{DS} = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_{TH})^\alpha$</td>
<td>Delay estimates in a wider range of $V_{DD}$’s</td>
</tr>
<tr>
<td>$I_{DS} = \frac{W}{L} \mu C_{ox} \left( (V_{GS} - V_{TH}) V_{Dsat} - \frac{V_{Dsat}^2}{2} \right)$</td>
<td>Easy to remember, does not handle stacks correctly</td>
</tr>
<tr>
<td>$I_{DS} = \frac{W}{L} \mu C_{ox} \frac{E_{CL}}{2} \frac{(V_{GS} - V_{TH})^2}{(V_{GS} - V_{TH}) + E_{CL}}$</td>
<td>Handles stacks correctly, sizing</td>
</tr>
</tbody>
</table>
Next Lecture

• Delay models