Universal Chiplet Interconnect Express (UCle) Announced: Setting Standards For The Chiplet Ecosystem
March 2, 2022, AnandTech

To that end, today Intel, AMD, Arm, and all three leading-edge foundries are coming together to announce that they are forming a new and open standard for chiplet interconnects, which is aptly being named Universal Chiplet Interconnect Express, or UCle.

www.uciexpress.org
Recap

• Standard cell architectures depend on technology, maximize density-performance-power

• Standard cell library
  • Delay is tabulated, dependent on slope, load
Design for Performance

Flip-Flop-Based Timing
Example Clock System
Clock Nonidealities

• Clock skew
  • Spatial variation in temporally equivalent clock edges; deterministic + random, $t_{SK}$

• Clock jitter
  • Temporal variations in consecutive edges of the clock signal; modulation + random noise
    • Cycle-to-cycle (short-term) - $t_{JS}$
    • Long-term - $t_{JL}$

• Variation of the pulse width
  • for level-sensitive clocking
Clock Skew and Jitter

- Both skew and jitter affect the effective cycle time
- Only skew affects the race margin, if jitter is from the source
  - Distribution-induced jitter affects both
Clock Uncertainties

Sources of clock uncertainty

1. Clock Generation
2. Devices
3. Interconnect
4. Power Supply
5. Temperature
6. Capacitive Load
7. Coupling to Adjacent Lines
Flip-Flop Parameters

Delays can be different for rising and falling data transitions
Delays can be different for rising and falling data transitions

Unger and Tan
Trans. on Comp.
10/86
Clock Constraints in Edge-Triggered Systems

\[ t_{CL} \leq t_{CY} - t_{SK} - t_{JS} - (t_{SU} + t_{CQ}) \]

\[ t_{CL} \geq t_{SK} + (t_{H} - t_{CQ}) \]

Pictorial View of Setup and Hold Tests

- Setup time
- Hold time
- Late slack
- Early slack
- Actual early AT
- Actual late AT
- Early RAT
- Late RAT
- Data must be stable
- Latest clock arrival time
- Earliest clock arrival time (next cycle)
- 0 or more switching(s) allowed
- Early RAT
- Late RAT
- Data must be stable

Data must be stable

ICCAD '07 Tutorial
Chandu Visweswariah
Latch Timing
Key Point

• Latch-based sequencing can improve performance, but is more complicated
  • Timing analysis not limited to a consecutive pair of latches
Latch Timing

When data arrives to transparent latch

Latch is a ‘soft’ barrier

When data arrives to non-transparent latch

Data has to be ‘re-launched’
Latch Sequencing

Logic

Logic

Clk1

Clk2
Latch-Based Timing

• Single-phase, two-latch

As long as transitions are within the assertion period of the latch, no impact of position of clock edges
Latch Design and Hold Times

\[ t_{\text{CLL}} \geq t_{\text{SK}} + (t_H - t_{CQ}) \]

Diagram showing the timing relationships between inputs and outputs of latches.
Soft-Edge Properties of Latches

• **Slack passing** – logical partition uses left over time (slack) from the *previous* partition

• **Time borrowing** – logical partition utilizes a portion of time allotted to the *next* partition

• Makes most impact in unbalanced pipelines

Bernstein et al, Chapter 8, Chandrakasan, Chap 11 (by Partovi)
Slack Passing and Time Borrowing

![Diagram showing read and write operations with timing notations](image)
Slack Passing and Time Borrowing

- Slack passed

Diagram showing timing relationships and slack passed.
Slack Passing and Time Borrowing

- Time borrowed
Slack-Passing and Cycle Borrowing

For N stage pipeline, overall logic delay should be < N Tcl
Announcements

• Assignment #1 due tomorrow
  • Quiz 1 next Tuesday, in lecture

• Lab 5 due next week
Design for Performance

Latch Design
Review: MUX

• 2-input MUX
Review: Transmission Gates

![Transmission Gate Diagram]
Generating Complementary Clocks
Latch vs. Flip-Flop

(a) Latch

(b) Flip-flop

Latches

Transmission-Gate Latch

C\textsuperscript{2}MOS Latch

Usually without contention
Latches

(a) The transparent high latch (THL)

(b) The transparent low latch (TLL)

(c) Timing waveforms for the THL.

Design for Performance

Delay, Setup, Hold
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data

Clock

\( T_{\text{Setup-1}} \)

\( t=0 \)

\( T_{\text{Clk-Q}} \)

\( D \)

\( D_1 \)

\( CN \)

\( CP \)

\( S_M \)

\( Q_M \)

\( \text{Inv1} \)

\( \text{Inv2} \)

\( \text{TG1} \)
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

Hold-1 case

Hold-1 case diagram with timing relationships.

Clock, Data, and Timing relationships for Hold-1 case.
Setup-Hold Time Illustrations

Hold-1 case

Clk-Q Delay

Data

Clock

Time

T_{Hold-1}

T_{Clk-Q}

D

Q_M

Inv1

Inv2

TG1

CN

SM

CP

D_1

S

Inv1

Inv2

TG1

CN

SM

CP

D

0

T_{Hold-1}

Time

T_{Clk-Q}

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Setup-Hold Time Illustrations

Hold-1 case

Clock  Data

Time

$T_{Hold-1}$

$T_{Clk-Q}$

$D$

$CN$

$CP$

$Q_M$

$D_1$

$S_M$

$Inv1$

$Inv2$

$TG1$

$S$

$M$

$Q$

$M$

Setup-Hold Time Illustrations
Setup-Hold Time Illustrations

Hold-1 case

Clock

Data

Time

$T_{Hold-1}$

$T_{Clk-Q}$
Setup-Hold Time Illustrations

Hold-1 case

[Diagram showing a circuit with labels for D, Inv1, TG1, CP, S_M, CN, Inv2, Q_M, Clock-Q Delay, T_{Hold-1}, and T_{Hold} with time axis labeled.]
More Precise Setup Time

\[
\begin{aligned}
t_D &= t_c^2 \\
Q &= 1.05(t_c^2) \\
Su &= t_{\text{clk-q}} \\
F_{d-\text{clk}} &= t_{H} + t_{\text{clk-q}}
\end{aligned}
\]
Latch $t_{D-Q}$ and $t_{Clk-Q}$
\[ t_{\text{setup}} \]
Summary

• Flip-flop-based (edge-triggered) timing dominates today

• Latch-based timing can increase performance, but needs extra care

• There is also asynchronous design

• Logical effort can be used to analyze latch timing
Next Lecture

• Flip-flops
• Variability