Universal Chiplet Interconnect Express (UCIe) Announced: Setting Standards For The Chiplet Ecosystem
March 2, 2022, AnandTech

To that end, today Intel, AMD, Arm, and all three leading-edge foundries are coming together to announce that they are forming a new and open standard for chiplet interconnects, which is aptly being named Universal Chiplet Interconnect Express, or UCIe.

www.uciexpress.org

Recap

• Standard cell architectures depend on technology, maximize density-performance-power

• Standard cell library
  • Delay is tabulated, dependent on slope, load
Design for Performance
Flip-Flop-Based Timing

Example Clock System

Clock Nonidealities

• Clock skew
  • Spatial variation in temporally equivalent clock edges; deterministic + random, $t_{SK}$

• Clock jitter
  • Temporal variations in consecutive edges of the clock signal; modulation + random noise
  • Cycle-to-cycle (short-term) - $t_{JS}$
  • Long-term - $t_{JL}$

• Variation of the pulse width
  • for level-sensitive clocking

Clock Skew and Jitter

- Both skew and jitter affect the effective cycle time
- Only skew affects the race margin, if jitter is from the source
  • Distribution-induced jitter affects both
Clock Uncertainties

Sources of clock uncertainty

Flip-Flop Parameters

Delays can be different for rising and falling data transitions
Latch Parameters

Delays can be different for rising and falling data transitions

Clock Constraints in Edge-Triggered Systems
Pictorial View of Setup and Hold Tests

Data must be stable

Hold time

Latest clock arrival time

Early RAT

Late RAT

0 or more switching(s) allowed

Actual early AT

Actual late AT

Early slack

Late slack

Setup time

Earliest clock arrival time (next cycle)

Latch Timing
Key Point

• Latch-based sequencing can improve performance, but is more complicated
  • Timing analysis not limited to a consecutive pair of latches

Latch Timing

When data arrives to transparent latch
Latch is a ‘soft’ barrier

When data arrives to non-transparent latch
Data has to be ‘re-launched’
Latch Sequencing

D Q
Clk

Logic

D Q
Clk

D Q
Clk

Logic

D Q
Clk

D Q
Clk

Latch-Based Timing

• Single-phase, two-latch

As long as transitions are within the assertion period of the latch, no impact of position of clock edges
Soft-Edge Properties of Latches

- **Slack passing** — logical partition uses left over time (slack) from the previous partition
- **Time borrowing** — logical partition utilizes a portion of time allotted to the next partition
- Makes most impact in unbalanced pipelines
Slack Passing and Time Borrowing

- Slack passed
Slack Passing and Time Borrowing

- Time borrowed

For N stage pipeline, overall logic delay should be < N Tcl
Announcements

• Assignment #1 due tomorrow
  • Quiz 1 next Tuesday, in lecture
  • Lab 5 due next week

Design for Performance
Latch Design
Review: MUX

- 2-input MUX

Review: Transmission Gates
Generating Complementary Clocks

Latch vs. Flip-Flop

(a) Latch

(b) Flip-flop

Latches

Transmission-Gate Latch

\[ D \rightarrow Q \] (a) The transparent high latch (THL)

\[ D \rightarrow Q \] (b) The transparent low latch (TLL)

(c) Timing waveforms for the THL

Design for Performance
Delay, Setup, Hold

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data $T_{\text{Setup-1}}$ Clock

$D$ $S_M$ $Q_M$

Inv1 TG1 Inv2

$C_N$ $D_1$

$C_P$

$t=0$

Clk-Q Delay

Time

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data $T_{\text{Setup-1}}$ Clock

$D$ $S_M$ $Q_M$

Inv1 TG1 Inv2

$C_N$ $D_1$

$C_P$

$t=0$

Clk-Q Delay

Time
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data $\rightarrow$ Clock

Time}

$t=0$

Clk-Q Delay

Time $\rightarrow$

T$_{Setup-1}$
Setup-Hold Time Illustrations

Hold-1 case

Clock

Data

Clk-Q Delay

THold-1

Time

Setup-Hold Time Illustrations

Hold-1 case

Clock

Data

Clk-Q Delay

THold-1

Time
Setup-Hold Time Illustrations

Hold-1 case

Clock

Data

Time

D

Inv1

Inv2

CN

TG1

CP

0

Clk-Q Delay

Time

Setup-Hold Time Illustrations

Hold-1 case

Clock

Data

Time

D

Inv1

Inv2

CN

TG1

CP

0

Clk-Q Delay

Time
Setup-Hold Time Illustrations

Hold-1 case

(Time)

Data

Clock

T_Hold-1

D

Inv1

Inv2

TG1

CP

0

Q

M

S

Clk-Q Delay

T_{Clk-Q}

Setup-Hold Time Illustrations

Hold-1 case

Data

Clock

T_Hold-1

D

Inv1

Inv2

TG1

CP

0

Q

M

S

Clk-Q Delay

T_{Clk-Q}

More Precise Setup Time

Clk

D

Q

T_{clk-q}

1.05(T_{clk-q})

T_{d-clk}

EECS251B L13 TIMING 41

EECS251B L13 TIMING 42
Latch $t_{D-Q}$ and $t_{Clk-Q}$
Summary

- Flip-flop-based (edge-triggered) timing dominates today
- Latch-based timing can increase performance, but needs extra care
- There is also asynchronous design
- Logical effort can be used to analyze latch timing

Next Lecture

- Flip-flops
- Variability