Recap

- Logical effort can be used to analyze latch timing
- Clk-Q, D-Q delays are \(~1\)FO4 delay (with F=1)
\[ t_{\text{clk-q}} = 2.7 t_s + 2.2 t_u \]

Flip-Flops
Key Point

- Two ways to design a flip-flop
  - Latch pair (large majority)
  - Pulsed latch

Latch vs. Flip-Flop

(a) Latch

(b) Flip-flop

Flip-Flops

- Performance metrics
- Delay metrics
  - Insertion delay
  - Inherent race immunity
  - ‘Softness’ (Clock skew absorption)
  - Inclusion of logic
  - Small (+constant) clock load
- Power/Energy Metrics
  - Power/energy
- Design robustness
  - Noise immunity
Types of Flip-Flops

Latch Pair

Pulse-Triggered Latch

Flip-Flop (Latch Pair) Clk-Q, setup, hold
Flip-Flop Timing Characterization

- Combinational logic delay is a function of output load and input slope.
- Sequential timing (flip-flop):
  - $t_{clk-q}$ is a function of output load and clock rise time.
  - $t_{su}$, $t_{h}$ are functions of $D$ and $Clk$ rise/fall times.

Pulse-Triggered Latches

- First stage is a pulse generator
  - Generates a pulse (glitch) on a rising edge of the clock.
- Second stage is a latch
  - Captures the pulse generated in the first stage.
- Pulse generation results in a negative setup time.
- Frequently exhibit a soft edge property.

- Note: power is always consumed in the pulse generator
  - Often shared by a group (register).
Pulsed Latch

Simple pulsed latch

(a) Sub-nano Pulse Generator

(b) Pulse Register

Kozu, ISSCC’96

Intel/HP Itanium 2

Latch

Pulse Generator

Scan Circuitry

Naffziger, ISSCC’02
Pulsed Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC’96

1-0 and 0-1 transitions at the input with 0ps setup time
Hybrid Latch Flip-Flop

Skew absorption

Pulsed Latches

7474, from mid-1960's
Pulsed Latches

DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to high, when \( Clk = 0 \)
After rising edge of the clock sense amplifier generates the pulse on
S or R
The pulse is captured in S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges

Sense Amplifier-Based Flip-Flop

Announcements

• Lab 5 due this week
• Midterm reports due next week
  • 4 pages, conference format
• Assignment 2 posted this week
Design Variability Sources and Impact on Design

Variability Classification

- Nature of process variability
  - Within-die (WID), Die-to-die (D2D), Wafer-to-wafer (W2W), Lot-to-lot (L2L)
  - Systematic vs. random
  - Correlated vs. non-correlated

- Spatial variability/correlation
  - Device parameters (CD, $t_{ox}$, …)
  - Supply voltage, temperature

- Temporal variability/correlation
  - Within-node scaling, Electromigration, Hot-electron effect, NBTI, self-heating, temperature, SOI history effect, supply voltage, crosstalk
  - [Bernstein, IBM J. R&D, July/Sept 2006]

- Known vs. unknown
  - Goal of model-to-hw correlation is to reduce the unknowns
Sources of Variability

• Technology
  • Front-end (Devices)
    • Systematic and random variations in Ion, Ioff, C, ...
  • Back-end (Interconnect)
    • Systematic and random variations in R, C

• Environment
  • Supply (IR drop, noise)
  • Temperature

Spatial Variability

Global
- Fab to fab
- Deployed environment
- Lot to lot

Local
- Temperature
- Metal polishing
- Transistor $I_{on}$, $I_{off}$
- Line-edge roughness
- Dopant fluctuation
- Film thickness
- Across wafer
- Across reticle
- Across chip
- Across block

After Rohrer
ISSC’06 tutorial

Spatial range [m]
### Temporal Variability

#### Technology
- Tech. node scaling
- Within-node scaling

#### Environment
- Temperature
- Data stream
- Electromigration
- NBTI
- Hot carrier effect
- SOI history effect
- Self heating
- Tooling changes
- Lot-to-lot
- Supply noise
- Coupling
- Charge

**After Rohrer ISSCC'06 tutorial**

![Temporal range [s]](chart)

### Systematic vs. Random Variations

- **Systematic**
  - A systematic pattern can be traced down to lot-to-lot, wafer-to-wafer, within reticle, within die, from layout to layout,…
  - Within-die: usually spatially correlated

- **Random**
  - Random mismatch (dopant fluctuations, line edge roughness,…)
  - Things that are systematic, but e.g. change with a very short time constant (for us to do anything about it). Or we don’t understand it well enough to model it as systematic. Or we don’t know it in advance (“How random is a coin toss?”).

- **Unknown**
### Systematic and Random Device Variations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Random</th>
<th>Systematic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Dopant Concentration Nch</td>
<td>Affects $\sigma_{VT}$ (^{(1)})</td>
<td>Non uniformity in the process of dopant implantation, dosage, diffusion</td>
</tr>
<tr>
<td>Gate Oxide Thickness Tox</td>
<td>Si/SiO$_2$ &amp; SiO$_2$/Poly-Si interface roughness (^{(2)})</td>
<td>Non uniformity in the process of oxide growth</td>
</tr>
<tr>
<td>Threshold Voltage $V_T$ (non Nch related)</td>
<td>Random anneal temperature and strain effects</td>
<td>Non-uniform annealing temperature (^{(3)}) (metal coverage over gate) Biaxial strain</td>
</tr>
<tr>
<td>Mobility $\mu$</td>
<td>Random strain distributions</td>
<td>Systematic variation of strain in the Si due to STI, S/D area, contacts, gate density, etc</td>
</tr>
<tr>
<td>Gate Length L</td>
<td>Line edge roughness (LER) (^{(3)})</td>
<td>Lithography and etching: Proximity effects, orientation (^{(3)})</td>
</tr>
<tr>
<td>Fin geometry/ film thickness variations</td>
<td>Rounding, etc, $\sigma_{VT}$, mobility</td>
<td>Systematic fin thickness Systematic Si film/BOX variations</td>
</tr>
</tbody>
</table>

---

### Dealing with Systematic Variations

- **Model-to-hardware correlation classifies unknown sources**

  - **Systematic effect**

    - **Improve process**
      - Limited options
      - Density loss
    - **Tighten a design rule**
      - Model/Design-in
      - Extraction/Compact modeling/Design techniques
Systematic (?) Temporal Variability

Metal 3 resistance over 3 months

Impact of Correlations
Chip Yield Depends on Inter-Gate Correlation

Yield = Pr (sum of n delays < clock period)

\( \rho = 0 \) gives highest yield through averaging

Non-correlated gates in a path reduce impact of variation

Bowman et al, JSSC, Feb 2002.

Chip Yield Depends on Inter-Path Correlation

Yield = Pr (max delay of K paths < clock period)

K = 1 gives highest yield

Correlated paths reduce impact of variation

Bowman et al, JSSC, Feb 2002.
Process Corners

Design Variability
Some Systematic Effects
Layout: Poly Proximity Effects

• Gate CD is a function of its neighborhood

![Diagram showing gate length and proximity effects]

Gate length depends on

- Light intensity profile falling on the resist
- Resist: application of developer fluid\(^1\), post exposure bake (PEB) temperature\(^2\)
- Dry etching: microscopic loading effects\(^3\)

\(^1\) J. Cain, M.S. Thesis, UC Berkeley
\(^2\) D. Steele et al., SPIE, vol.4689, July 2002.

Layout: Proximity Test Structures

• 90nm experiments

- Single gate inverter layout
- Dummy poly
- Stacked gates

L.T. Pang, VLSI'06

• 45nm experiments

- No single gates allowed
- Ring oscillators and individual transistor leakage currents

L.T. Pang, CICC'08
Results: Single Gates in 90nm

- Max $\Delta F$ between layouts $> 10\%$
- Within-die $3\sigma/\mu \sim 3.5\%$, weak dependency on density

Results: Single Gates in 45nm

- Weak effect on performance. $\Delta F \sim 2\%$
- Small shifts in NMOS leakage and bigger shifts in PMOS leakage
Impact of Stress

Vertical compressive strain
Parallel tensile strain

> 45nm STM process: Wafer rotated <100> - higher PMOS mobility
> NMOS strained through capping layer
> Subatmospheric STI – weak tensile stress

- Strongest effect measured in 45nm, $\Delta F \sim 5\%$
- No significant shift in $I_{\text{LEAK}}$

Impact of Longer Diffusion in 45nm

- Fastest chip
- Slowest chip
- 22 chips from 2 wafers

- Strongest effect measured in 45nm, $\Delta F \sim 5\%$
- No significant shift in $I_{\text{LEAK}}$
Impact of Shallow Trench Isolation (STI)

- ΔF ~ 3%, small changes in I_{LEAK}
- Due to STI-induced stress

Design Variability
Some Random Effects
Random Dopant Fluctuations

- Number of dopants is finite

Frank, IBM J R&D 2002

Processing: Line-Edge Roughness

- Sources of line-edge roughness:
  - Fluctuations in the total dose due to quantization
  - Resist composition
  - Absorption positions
  Effect:
  - Variation (random) in leakage and power
Transistor Matching

- $V_{Th}$ matching of geometrically identical transistors varies with size $\sim \sqrt{WL}$ and distance.

![Graph showing $\sigma_{VT}$ vs. $1/\sqrt{WL}$]

Pelgrom parameter $A_{VT}$
- Scales with technology (EOT)
- $A_{VT}$ in FDSOI technology


Negative Bias Temperature Instability

- PFET $V_{Th}$'s shift in time, at high negative bias and elevated temperatures
- The mechanism is thought to be the breaking of hydrogen-silicon bonds at the Si/SiO2 interface, creating surface traps and injecting positive hydrogen-related species into the oxide.
- Also other charge trapping and hot-carrier defect generation
- Systematic + random shifts

![Graph showing $\Delta V_{th}$ vs. time]

Tsujikawa, IRPS'2003
Random Telegraph Signal (RTS)

- Trapping of a carrier in oxide traps modulates $V_{th}$ or $I_{ds}$
- $\tau_e$ and $\tau_c$ are random and follow exponential distributions


RTS and Technology Scaling

- RTS exceeds RDF at 3 sigma with 20nm gates

\[
\Delta V_{th, RTS} \sim \frac{1}{WL}
\]

\[
\Delta V_{th, RDF} \sim \frac{1}{\sqrt{WL}}
\]

Tega et al, VLSI Tech. 09
Summary

- Flip-flops:
  - Latch pairs
  - Pulse triggered
- Variability
  - Systematic
  - Random

Next Lecture

- Memories