Broadcom launches Wi-Fi 7 chips

**Recap**
- Limiting transistor leakage
- Multi-threshold designs
- Transistor stacking
- Sleep modes
- Power gating

**Dynamic Body Bias**
- Similar concept to dynamic voltage scaling
- Control loop adjusts the substrate bias to meet the timing/leakage goal
  - Can be used just as runtime/sleep
  - Limited range of threshold adjustments in bulk (<100mV)
  - Limited leakage reduction (<10x)
  - Works well in FDSOI (80-85mV/V, with ~1.8V range)
  - No delay penalty
  - Can increase speed by forward bias
  - Energy cost of charging/discharging the substrate capacitance
    - but doesn’t need a regulator

**FDSOI and Bulk**
- Bulk CMOS
- Leakage paths through bulk
- RDF dominates local variability
- Diodes and B2B tunneling limit back-bias range

**FDSOI Wells and Back Bias**
- Flip-well (LVT)
  - \( V_{DD}, \text{nom} = G_{NDS}, \text{nom} = 0V \)
  - Forward body bias \( V_{BSN} > 0V \)
  - \( 0.3V < G_{NDS} < (3V) \)
  - Can forward bias 2-3V each
- Typical (RVT)
  - \( V_{DD}, \text{nom} = G_{NDS}, \text{nom} = V_{DD} \)
  - Reverse body bias \( V_{BSN} < 0V \)
  - \( (-3V) < G_{NDS} < V_{DD}/2+0.3V \)
  - Can reverse bias 2-3V each

**Back-Bias in FDSOI**
- \( \gamma = 8.5mV/V \) body coefficient, and extended voltage range
  - Lower coefficient and voltage range in bulk, FinFET

**Multi \( V_{Th} \)**
- No channel implant in 2B-FDSOI
- No multi \( V_{Th} \)
- Can’t abut wells
- RVT and LVT require different well biases
**Back Bias in FDSOI**

- Triple well (deep N-Well, DNW) allows for separate back bias
- Layout penalty; capacitance to drive

**Digital Logic - Implementation**

- Well taps added explicitly
- Difference from bulk

**Dynamic Body Bias (Bulk)**

- **Active mode**
  - Forward body bias (FBB)
  - Local $V_{CC}$ tracking

- **Idle mode**
  - Reverse body bias (RBB)
  - Triple well needed

**Generating Back-Bias**

- Tradeoff – speed of charging and discharging well caps
- Often measure $V_{BB}$ indirectly (leakage)
- Challenge: Generating $-V_{SS}$

**Body Bias Layout**

- Sleep transistor LBGs
- ALU core LBGs

**Total Active Power Savings**

- (Fixed activity: $a = 0.05$)

- Reference: 450mV FBB to core with clock gating, 1.28V, 4.05GHz, 75°C

**Digital Logic: UPF**

- Supply, back-bias defined in Unified Power Format (UPF)
- Or Common Power Format (CPF)
- Handled by synthesis, place and route tools

```
create_power_domain PD_TOP
create_supply_port GND
create_supply_port VDD
create_supply_net GND -domain PD_TOP
connect_supply_net GND -ports {GND}
create_supply_net VDD -domain PD_TOP
connect_supply_net VDD -ports {VDD}
set_domain_supply_net PD_TOP -primary_power_net VDD -primary_ground_net GND

# Body-bias specification
create_supply_port VDDS
create_supply_port GNDS
create_supply_net VDDS -domain PD_TOP
connect_supply_net VDDS -ports {VDDS vddgndvdds*/VDDSCORE}
create_supply_net GNDS -domain PD_TOP
connect_supply_net GNDS -ports {GNDS gnds*/VDDCORE1V8}
create_supply_set back_bias_set 
  -function {nwell VDDS} 
  -function {pwell GNDS} 
  -reference_gnd {GND} 
create_power_domain PD_TOP -update -supply bias
associate_supply_set back_bias_set -handle PD_TOP.bias
```

**EECS251B L22 OPTIMAL THRESHOLDS**

- Digital Logic: UPF
- Dynamic Body Bias (Bulk)
- Body Bias Layout
Generating Back Bias

* Fast and wide voltage range back-bias in FDSOI

Switched capacitors generate negative bias and pump substrate

Supply/Process Compensation

* Able to track ~200mV supply droops and maintain constant frequency (measured by a replica) by back-bias adjustments

Dynamic Frequency Loop in FDSOI

Announcements

* Quiz 3 today
* Homework 4 due next week

Dynamic Voltage Scaled Microprocessor

Adapting $V_{DD}$ and $V_{TH}$

* Adapting both $V_{DD}$ and $V_{TH}$ during runtime
  * $V_{TH}$ is much less sensitive

Adapting $V_{DD}$ and $V_{TH}$

Miyazaki, ISSCC'02
Optimal $V_{DD}$, $V_{th}$

- Adjusting $V_{DD}$, $V_{th}$ trades of energy and delay
- We studied energy-limited design
  - And alternate ways for optimizing energy and delay together
  - E.g. energy-delay product (EDP)
  - Or $E^*P^*$, $n,m > 1$

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- E.g. energy-delay product (EDP)
- Or $E^*P^*$, $n,m > 1$

Optimal EDP Contours

- Plot of EDP curves in $V_{DD}$, $V_{th}$ plane

$V_{DD}$, $V_{th}$

- Large variation in optimal circuit parameters $V_{DD}^{opt}$, $V_{th}^{opt}$

Technology parameters ($V_{DD}^{max}$, $V_{th}^{min}$) rarely optimal

Sizing, Supply, Threshold Optimization

<table>
<thead>
<tr>
<th>Reference Design: $D^{ref}$ ($V_{DD}^{max}$, $V_{th}^{ref}$)</th>
<th>Topology</th>
<th>Inverter</th>
<th>Adder</th>
<th>Decoder</th>
</tr>
</thead>
<tbody>
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Large variation in optimal circuit parameters $V_{DD}^{opt}$, $V_{th}^{opt}$

Energy-constrained delay

- Active power $P_{act} = \alpha f CV_{DD}^2$
  $f = 1/\tau_D$
- Leakage power $P_{leak} = I_d \theta S V_{DD}$
- Eliminate one variable ($V_{in}$) and find $P_{max}(V_{DD})$

Nose, ASP-DAC'00

Optimal EDP Contours

- Plot of EDP curves in $V_{DD}$, $V_{th}$ plane

Energy efficient curve $f (W/V_{DD}, V_{th})$

Minimum energy: $E_{Sw} = 2 E_{Lk}$

- Large $(E_{Lk}/E_{Sw})^{opt}$
- Flat $E_{Sw}$ minimum
- Topology dependent

$E_{Sw}^* = \frac{2}{ln(\theta_{avg})}$

Optimal designs have high leakage $(E_{Lk}/E_{Sw} = 0.5)$

Summary

- Body effect weak in bulk CMOS
  - Strong in FDSOI
- Dynamic threshold scaling
  - Primarily for leakage control, process compensation
- Optimal thresholds
  - Total energy is minimized with 1/3 being leakage

Subthreshold Optimum

- $f = 30kHz$
- Minimum is independent of $V_{th}$

Result: E-D Tradeoff in an Adder

- 80% of energy saved without delay penalty
- 40% delay improvement without energy penalty

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Next Lecture

- Clock generation and distribution