Recap

• Basics of phase-locked loops
• Digital PLLs

Delay-Locked Loops

- First order loop: inherently stable
- No filtering of input jitter
- Constant frequency (no synthesis)
- No phase error accumulation

Delay-Locked Loop

- Open loop transfer function
  \[ \frac{D_o(s)}{D_i(s)-D_o(s)} = \frac{K_D}{S} \]
  \[ \text{Open loop gain} \]

- Closed loop transfer function
  \[ H(s) = \frac{ \frac{D_o(s)}{D_i(s)} }{ \frac{1}{s} + K_D K_P K_{DL} } = \frac{K_D K_P K_{DL}}{s + K_D K_P K_{DL}} \]
  \[ \text{Closed loop transfer function} \]

Delay-Locked Loop

- DLL Locking
- Use of DLLs requires low-jitter input
- VCDL must span adequate delay range + reset to min delay
- Noise sources:
  - Delay line (Supply sensitivity)
  - Clock buffer that follow
  - Device noise (Jitter)

Clock Generation

Delay-Locked Loop (Delay Line Based)

Phase-Locked Loop (VCO/DCO-Based)
Announcements

• Final is in-class 4/28
  • 80min, 9:40am-11:10am
• Project presentations 5/5
  • 9am – 12:30pm
  • BWRC
  • 12min + 3min Q&A

Clock Distribution

Example (Older) Clock System

• IBM Power 4

Clock Grid

One PLL with multiple DLLs

• Single PLL, and two cores vary frequency through digital frequency dividers (DFDs) and DLLs
  • SLCB: Second-Level Clock Buffer
  • CVD: Clock Vernier Device – fine (static) delay tuning

Clock Domain Synchronization

<table>
<thead>
<tr>
<th>Type</th>
<th>Frequency</th>
<th>Phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synchronous</td>
<td>Some</td>
<td>Some</td>
</tr>
<tr>
<td>Mesochronous</td>
<td>Some</td>
<td>Constant offset</td>
</tr>
<tr>
<td>Plesiochronous</td>
<td>Small difference</td>
<td>Mostly varying</td>
</tr>
<tr>
<td>Asynchronous</td>
<td>Different</td>
<td>Arbitrary</td>
</tr>
</tbody>
</table>
Deskew System (Mesochronous)

- Deskew System

- Deskew Buffer
  - Essentially a DLL to align regional clock with ref. clock

- Clock Subsystem
  - Intel Xeon – Bowhill, ISSCC’15
  - Independent clocks for 4-18 cores
  - Self-biased (SB) and LC PLLs

- Clock Domain Crossings
  - Bowhill, ISSCC’15

- Brute-Force Synchronizer
  - Cascaded flip-flops reduce the probability of metastability

- Clock Crossing FIFOs
  - FIFO for clock crossings

Supply Generation

Supply Generation

- Linear
  - Series or shunt
  - Linear regulation
  - Quiet
  - Inefficient (unless Vin-Vout is small)

- Switching (Capacitive)
  - Limited efficiency
  - Poor regulation
  - Voltage ripples

- Switching (Magnetic)
  - Efficient
  - Require external components
  - Noisy

Linear vs. Switching Regulators

Efficiency:

\[ K = \frac{V_{out}}{V_{in}} \cdot R_{load} \]

Linear Voltage Regulator

- Negative feedback sets low supply resistance
- Voltage regulated to desired level

E.g. IBM Power7 has 48 linear regulators

Switching Supply

- Buck Converter

- Pulse-Width Modulation (PWM) regulates \( V_{out} \)

Inside Haswell

Integrated VR Technology

- Chiplet/Cell Architecture: 20 die
- Architecture supports 80 efficiency curve
- Fine grain power management
- Modifies its in-house voltage rails
- Tolerance and margining features
- Active Voltage Positioning for current sharing and SMPS
- Control features, including TRIM, PRM, TSV/BIST

Inductive Supply

- 16 phases per power cell, 220 phases per chip
- High phase count reduces noise, ripple
- High granularity
- Cell matching
- Bridge shedding

- BIST
  - Self-test and characterization system
- Synthesis/lookup for testing control & 100C
- MC Bus Register/interfacing

Intel Broadwell

- Inductors moved to a small PCB

Switched-Capacitor Supply

- Interleaving reduces ripple, but lowers efficiency
What happens with supply when load changes?

Power Delivery

- Typical model

Supply Resonances

- First droop
  - Package L + on-die C
- Second droop
  - Motherboard + package decoupling
- Third droop
  - Board capacitors

Clock and Supply

- First droop
- Second droop
- Third droop

How to model

- Abstracted delay line

Droop Detection

- Hashimoto, JSSC 4/18

Summary

- DLLs are used for phase alignment, deskewing
- Modern SoCs are globally asynchronous, locally synchronous
- Supply regulators
- Clock and supply interact
Next Lecture
• Wrap-up