Recap
• Technology affects circuit design
  • Optimized for standard cell, SRAM density
  • Recent scaling not uniform per layer
• Lithography restricts layer orientation, length quantization
  • Favors layout regularity
  • Has implications on variability
• FinFETs add more restrictions (width quantization)

Lithography Implications

Litho (4): Restricted Design Rules (~45nm Node)

Litho (5): Phase-Shift Masks
* Phase Shifting Masks (PSM)
  * Creates interference fringes on the wafer → Interference effects boost contrast → Phase Masks can make extremely small lines

Litho (6): Double Patterning
* Double exposure double etch
  * Double exposure double etch
  * Pitch split, litho-etch-litho-etch (LELE)
* Self-aligned methods
  * Self-aligned double patterning
  * Self-aligned quadruple patterning

Double-Exposure Double-Etch

32nm Examples

SRAM image from K. Mistry, IEDM'07

IEDM'08
Pitch-Split Double Exposure

Starting layout

Split pattern

Overlay

Also called litho-etch-litho-etch (LELE)

Self-Aligned Double Patterning (SADP)

SADP: Double patterning

Two litho-defined lines to form four fins

SADP: Quadruple patterning

Litho: Design Implications

• Forbidden directions
  • Depends on illumination type
  • Poly lines in other directions can exist but need to be thicker

• Forbidden pitches
  • Nulls in the interference pattern
  • Multiple patterning
  • Forbidden shapes in PSM, multiple-patterning

• Assist features
  • If a transistor doesn’t have a neighbor, let’s add a dummy

Litho: Current Options (Beyond 10nm)

• Multiple patterning
  • NA ~ 1.2-1.35

• EUV lithography
  • \[ \lambda = 13.5 \text{nm} \]

<table>
<thead>
<tr>
<th>Normalized wafer cost adder²</th>
<th>SE</th>
<th>LEELE</th>
<th>SADP</th>
<th>EUV SE</th>
<th>EUV SADP</th>
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<td>Cost adder reduced with increased power/throughput of EUV</td>
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Some of the Process Features (Designer’s Perspective)

1. Shallow-trench isolation
2. High-k/Metal-gate technology
3. Strained silicon
4. Thin-body devices (28nm, and beyond)
5. Copper interconnects with low-k dielectrics

Modern Bulk/finFET/FDSOI processes

1. Shallow Trench Isolation
  • Less space needed for isolation
  • Some impact on stress

2. Hi-k/Metal gate

Replacement gate technology (Intel)
3. Strained Silicon

High Stress Film

Compressive channel strain 30\% drive current increase in 90nm CMOS

Tensile channel strain 10\% drive current increase in 90nm CMOS

Intel's Strained Si Numbers

Performance gains:

<table>
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<th>65 nm</th>
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<td>PMOS</td>
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<td>55%</td>
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</table>

S. Thompson, VLSI'06 Tutorial

5. Thin-Body Devices

- 28nm FDSOI
- 22/14nm finFET

2012 2017

FinFETs and gate P/N sizing

- The use of strain closes the gap between N and P on currents to $\sim 1:1$
- No strain
- Strained planar Si
- FinFET

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5. FinFETs

- FinFET scaling
- Track scaling

N. Planes, VLSI'2012
C. Auth, VLSI'2012

5. FDSOI

2012 2013 2014 2015 2016 2017

28FD-SOI (STMicroelectronics)
28FD-SOI (Samsung)
22FDX (GLOBALFOUNDRIES)
12FDX (GLOBALFOUNDRIES)
18FDX (Samsung)
5. Interconnect

Interconnect: CMP

- Cu interconnect: Dual damascene process
- Metal density rules (20%-80%)
- Slotting rules
- Also: Antenna rules

DRAM Scaling

- DRAM density scaling:
  - Transistor
  - Cap
  - Integration

Flash Scaling

- Density and architecture scaling

Die Size Trend

- To increase functionality and performance, die sizes have been increasing
  - Yield, cost tradeoffs

Chiplets

Migration to Chiplets

- Split the product into multiple dies
- Some or mixed technologies
- Increase functionality, performance @ lower cost
- Mix technologies

2D Chiplet Interfaces

- High-density interfaces have been evolving over the past decade
Interconnect Density Scaling

- Bump density and BW/edge or BW/area

Today's core

- On-chip integration: 25x
- Tech-scaling: 50x
- Packaging: 2x
- Scale-out: 400x

Scaling is scale-out ... Getting to 1M cores/system

Some Open Issues

- High-value (e.g. hyperscale) products are driving the chiplet technology
- What about sub-150mm² dies?

Chiplets are not for free

Cost of disintegration:
- AIB 1.0: 12mm² in 16nm @ $0.1/mm² = $1.2 on each side
  55nm wafers are $15k - chiplet interface is 2 x $4
  Substrate cost: $10 (could be $100)
  Test escape issues
  Sum: $25+ (but can be $100)

Can they offset the NRI cost? Make medium volume ASICs affordable?

Summary

- FinFET and FDSOI processes deployed now
- Expected to be replaced by nanosheets
- Lithography and manufacturing restrict design rules
- Need to be aware of implications on design
- EUV entering production
- More changes coming: forksheets, buried power rails, chiplets – 2.5D and 3D
- Plurality of interconnect standards

Next Lecture

- Transistor models, gate sizing