SRAM Peripheral Circuits
Peripheral Circuits in SRAM

• Decoders (and pre-decoders)
• Column circuitry: read, write, multiplex, mask
• Write assist techniques
• Read assist techniques
• Redundancy
• BIST
• ECC
• Power management
SRAM Array

• SRAM periphery:
  • Decoders (covered in EECS251A)
  • Bitline design and sense-amps
Sense-Amp Trigger

- Sense-amp trigger needs to be timed carefully
  - Too early: Incorrect evaluation
  - Too late: Unnecessary timing margin

- Problem: Delay based on inverter chains does not track the delay of the memory cell
Aside: Delay Lines, Replicas and Time Amplification

- We will encounter it several times in this course
  - Used in a wide range of mixed-signal circuits

- A simple delay line

![Diagram of a simple delay line](image-url)

Time-to-digital converter (TDC)

Start-Stop difference read out as a thermometer-coded binary value

Resolution set by inverter delay

Sub-inverter delays are hard to generate

Small $\alpha$ requires large area

Lee, Abidi, JSSC 4/08
Sense-Amp Triggering

• Replica bitline

Replica delay tracks better across corners
But still mistracks across a wide range of supplies
Amrutur, Horowitz, JSSC 8/98
Time Amplification

- Time amplified through metastability (by using setup time characteristics)

Lee, Abidi, JSSC 4/08
Voltage Scaling: Multiplicative Replica Bitline

• Conventional replica

\( n \) replica cells discharging replica BL in parallel to reduce the current/cell variation by \( \sqrt{n} \)

Threshold for discharge is set accordingly to \( V_{DD} - nV_{os} \)

Limits \( n \) to \(~2-4\)

Niki, JSSC'11
Voltage Scaling: Multiplicative Replica Bitline

- **Multiplicative replica**
  - Programmable replica delay
  - Multiplicative replica scales the delay, w/o increasing variance correspondingly

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Forward path digitizes SAEi to CK delay
Backward path multiplies

Niki, JSSC'11
Redundancy and ECC
Redundancy and ECC

• Redundancy
  • Spare columns (or rows)
  • Selected at test via eFuse
  • Possible to dynamically program redundancy

• ECC
  • Error detection/correction codes
  • Parity
  • SECDED
  • DECTED
Redundancy

• Principle

Rows


Columns

McPartland, CICC’00.
Redundancy

• Effectiveness (Bickford, 2008)

Figure 1: Modeled Yield impact comparison for 65 nm SRAM complier. Vmin cell fail rate used in analysis shown in the left chart is 5.10 sigma. Vmin cell fail rate used in the analysis shown in the right chart is 5.20 sigma. 147 Kbit segment is a standardized array size block segment used for comparison purposes.
Soft Errors

• From packaging and cosmic rays

• Packaging:
  • Lead ore contains Po-210 -> (5 days) -> Bi-210 -> (22.3 years) -> Pb-210
  • Or Po-210 -> (138.4 days) -> Pb-210
  • Need ‘old lead’

• Cosmic rays
  • Large particles collide with Earth’s atmosphere to produce alpha (and other) particles
Error Correction

• Parity – Single Error Detection (SED)
  • \( p = d_7 \oplus d_6 \oplus d_5 \oplus d_4 \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \)

• Single Error Correction Double Error Detection (SECDED)
  • Hamming codes with additional parity

• Double Error Correction Triple Error Detection (DECTED)
  • BCH codes – higher decoding complexity
Multi-bit Errors

Multi-bit Errors

Kawahara, ISSCC’07 tutorial
Multi-bit Errors

Equivalent circuits of 16 SRAM cells between well tap

- SRAM cell
- Nc=16
- Well tap

No failure
Bipolar action
Failure
No failure

Simulation
Max. no. of errors per cosmic-ray strike

Nc is the number of cells between well taps.

Measured
Ratio of multiple to single errors (%)

Well tap/16 cells
Parasitic bipolar effect

Peak neutron energy: 63.5 MeV

Well tap/cell

Ref.: K. Osada et. al., [11]
Multi-bit Errors: Interleaving

Placement at alternate addresses

Multi-error B
Word<0> A0 A1 A0 A1 A0 A1
Word<1> A2 A3 A2 A3 A2 A3
Word<2> A4 A5 A4 A5 A4 A5
Word<3> A6 A7 A6 A7 A6 A7
Word<4> A8 A9 A8 A9 A8 A9

Multi-error A
2 to 1 2 to 1 2 to 1
S.A. S.A. S.A.

Memory cell
Soft-error bit
Data: 128 bit Parity: 10 bit

Data is not corrected
All data is corrected

Ref.: K. Osada et al., [12].

Neutron peak energy: 63.5 MeV
Total fluency: 6.14 x 10⁹/cm²

w/o ECC
This work
-99.5%
6T SRAM Alternatives
8T-SRAM

- Dual-port read/write capability (register-file-like cells)
- \( N_0, N_1 \) separates read and write
  - No Read SNM constraint
  - Half-selected cells still undergo read
- Stacked transistors reduce leakage

L. Chang, *VLSI Circuits* 2005
eDRAM

- Process cost: Added trench capacitor

Barth, ISSCC'07, Wang, IEDM'06
Crosspoint Memories

• Barrett, IRE Trans. Comp. 1961.

Fig. 2—Memory structure. $I_1$ and $I_2$ are access drive currents to core-selection switch. Presence or absence of a magnet over a twistor-strip solenoid crosspoint yields a “zero” or “one.” Signals observed between twistor and return wire.
Crosspoint Memories

- Neale, Nelson, Moore, Electronics’70
  - 16 x 16 array (256b) of ‘read-mostly memory’
Crosspoint Memory

• Four modes
  • Form
  • Set
  • Reset
  • Read

Endurance
3D Crosspoint Arrays

- Kau, IEDM’09
- Yeh, JSSC’15
- Ou, JSSC’11
Crosspoint Arrays

• Read and sneak currents

Bae, TED 4/17
Summary

• SRAM periphery
  • Decoders
  • Assist circuits
  • Sense amp timing replicas

• 6-T SRAM alternatives
  • 8-T SRAM
  • eDRAM
  • Crosspoint arrays (e.g. RRAM)