UNIVERSITY OF CALIFORNIA, BERKELEY
Department of Electrical Engineering and Computer Sciences

EE251B Advanced Digital Circuits and Systems

Spring 2024, Prof. Borivoje Nikolic
Homework 1

Issued: Thursday January 25, 2024
Due: Friday February 2, 2024

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1 SystemVerilog Assertions (50 %)

(a) Explain (in regular English) what condition each of the following assertions checks for:

i. `assert property (!(mem_read && mem_write));`

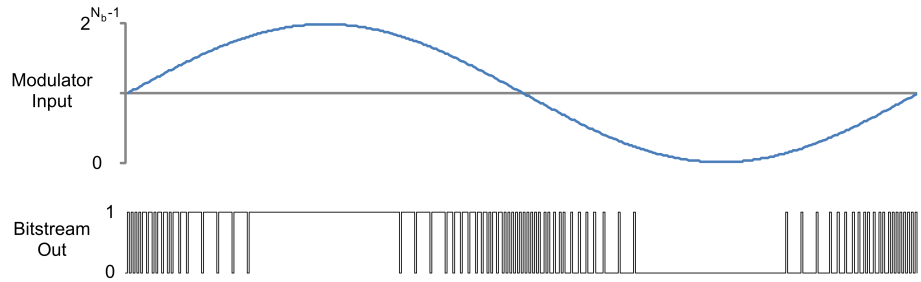
ii. `assert property (@(posedge clk) ready |-> ##1 valid);`

iii. `assert property (@(posedge clk) ready |=> valid);`

iv. `assert property (@(posedge clk) ready |-> ##[1:2] valid);`

v. `assert property (@(posedge clk) disable iff (rst) not sel[0] ##1 sel[1]);`

(b) A delta-sigma modulator is a common digital signal processing block that can be used to make a simple digital to analog converter using an FPGA output pin and an external RC filter. It converts a sequence of digital codes into a fast-switching bitstream, which can then be converted into a smooth analog signal by a lowpass filter. For example, here is a bitstream produced from a digitally sampled sine wave played back through a delta-sigma modulator:



One common implementation of a delta-sigma modulator is called the error feedback structure. An error feedback modulator works by taking an unsigned `input` vector of width `N` and adding it to an `N`-bit accumulator register on every clock cycle. The clock-synchronous carry-out from this addition is the bitstream. The clock runs at a much faster rate than the input update rate, allowing each digital input code to generate a long sequence of output bits with the correct average value. Write a parameterized Verilog module that implements this structure. Include a synchronous `reset` signal that sets the state of all registers to zero.

Write a SystemVerilog assertion or assertions that check for the correct behavior of the accumulator and bitstream on each clock cycle. Make sure to include the `reset` signal.

Write a SystemVerilog coverage statement that detects whether the bitstream changes value during a verification simulation.

2 System Interconnect (50 %)

You have been tasked with building a system interconnect for a system-on-chip with 1024 processing cores. You are considering several options for the on-chip system interconnect network:

i. 32-ary 2-mesh

ii. 32-ary 2-cube

iii. 16-ary 2-Cmesh4

iv. 32-ary 3-fly Clos

The application requires a packet size of 2048 bits.

(a) Calculate the required number of bits per unidirectional channel, for each network option, such that each of the networks can support the ideal throughput of 128 bits/cycle/core under uniform random traffic.

Hints: Start by calculating the total throughput of the network, then find the bisection bandwidth and number of unidirectional bisection channels for each network. Express all numerical answers in terms of integer powers of 2.

(b) Show the worst-case zero-load latency breakdown for each interconnect network. Independent of your calculations above, assume the following:

- The flit size is 64 bits and all channel widths are matched to that flit size.
- Assume that the latency of each channel (core-to-router or router-to-router) is 1 cycle.
- Assume the latency of each router to be 2 cycles.