UNIVERSITY OF CALIFORNIA, BERKELEY
Department of Electrical Engineering and Computer Sciences
EE251B Advanced Digital Circuits and Systems

Spring 2024, Prof. Borivoje Nikolic
Homework 4

Issued: Thursday, April 4, 2024
Due: Friday, April 12th, 11:59pm

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1 SRAM assists (50 %)

Consider a conventional 6-T SRAM cell, sized to be stable at nominal operating conditions. The cell is a part of a conventional, precharged bitline array. We would like to operate it at a reduced supply voltage, so we are considering assist techniques. Let's analyze the effect of peripheral signals on the operation of the cell. One-sentence answers, please!

(a) How does increased wordline voltage affect the read stability of the cell?

(b) How does increased wordline voltage affect the read access time of the cell?

(c) How does increased wordline voltage affect the writeability of the cell?

(d) How does decreased cell supply voltage (without changing other signal levels) affect the writeability of the cell?

2 SRAM yield (50 %)

We will analyze a 4 MiB = 2^{22} B SRAM array, consisting of 256 x 256 bit subarrays. Two columns share one sense amplifier. Bitline capacitance is 2 pF and the supply is 1.8 V. For this problem, assume that all the SRAM cells in the array are identical (i.e. not affected by the random process variation) and $I_{on} = 400\,\mu A, I_{off} = 100\,nA$. Assume that the target access time of 1 ns is dominated by the bitline discharge.

If the sense amplifier offset has normal distribution, with zero mean and standard deviation of 30 mV, would you expect this array to have a high yield? How many redundant columns would need to be added per subarray to have at least 99% yield for the whole 4 MiB SRAM array (note that you may not have to do the exact calculation of this)?