UNIVERSITY OF CALIFORNIA, BERKELEY
Department of Electrical Engineering and Computer Sciences
EE251B Advanced Digital Circuits and Systems

Spring 2024, Prof. Borivoje Nikolic
Homework 4

Issued: Thursday, April 4, 2024
Due: Friday, April 12th, 11:59pm

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1 SRAM assists (50 %)

Consider a conventional 6-T SRAM cell, sized to be stable at nominal operating conditions. The cell is a part of a conventional, precharged bitline array. We would like to operate it at a reduced supply voltage, so we are considering assist techniques. Let's analyze the effect of peripheral signals on the operation of the cell. One-sentence answers, please!

(a) How does increased wordline voltage affect the read stability of the cell?

It decreases read stability since the access transistors are activated more strongly relative to the feedback transistors.

(b) How does increased wordline voltage affect the read access time of the cell?

It decreases read access time since the access transistors will be activated more strongly, reducing the effective resistance and the resulting RC delay on the bitlines.

(c) How does increased wordline voltage affect the writeability of the cell?

It increases writability since the pull-down strength of the access transistors are increased relative to the pull-up strength of the feedback transistors.

(d) How does decreased cell supply voltage (without changing other signal levels) affect the writeability of the cell?

It increases the writeability of the cell since the strength of the cross-coupled inverters is decreased.

2 SRAM yield (50 %)

We will analyze a 4 MiB = 2^{22} B SRAM array, consisting of 256 x 256 bit subarrays. Two columns share one sense amplifier. Bitline capacitance is 2 pF and the supply is 1.8 V. For this problem, assume that all the SRAM cells in the array are identical (i.e. not affected by the random process variation) and $I_{on} = 400\,\mu A, I_{off} = 100\,nA$. Assume that the target access time of 1 ns is dominated by the bitline discharge.

If the sense amplifier offset has normal distribution, with zero mean and standard deviation of 30 mV, would you expect this array to have a high yield? How many redundant columns would need to be added per subarray to have at least 99% yield for the whole 4 MiB SRAM array (note that you may not have to do the exact calculation of this)?

First, we compute the number of sense amps present in the array. We have $2^{22} \cdot 2^3 = 2^{25}$ bits in the entire SRAM array. Each subarray has $2^8 \cdot 2^8 = 2^{16}$ bits, meaning the array has $2^{25}/2^{16} = 2^9$

subarrays. Since 2 columns share a sense amp, each subarray has $2^8/2 = 2^7$ sense amps. In total, we have $2^9 \cdot 2^7 = 2^{16}$ sense amps.
We now find the yield per sense amp. The worst case voltage offset occurs when the I_{off} of all bitcells in the column counteract the I_{on} of the desired bitcell. As such, the differential bitline voltage can be computed as

$$\Delta V = t_{read}(I_{on} - 255I_{off})/C_{BL} = 187\,\text{mV}.$$

For a single sense amp to work, its offset magnitude must be smaller than ΔV. This gives a yield per sense amp of

$$1 - 2 \cdot \text{normalcdf}(\mu = 0, \sigma = 30\,\text{mV}, -187\,\text{mV}) = 1 - 2 \cdot 2.33 \times 10^{-10}.$$

The total yield of this array is given by taking the yield per sense amp to the power of the total number of sense amps:

$$(1 - 2 \cdot 2.33 \times 10^{-10})^{2^{16}} = \boxed{0.999969}.$$

The array has high yield and does not need any redundant columns. An interesting exercise is to see how many sense amps you would need before the yield drops below 99%.