UNIVERSITY OF CALIFORNIA, BERKELEY
Department of Electrical Engineering and Computer Sciences

EE251B Advanced Digital Circuits and Systems

Spring 2024, Prof. Borivoje Nikolic
Homework 5

Issued: Monday April 15, 2024
Due: Tuesday April 23, 2024

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1 DVFS (50 %)

Plot the energy per clock cycle for a digital block in highly-scaled CMOS with DVFS and the specifications listed below and determine the combination of clock frequency and supply voltage that leads to minimum total energy per clock cycle using RVT (regular threshold), LVT (low threshold), and HVT (high threshold) standard cells. Which type of standard cell should you use to create the most energy-efficient version of the design?

The block parameters are:

- $C_{\text{eff}} = 100\,\text{pF}$ (effective switching capacitance of the digital block)
- $V_{\text{dd,nom}} = 1.0\,\text{V}$
- $V_{\text{th,RVT}} = 0.3\,\text{V}$, $V_{\text{th,LVT}} = 0.27\,\text{V}$, $V_{\text{th,HVT}} = 0.33\,\text{V}$.
- Assume that the leakage power is 20% of the dynamic power at a nominal clock frequency of 1 GHz at $V_{\text{dd,nom}}$ with RVT transistors, and that leakage current is 3x higher with LVT transistors and 3x smaller with HVT transistors.
- Assume that the gate delay in this block follows the alpha power-law model with $\alpha = 1.3$ and the DVFS controller reduces the nominal clock frequency as V_{dd} decreases, by an amount that is proportional to the change in gate delay (*hint*: see slide 24 of lecture 21 on low-power design for an example of this type of calculation).

Submit your code along with the plot. We are expecting 9 answers for this question to receive full credit – (1) plots of f_{clk} and energy/cycle vs. supply voltage, (2) code listing, (3-8) numerical answers optimum V_{dd} and f_{clk} for each standard cell type, and (9) type of standard cell that produces the most energy-efficient design.

2 Power Gating (50 %)

A digital circuit block has the following parameters:

- $C_{\text{eff}} = 150\,\text{pF}$ (effective switching capacitance for average dynamic power)
- $C_{\text{rail}} = 300\,\text{pF}$ (supply rail capacitance)
- $I_{\text{peak,dyn}}/I_{\text{avg,dyn}} = 2$ (peak to average current ratio)
- $I_{\text{leak}} = 0.25 \times I_{\text{avg,dyn}}$ (leakage current is 25% of average dynamic switching current)
- $f_{\text{clk}} = 2\,\text{GHz}$
- $V_{\text{dd,nom}} = 1.2\,\text{V}$

(a) Design a high-side power gate that has a maximum voltage droop of 5% of $V_{\text{dd,nom}}$. Assume that $R_{\text{on,n}} = 1.0\,\text{k}\Omega\text{-}\mu\text{m}$ and $R_{\text{on,p}} = 1.5\,\text{k}\Omega\text{-}\mu\text{m}$.

(b) Determine the energy pulled from the supply to switch the power gate. Assume $C_{\text{g}} = 2\,\text{fF}/\mu\text{m}$.

(c) Determine the energy discharged from the block after the power gate is turned off. Assume that the supply rail capacitance is the capacitance of the virtual (i.e. gated) supply rails.

(d) Determine the minimum off time for the block at which the leakage savings break even with the energy required to switch the power gate and re-charge the virtual rails.