**UNIVERSITY OF CALIFORNIA, BERKELEY**

Department of Electrical Engineering and Computer Sciences

# EE251B Advanced Digital Circuits and Systems

Spring 2024, Prof. Borivoje Nikolic  
Homework 5 Solution

Issued: Monday April 15, 2024  
Due: Tuesday April 23, 2024

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## 1 DVFS (50 %)

Plot the energy per clock cycle for a digital block in highly-scaled CMOS with DVFS and the specifications listed below and determine the combination of clock frequency and supply voltage that leads to minimum total energy per clock cycle using RVT (regular threshold), LVT (low threshold), and HVT (high threshold) standard cells. Which type of standard cell should you use to create the most energy-efficient version of the design?

The block parameters are:

- $C_{\text{eff}} = 100 \, \text{pF}$ (effective switching capacitance of the digital block)

- $V_{\text{dd,nom}} = 1.0 \, \text{V}$

- $V_{\text{th,RVT}} = 0.3 \, \text{V}$, $V_{\text{th,LVT}} = 0.27 \, \text{V}$, $V_{\text{th,HVT}} = 0.33 \, \text{V}$.

- Assume that the leakage power is 20% of the dynamic power at a nominal clock frequency of $1 \, \text{GHz}$ at $V_{\text{dd,nom}}$ with RVT transistors, and that leakage current is 3x higher with LVT transistors and 3x smaller with HVT transistors.

- Assume that the gate delay in this block follows the alpha power-law model with $\alpha = 1.3$ and the DVFS controller reduces the nominal clock frequency as $V_{\text{dd}}$ decreases, by an amount that is proportional to the change in gate delay (*hint*: see slide 24 of lecture 21 on low-power design for an example of this type of calculation).

Submit your code along with the plot. We are expecting 9 answers for this question to receive full credit – (1) plots of $f_{\text{clk}}$ and energy/cycle vs. supply voltage, (2) code listing, (3-8) numerical answers optimum $V_{\text{dd}}$ and $f_{\text{clk}}$ for each standard cell type, and (9) type of standard cell that produces the most energy-efficient design.

<span style="color:red">MATLAB code listing:</span>

```
%% Cleanup
clc; close all; clear;

%% Make plot

% Plot formatting
fs = 12;
lw = 1.5;

% Setup sweeps
fclk_vec = 1e9 * linspace( 0.1, 3.0, 100 );
```

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```matlab
% Block parameters
Ceff = 100e-12;
Vdd_nom = 1.0;
fclk_nom = 1e9;
leakage_factor_nom = 0.2;
alpha = 1.3;

% Setup standard cell types
rvt.name = 'RVT';
rvt.Vth = 0.3;
rvt.leakage_multuplier = 1;

lvt.name = 'LVT';
lvt.Vth = 0.27;
lvt.leakage_multuplier = 3;

hvt.name = 'HVT';
hvt.Vth = 0.33;
hvt.leakage_multuplier = 1/3;

std_cells = { lvt, rvt, hvt };

fig = figure( );

% Run and plot calculations for each standard cell type
for ind = 1 : length( std_cells )
    std_cell = std_cells{ ind };

    name = std_cell.name;
    Vth = std_cell.Vth;
    leakage_factor = leakage_factor_nom * std_cell.leakage_multuplier;

    % Start at Vth -- this model doesn't go to subthreshold regime
    Vdd_vec = Vth : 0.001 : Vdd_nom;

    % Clock scaling based on alpha power law
    tdelay_scaling_vec = Vdd_vec / Vdd_nom .* ...
        ( Vdd_nom - Vth ).^alpha ./ ( Vdd_vec - Vth ).^alpha;
    fclk_vec = fclk_nom ./ tdelay_scaling_vec;

    % Energy/operation calculations
    Edyn = Ceff * Vdd_vec.^2;
    Ileak_nom = leakage_factor * fclk_nom * Ceff * Vdd_nom;
    Eleak = Ileak_nom .* Vdd_vec ./ fclk_vec;
    Etot = Edyn + Eleak;

    % Find the min energy point
    [ Eopt, ind_opt ] = min( Etot );
    std_cells{ ind }.E_opt = Eopt;
    std_cells{ ind }.fclk_opt = fclk_vec( ind_opt );
    std_cells{ ind }.Vdd_opt = Vdd_vec( ind_opt );

    % Print the optimal point
    disp( [ name ' standard cell optimal point:' ] );
    disp( [ 'Energy/op = ' num2str( 1e12 * std_cells{ ind }.E_opt, '%.0f' ) ' pJ' ] );
    disp( [ 'Vdd = ' num2str( std_cells{ ind }.Vdd_opt, '%.2f' ) ' V' ] );
```

```matlab
        disp( [ 'fclk = ' num2str( 1e-6 * std_cells{ ind }.fclk_opt, '%.1f' ) ' MHz' ] );

        % Plot the DVFS and energy curves
        subplot( 2, 1, 1 ); hold all; grid on;
        set( gca, 'ColorOrderIndex', ind );
        plot( Vdd_vec, 1e-9 * fclk_vec, 'LineWidth', lw, 'DisplayName', name );
        plot( std_cells{ ind }.Vdd_opt, 1e-9 * std_cells{ ind }.fclk_opt, ...
            'ro', 'LineWidth', lw, 'HandleVisibility', 'off' );

        subplot( 2, 1, 2 ); hold all; grid on;
        set( gca, 'ColorOrderIndex', ind );
        plot( Vdd_vec, 1e12 * Etot, 'LineWidth', lw, 'DisplayName', name );
        plot( std_cells{ ind }.Vdd_opt, 1e12 * std_cells{ ind }.E_opt, ...
            'ro', 'LineWidth', lw, 'HandleVisibility', 'off' );
end

% Common plot formatting
subplot( 2, 1, 1 );
xlabel( 'V_{dd} [V]' );
ylabel( 'f_{clk} [GHz]' );
legend( 'location', 'best' );
set( gca, 'fontsize', fs );

subplot( 2, 1, 2 );
xlabel( 'V_{dd} [V]' );
ylabel( 'Energy/Cycle [pJ]' );
set( gca, 'fontsize', fs );
ylim( [ 0, 200 ] );

% Save as vector graphic
set( fig, 'Units', 'Inches' );
pos = get( fig, 'Position' );
set( fig, 'PaperPositionMode', 'Auto', 'PaperUnits', 'Inches', ...
    'PaperSize', [ pos( 3 ), pos( 4 ) ] );
print( fig, '-dpdf', 'outputs/pr1_sol.pdf', '-r0' );
```

Script output:
LVT standard cell optimal point:
Energy/op = 92 pJ
Vdd = 0.51 V
fclk = 458.5 MHz
RVT standard cell optimal point:
Energy/op = 50 pJ
Vdd = 0.47 V
fclk = 338.0 MHz
HVT standard cell optimal point:
Energy/op = 33 pJ
Vdd = 0.45 V
fclk = 227.3 MHz

The HVT standard cells produce the most energy-efficient design, with $\approx 3\times$ energy savings compared to LVT at the cost of $\approx 2\times$ slower clock frequency for the optimized settings of the two. The left side of the plot is leakage energy dominated and the right side is dynamic energy dominated.
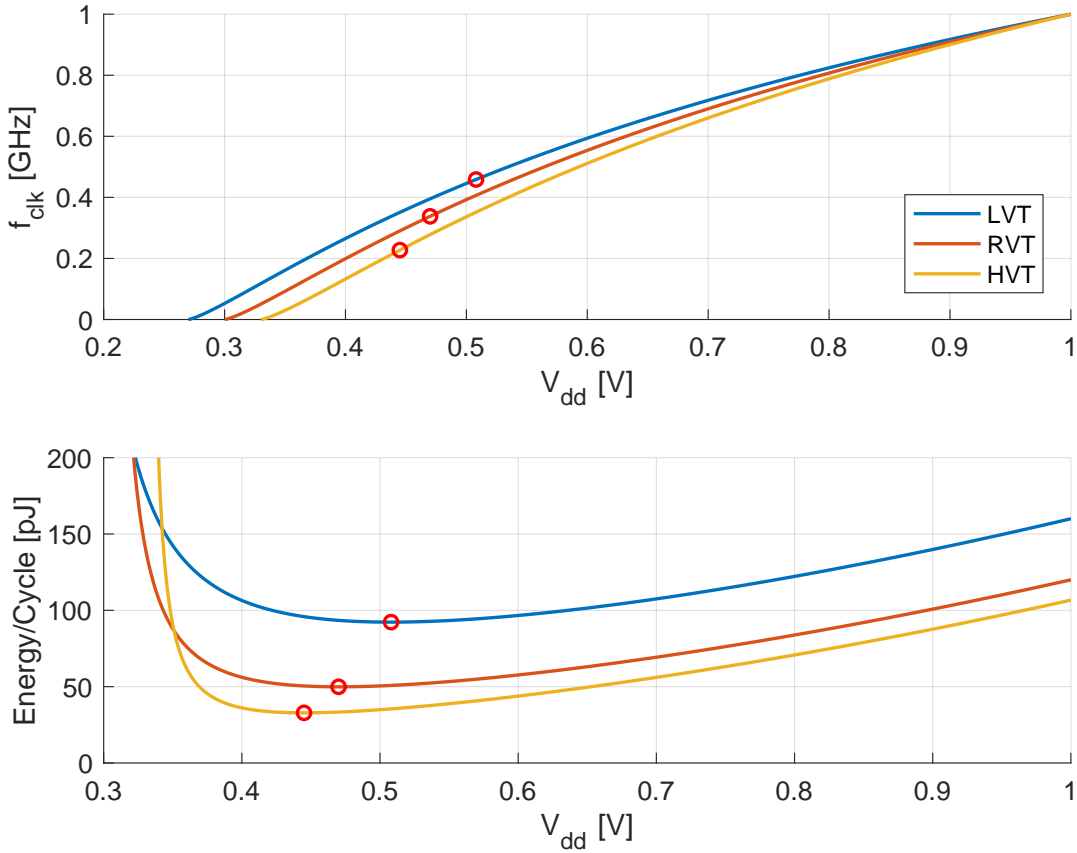
## 2   Power Gating (50 %)

A digital circuit block has the following parameters:

- $C_{\text{eff}} = 150\,\text{pF}$ (effective switching capacitance for average dynamic power)

- $C_{\text{rail}} = 300\,\text{pF}$ (supply rail capacitance)

- $I_{\text{peak,dyn}}/I_{\text{avg,dyn}} = 2$ (peak to average current ratio)

- $I_{\text{leak}} = 0.25 \times I_{\text{avg,dyn}}$ (leakage current is 25% of average dynamic switching current)

- $f_{\text{clk}} = 2\,\text{GHz}$

- $V_{\text{dd,nom}} = 1.2\,\text{V}$

(a) Design a high-side power gate that has a maximum voltage droop of 5% of $V_{\text{dd,nom}}$. Assume that $R_{\text{on,n}} = 1.0\,\text{k}\Omega\text{-}\mu\text{m}$ and $R_{\text{on,p}} = 1.5\,\text{k}\Omega\text{-}\mu\text{m}$.

$$I_{\text{avg,dyn}} = P_{\text{avg,dyn}}/V_{\text{dd,nom}} = (C_{\text{eff}} \times V_{\text{dd,nom}}^2 \times f_{\text{clk}})/V_{\text{dd,nom}} = 0.36\,\text{A}$$

$$I_{\text{peak,dyn}} = 2 \times I_{\text{avg,dyn}} = 0.72\,\text{A}$$

$$I_{\text{leak}} = 0.25 \times 0.36\,\text{A} = 0.09\,\text{A}$$

$$\Delta V = 60\,\text{mV} \rightarrow R_{\text{pg}} = \Delta V/(I_{\text{peak,dyn}} + I_{\text{leak}}) = 74.1\,\text{m}\Omega$$

$$W_{\text{pg}} = R_{\text{on,p}}/R_{\text{pg}} = 20,200\,\mu\text{m}$$

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(b) Determine the energy pulled from the supply to switch the power gate. Assume $C_{\text{g}} = 2\,\text{fF}/\text{µm}$.

$$C_{\text{pg}} = W_{\text{pg}} \times C_{\text{g}} = 40.4\,\text{pF}$$
$$E_{\text{pg}} = C_{\text{pg}} \times V_{\text{dd,nom}}^2 = 58\,\text{pJ}$$

(c) Determine the energy discharged from the block after the power gate is turned off. Assume that the supply rail capacitance is the capacitance of the virtual (i.e. gated) supply rails.

$$\begin{aligned}
E_{\text{discharged}} &= E_{\text{rail}} + E_{\text{pg,d}} + E_{\text{logic}} = 0.5 \times (C_{\text{rail}} + C_{\text{pg}} + C_{\text{eff}}) \times V_{\text{dd,nom}}^2 \\
&= 0.5 \times (300\,\text{pF} + 40.4\,\text{pF} + 150\,\text{pF}) \times (1.2\,\text{V})^2 \\
&= 353.1\,\text{pJ}
\end{aligned}$$

(d) Determine the minimum off time for the block at which the leakage savings break even with the energy required to switch the power gate and re-charge the virtual rails.

$$E_{\text{recharge}} = 2 \times E_{\text{discharged}} = 706.2\,\text{pJ}$$
$$T_{\text{off,min}} = E_{\text{recharge}}/(I_{\text{leak}} \times V_{\text{dd,nom}}) = 6.5\,\text{ns}$$