Timing

Discussion 7
Announcements

- Homework 3 released, due Friday 3/22
- Midterm report assignment will be officially released soon (also due Friday 3/22)
  - Start doing literature review on your block, decide on topology/implementation details
- Design review after break
151 Review: Inverter Chain Design
151 Review: Inverter Chain Design

- Strategy can be generalized to any logic gate
- Derivative approach is universal
  - $N\sqrt{F}$ situational, but often applicable
151 Review: Setup and Hold Time

\[ t_{\text{clk-q}} + t_{\text{logic, max}} + t_{\text{su}} \leq T_{\text{clk}} + t_{sk} \]

\[ t_{\text{clk-q}} + t_{\text{logic, min}} \geq t_{h} + t_{sk} \]

- Clock skew improves one margin at the cost of another
## Flip Flop vs. Latch

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<th>Flip Flop</th>
<th>Latch</th>
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<td><strong>Edge-triggered</strong></td>
<td>Edge-triggered</td>
<td>Level-triggered</td>
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<td><strong>Data launch set by clock edge</strong></td>
<td>Data launch set by clock edge</td>
<td>Data launch set by input data timing (and clock edge)</td>
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<tr>
<td><strong>Timing analysis limited to consecutive pair of FFs</strong></td>
<td>Timing analysis limited to consecutive pair of FFs</td>
<td>Timing analysis not limited to consecutive pair of latches</td>
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Latch Timing Exercise

- $t_{C-Q} = 50 \text{ ps}$, $t_{D-Q} = 50 \text{ ps}$, $t_{su} = 60 \text{ ps}$

- $t_{s1,max} = 200 \text{ ps}$, $t_{s2,max} = 240 \text{ ps}$

- Assume data input to R0 always arrives while R0 is non-transparent

- Compute the minimum clock period $T_{clk}$
Latch Timing Exercise: Latch Phases

The diagram illustrates a latch timing exercise with three latches labeled R0, R1, and R2. The clock (clk) signal is applied to each latch. The notations E0, Ei, Li, and Li/E2 are used to denote the edges and states of the clock signal.

- E0: When the latch becomes transparent.
- Ei: When the latch becomes transparent.
- Li: When it is no longer transparent.
- Li/E2: When it is no longer transparent.

The diagram shows the signal flow and timing relationships between the clock and the latches.
Latch Timing Exercise: \( R0 \rightarrow R1 \)

\[
\begin{align*}
\tau_c - q + t_{su} + t_{sl} & \leq T_{clk} = 50 + 60 + 200 \\
T_{clk} & \geq 370 \mu s
\end{align*}
\]
Latch Timing Exercise: R1 → R2

\[ +C - Q + t_{50} + t_{52} = 50 + 60 + 240 = 350 \leq T_{\text{clk}} \]
Latch Timing Exercise: R0 → R1 → R2

\[ t_{c-w} + t_{s1,max} + t_{D-Q} + t_{s2,max} + t_{su} \leq 1.5 \times T_{clk} \]

\[ 50 + 200 + 50 + 200 + 60 = \frac{600}{1 \text{ s}} = 900 \text{ ns} \]
A timing path with a single register driving a latch-based system is shown in Fig. 3. R0 is a rising-edge triggered register, while R1, R2, and R3 are level sensitive. There are two 50% duty cycle clock phases available, with clkb offset from clk by half a period. Both registers and latches have zero hold time, and there is no clock skew in the system. Registers have $t_{clk-Q} = 100$ ps. Latches have $t_{clk-Q} = t_{D-Q} = t_{su} = 150$ ps.

![Diagram of clock paths with registers and latches](image)

**Fig. 3.**

a) The critical path of S1 is 600 ps, the critical path of S2 is 400 ps, and the critical path of S3 is 550 ps. Compute the minimum clock period.
A more complex example

\[(R_1 \rightarrow R_2) \times N\]

Fig. 3.

\[
\begin{align*}
N &= 1 \\
&= \quad t_{c-Q} + t_{s2} + t_{D-Q} + t_{s1} + t_{sv} \leq 1.5T_{clk}
\end{align*}
\]

\[
\begin{align*}
N &= 2 \\
&= \quad t_{c-Q} + t_{s2} + t_{D-Q} + t_{s1} + t_{D-Q} + t_{s2} + t_{D-Q} + t_{s1} + t_{sv} \leq 2.5T_{clk}
\end{align*}
\]

\[
\begin{align*}
&= \quad t_{c-Q} + t_{sv} + N(2t_{D-Q} + t_{s2} + t_{s1}) - t_{D-Q} \leq \frac{2N+1}{2}T_{clk} \\
&= \quad \frac{2}{2N+1}(t_{c-Q} + t_{sv} - t_{D-Q}) + \frac{2N}{2N+1}(2t_{D-Q} + t_{s2} + t_{s1}) \leq T_{clk}
\end{align*}
\]
A more complex example

\[
\lim_{N \to \infty} \frac{2}{2^{N+1}} (t_c - q + t_s - t_D - q) + \frac{2N}{2^{N+1}} (2t_D - q + t_{S2} + t_{S1}) \\
= 2t_D - q + t_{S2} + t_{S1} = 2\times50 + 608 + 406 = 1360 \mu
\]
Z-Scores and Yield

- Gaussian (Normal) distribution often used to model random variation

- Common numbers:
  - 68% within +/-1 sigma
  - 95% within +/-1 sigma
  - 99.7% within +/-3 sigma

- For value $x$ belonging to a Gaussian distribution of mean $\mu$ and standard deviation $\sigma$, compute $z$ score as
  $$ Z = \frac{x - \mu}{\sigma} $$
Z-Scores and Yield

- Can compute yield using z-score tables
- Example:

  Systematic variation of datapath delay of $\sigma = 10$ ps, nominal setup timing met with slack = 15 ps.

  What's the yield?

- This is just an approximation! Please use a table.
Correlated variation

- Same example, but two paths:
  Systematic variation of datapath delay of $\sigma = 10$ ps, nominal setup timing met with slack = 15 ps. What’s the yield if there are two of these datapaths that must both meet timing?
- Need to know if they are correlated or not (solve both fully correlated and fully uncorrelated case).

- Fully correlated: still 0.97
- Fully uncorrelated: $0.97^2 \approx 0.94$