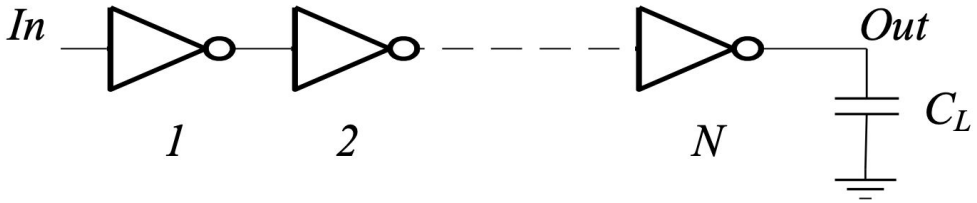
Timing

Discussion 7

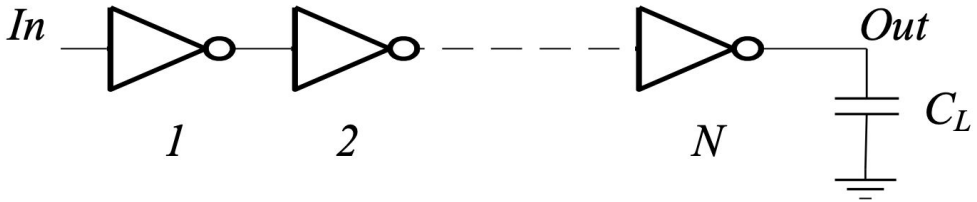
Announcements

- Homework 3 released, due Friday 3/22
- Midterm report assignment will be officially released soon (also due Friday 3/22)
    - Start doing literature review on your block, decide on topology/implementation details
- Design review after break

151 Review: Inverter Chain Design

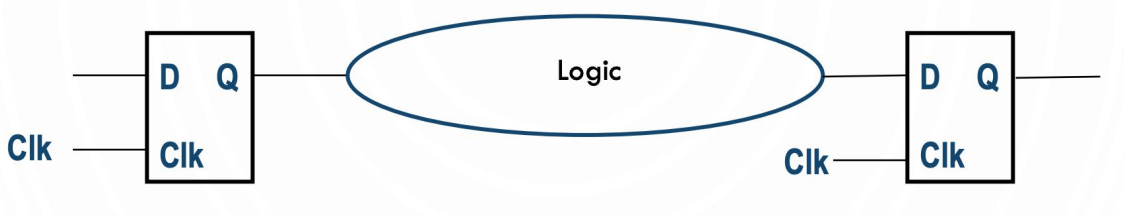


151 Review: Inverter Chain Design



- Strategy can be generalized to any logic gate
- Derivative approach is universal
  - $\sqrt[N]{F}$ situational, but often applicable

151 Review: Setup and Hold Time

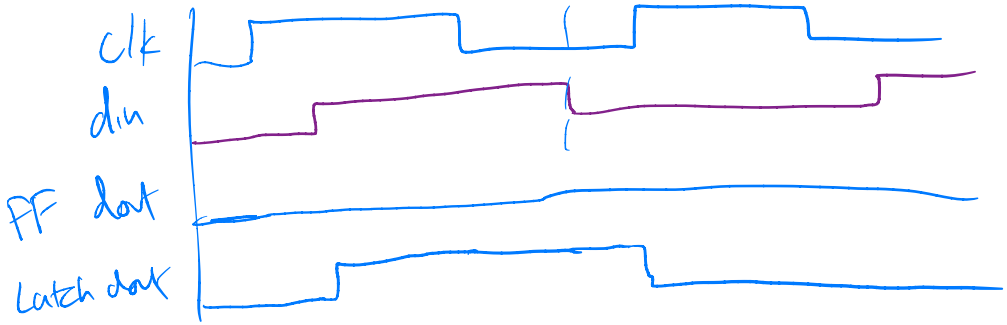


$$t_{clk-q} + t_{logic,max} + t_{su} \leq T_{clk} + t_{sk}$$

$$t_{clk-q} + t_{logic,min} \geq t_h + t_{sk}$$

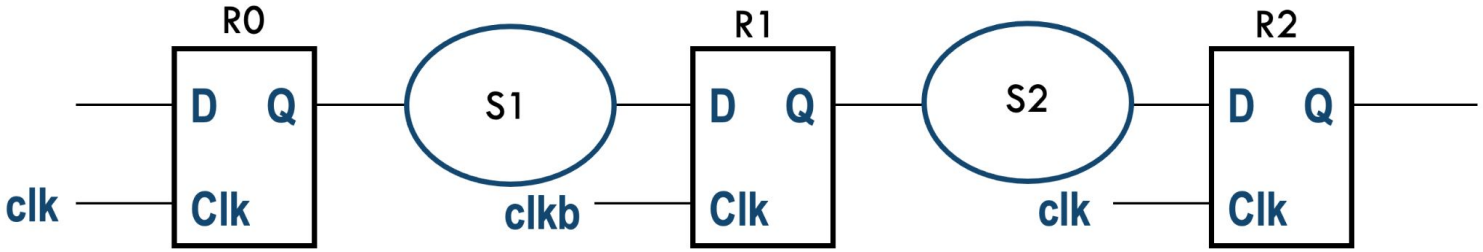
- Clock skew improves one margin at the cost of another

Flip Flop vs. Latch



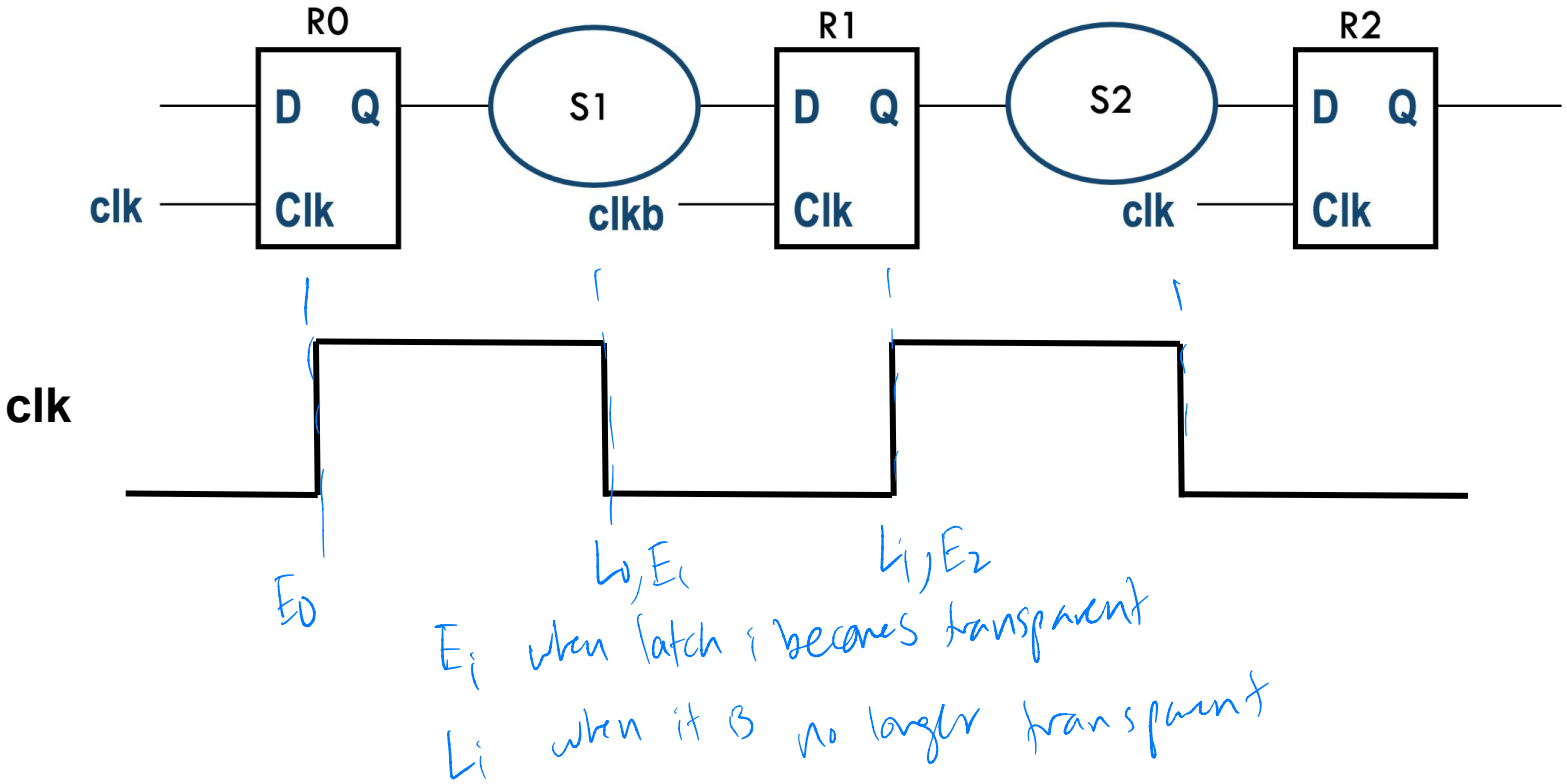
Flip Flop	Latch
Edge-triggered	Level-triggered
Data launch set by clock edge	Data launch set by input data timing (and clock edge)
Timing analysis limited to consecutive pair of FFs	Timing analysis not limited to consecutive pair of latches

Latch Timing Exercise

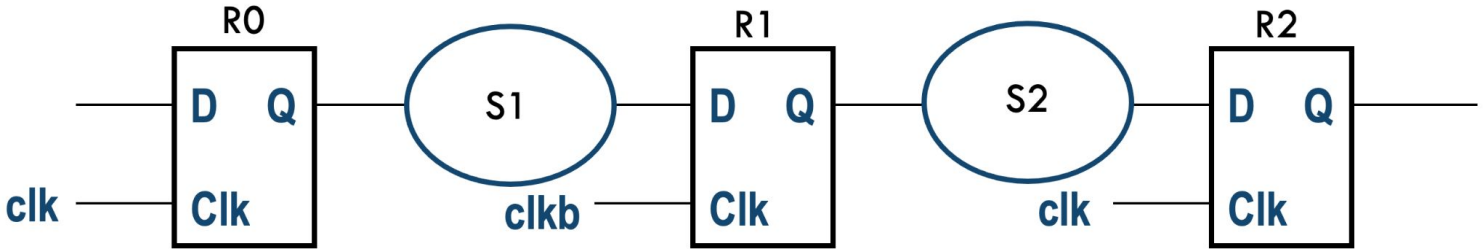


- $t_{C\text{-}Q}$ = 50 ps, $t_{D\text{-}Q}$ = 50 ps, t_{su} = 60 ps
- $t_{s1,max}$ = 200 ps, $t_{s2,max}$ = 240 ps
- Assume data input to R0 always arrives while R0 is non-transparent
- Compute the minimum clock period T_{clk}

Latch Timing Exercise: Latch Phases



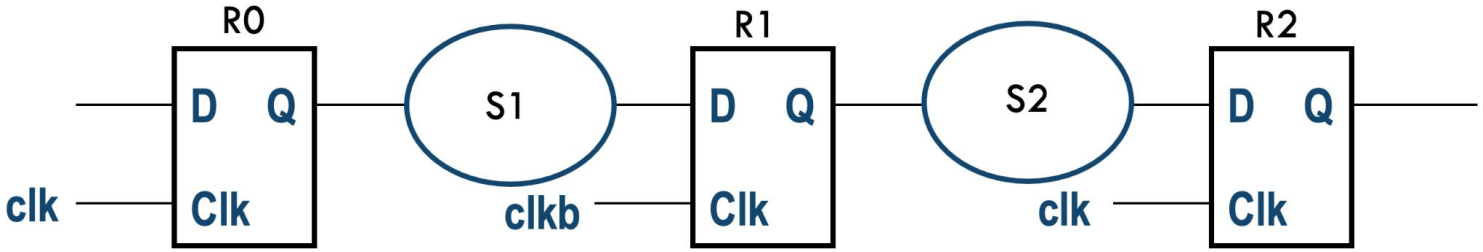
Latch Timing Exercise: R0 → R1



$t_{C\text{-}Q} + t_{su} + t_{S1} \leq T_{clk} = 50 + 60 + 200$

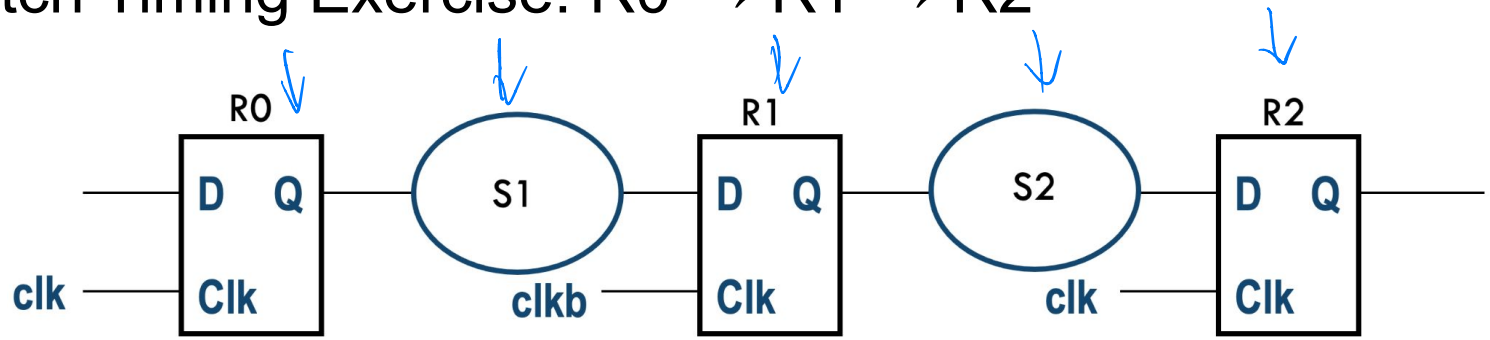
$T_{clk} \geq 310\ ps$

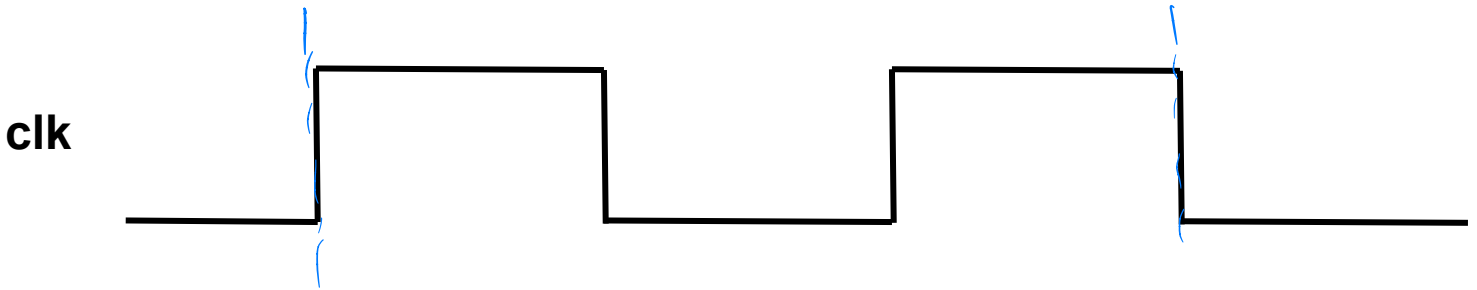
Latch Timing Exercise: R1 → R2



$t_{C-Q} + t_{S1} + t_{S2} = 50 + 60 + 240 = 350 \leq T_{clk}$

Latch Timing Exercise: R0 → R1 → R2





$t_{C\text{-}Q} + t_{S1,max} + t_{D\text{-}Q} + t_{S2,max} + t_{SU} \leq 1.5 T_{clk}$

$50 + 200 + 50 + 200 + 60 = \frac{600}{1.5} = 400\ ps$

A more complex example

A timing path with a single register driving a latch-based system is shown in Fig. 3. R0 is a rising-edge triggered register, while R1, R2, and R3 are level sensitive. There are two 50% duty cycle clock phases available, with clkb offset from clk by half a period. Both registers and latches have zero hold time, and there is no clock skew in the system. Registers have $t_{clk\text{-}Q} = 100$ ps. Latches have $t_{clk\text{-}Q} = t_{D\text{-}Q} = t_{su} = 150$ ps.

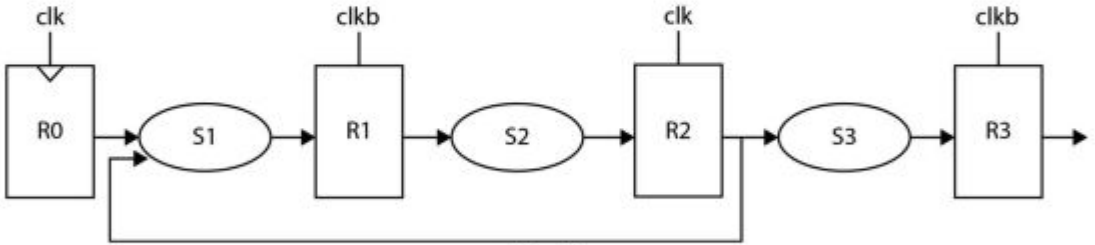


Fig. 3.

a) The critical path of S1 is 600 ps, the critical path of S2 is 400 ps, and the critical path of S3 is 550 ps. Compute the minimum clock period.

A more complex example

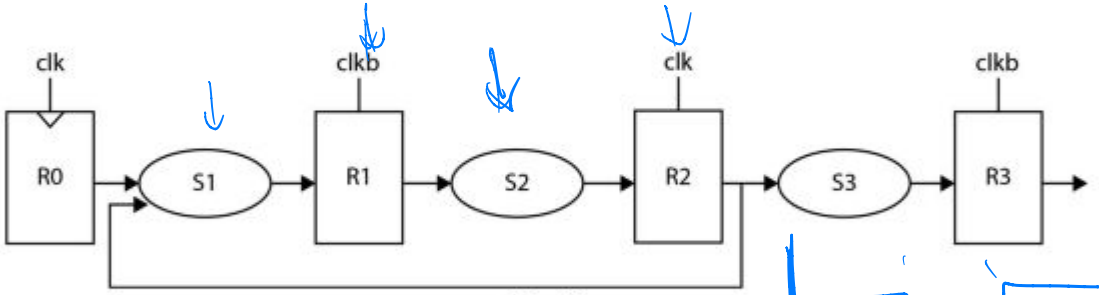


Fig. 3.

$(R_1 \to R_2) \times N$

clkb

$N=1 \quad t_{C\text{-}Q} + t_{S2} + t_{D\text{-}Q} + t_{S1} + t_{SU} \le 1.5 T_{clk}$

$N=2 \quad t_{C\text{-}Q} + t_{S2} + t_{D\text{-}Q} + t_{S1} + t_{D\text{-}Q} + t_{S2} + t_{D\text{-}Q} + t_{S1} + t_{SU} \le 2.5 T_{clk}$

$N \quad t_{C\text{-}Q} + t_{SU} + N(2t_{D\text{-}Q} + t_{S2} + t_{S1}) - t_{D\text{-}Q} \le \frac{2N+1}{2} T_{clk}$

$\frac{2}{2N+1}(t_{C\text{-}Q} + t_{SU} - t_{D\text{-}Q}) + \frac{2N}{2N+1}(2t_{D\text{-}Q} + t_{S2} + t_{S1}) \le T_{clk}$

A more complex example

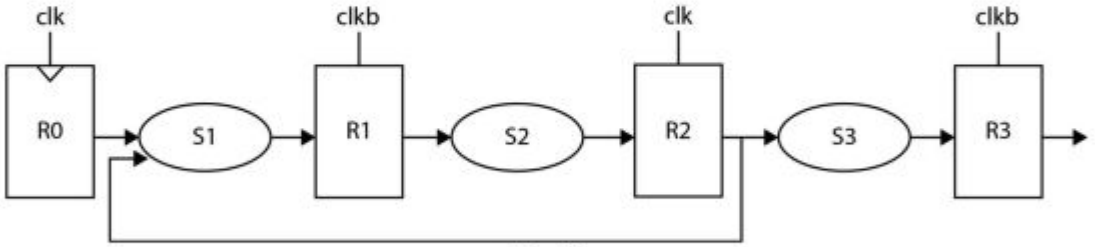
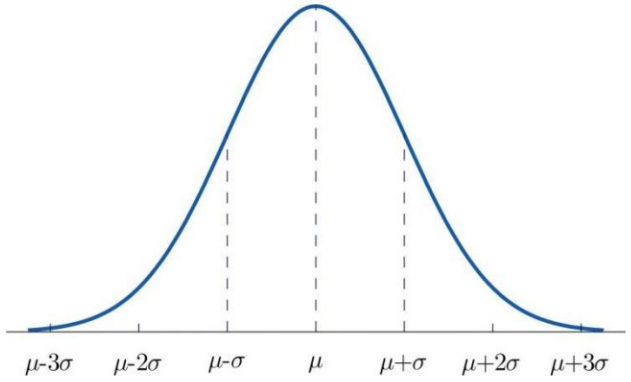


Fig. 3.

$$\lim_{N \to \infty} \frac{2}{2N+1}(t_{C\text{-}Q} + t_{S\text{-}} - t_{D\text{-}Q}) + \frac{2N}{2N+1}(2t_{D\text{-}Q} + t_{S2} + t_{S1})$$

$$= 2t_{D\text{-}Q} + t_{S2} + t_{S1} = 2(150) + 606 + 406 = 1300\ ps$$

Z-Scores and Yield



$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-(x-\mu)^2}{2\sigma^2}}$$

- Gaussian (Normal) distribution often used to model random variation
- Common numbers:
  - 68% within +/-1 sigma
  - 95% within +/-1 sigma
  - 99.7% within +/-3 sigma
- For value x belonging to a Gaussian distribution of mean μ and standard deviation σ, compute z score as $$z = \frac{x - \mu}{\sigma}$$

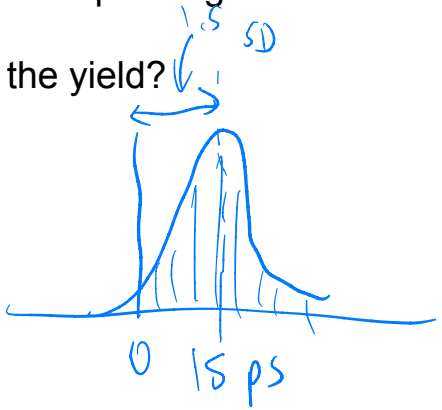
Z-Scores and Yield

- Can compute yield using z-score tables
- Example:

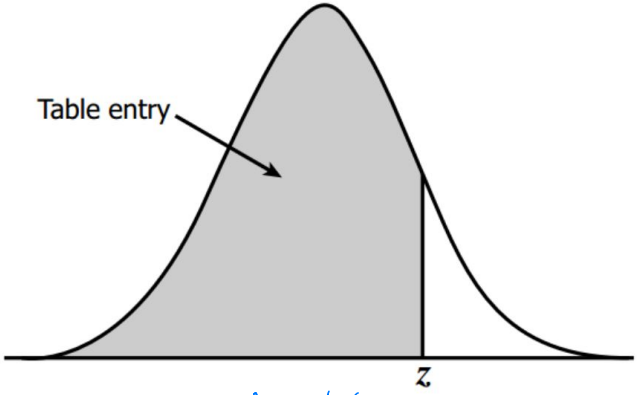
  Systematic variation of datapath delay of σ = 10 ps,

  nominal setup timing met with slack = 15 ps.

  What's the yield?



0.97 ← (this is just an approximation!! please use a table)



z	.00	.01	.02	.03	.04	.05	.06	.07	.08	.09
0.0	.5000	.5040	.5080	.5120	.5160	.5199	.5239	.5279	.5319	.5359
0.1	.5398	.5438	.5478	.5517	.5557	.5596	.5636	.5675	.5714	.5753
0.2	.5793	.5832	.5871	.5910	.5948	.5987	.6026	.6064	.6103	.6141
0.3	.6179	.6217	.6255	.6293	.6331	.6368	.6406	.6443	.6480	.6517
0.4	.6554	.6591	.6628	.6664	.6700	.6736	.6772	.6808	.6844	.6879
0.5	.6915	.6950	.6985	.7019	.7054	.7088	.7123	.7157	.7190	.7224
0.6	.7257	.7291	.7324	.7357	.7389	.7422	.7454	.7486	.7517	.7549
0.7	.7580	.7611	.7642	.7673	.7704	.7734	.7764	.7794	.7823	.7852
0.8	.7881	.7910	.7939	.7967	.7995	.8023	.8051	.8078	.8106	.8133
0.9	.8159	.8186	.8212	.8238	.8264	.8289	.8315	.8340	.8365	.8389
1.0	.8413	.8438	.8461	.8485	.8508	.8531	.8554	.8577	.8599	.8621
1.1	.8643	.8665	.8686	.8708	.8729	.8749	.8770	.8790	.8810	.8830
1.2	.8849	.8869	.8888	.8907	.8925	.8944	.8962	.8980	.8997	.9015
1.3	.9032	.9049	.9066	.9082	.9099	.9115	.9131	.9147	.9162	.9177
1.4	.9192	.9207	.9222	.9236	.9251	.9265	.9279	.9292	.9306	.9319
1.5	.9332	.9345	.9357	.9370	.9382	.9394	.9406	.9418	.9429	.9441

Correlated variation

- Same example, but two paths:
  Systematic variation of datapath delay of σ = 10 ps, nominal setup timing met with slack = 15 ps.
  What's the yield if there are two of these datapaths that must both meet timing?
- Need to know if they are correlated or not (solve both fully correlated and fully uncorrelated case).

Fully correlated: still 0.97

Fully uncorrelated: $(0.97)^2 < 0.97$