Latch timing and SRAMs

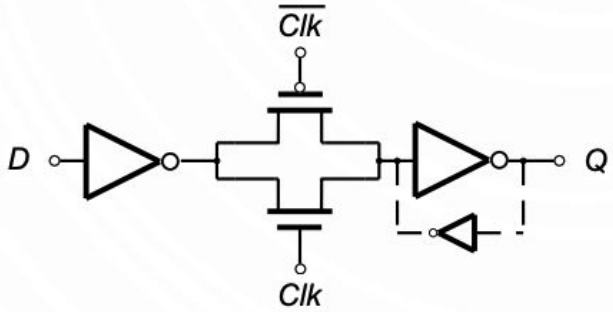
Discussion 8

Announcements

- Design review 4/8 4/9
- Homework 4 due 4/12
- Lab 5 due 4/12

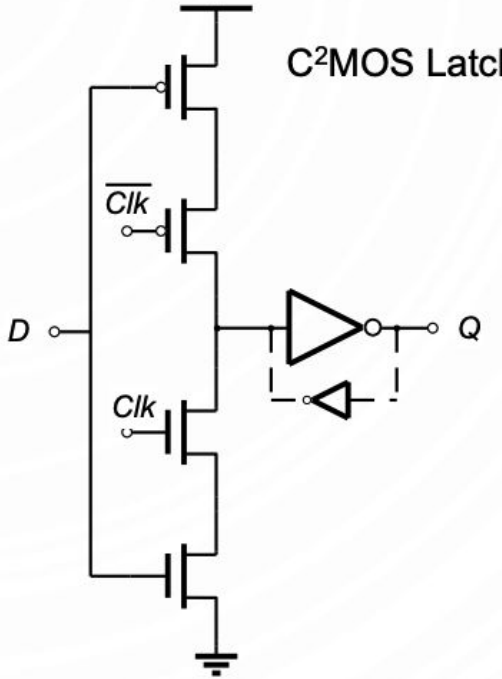
Latches

Transmission-Gate Latch



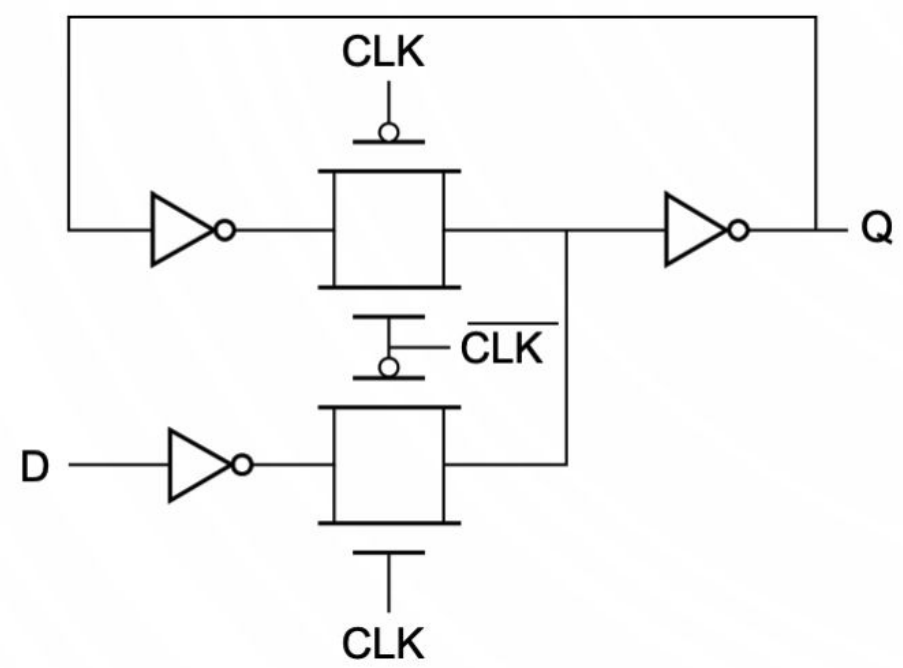
Usually without contention

C^2MOS Latch



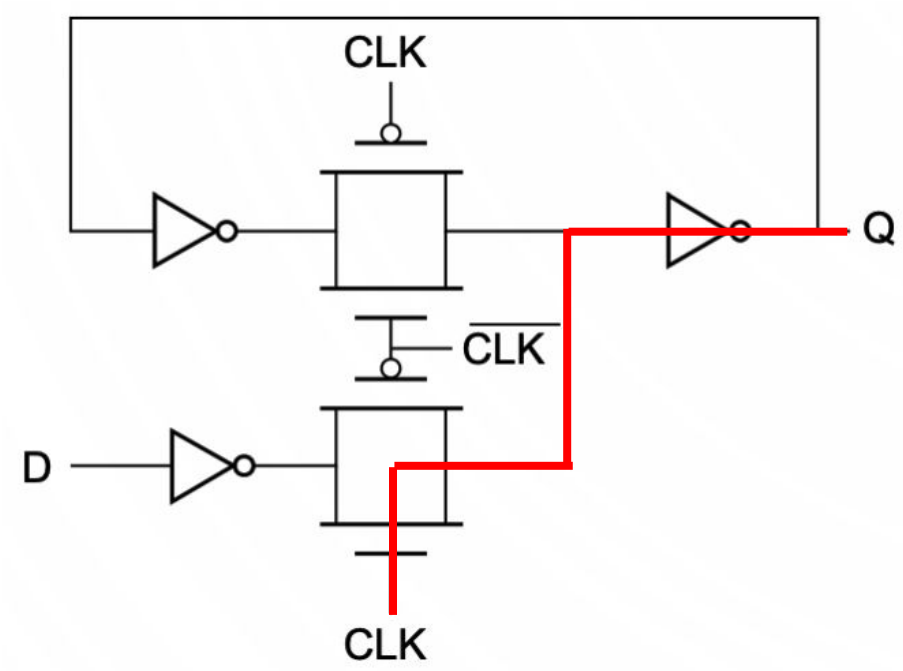
Latch timing

Where are the important paths?



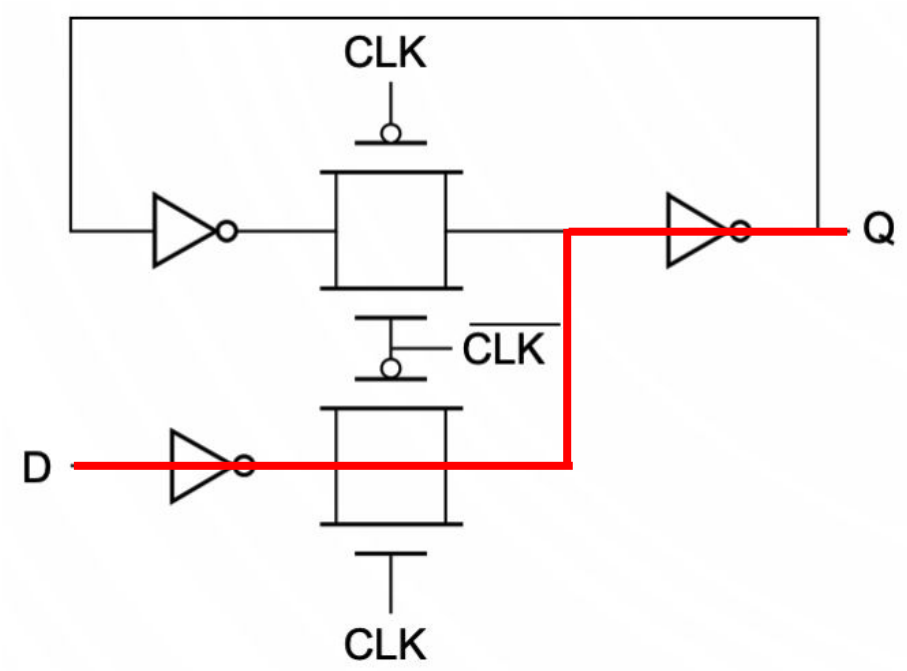
Latch timing

Clk-Q path:



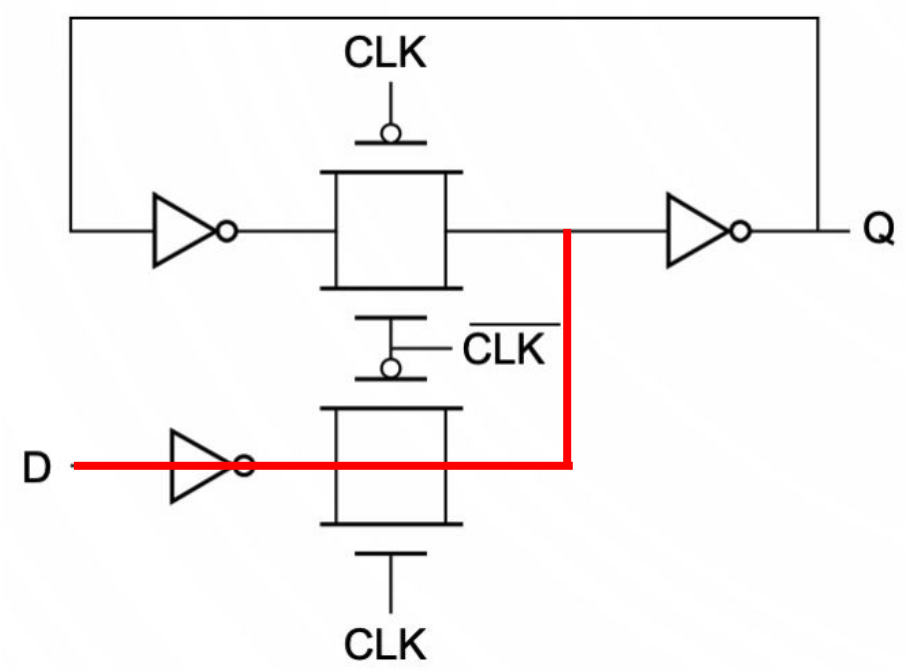
Latch timing

D-Q path:

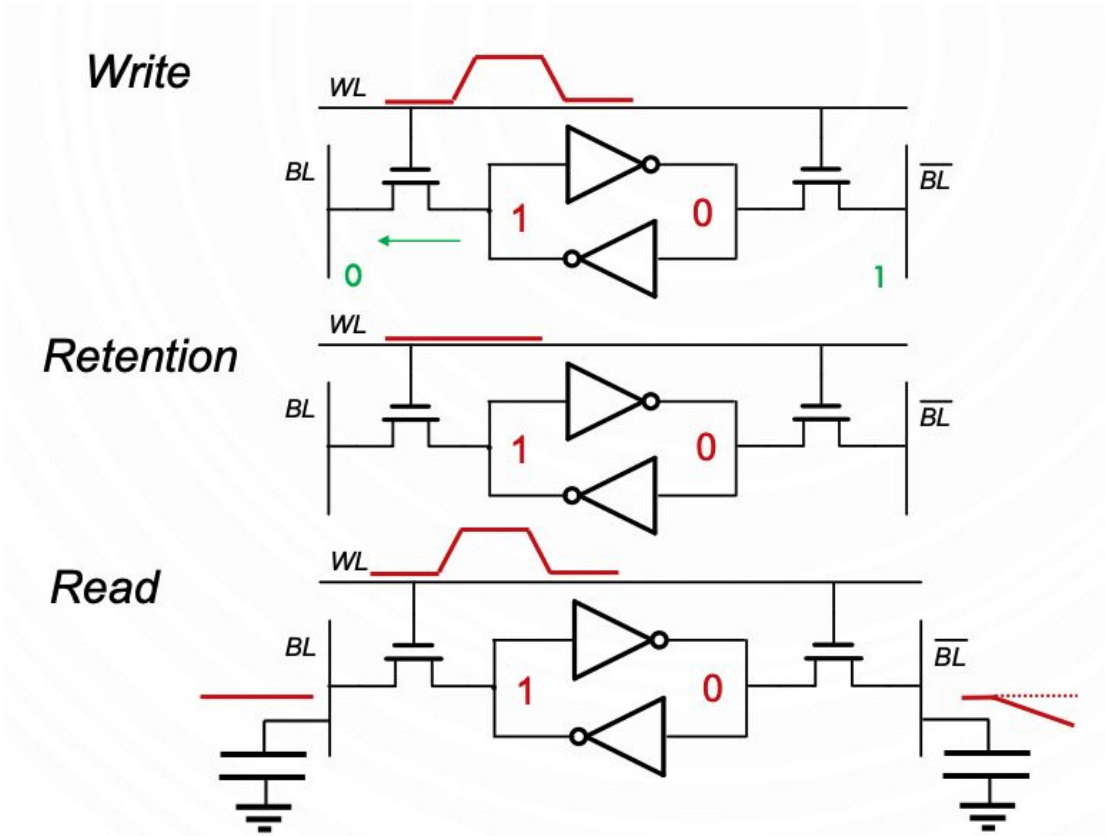


Latch timing

Setup path:

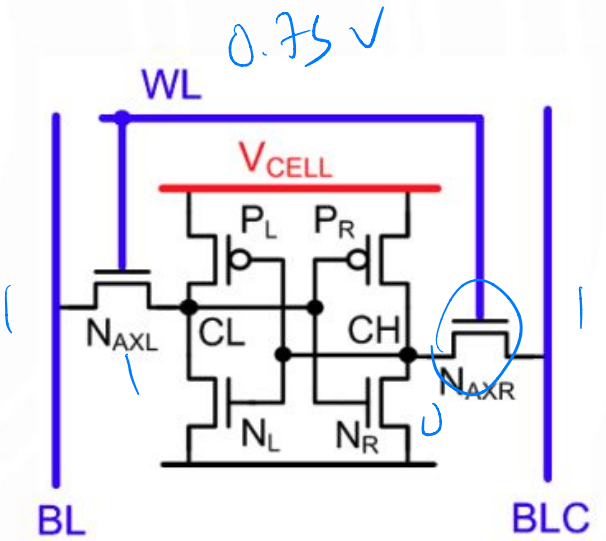


6T SRAM cell


Write
WL
BL
$\overline{BL}$
1
0
0
1
Retention
WL
BL
$\overline{BL}$
1
0
Read
WL
BL
$\overline{BL}$
1
0

SRAM assists

- Dynamically change voltages
- Negative BL helps with writing
- Lower VDD (V_{CELL}) helps with writing
- Higher WL helps with writing, lower hurts
- Lower WL helps with read, higher hurts



Homework 4 Problem 2 (2023)

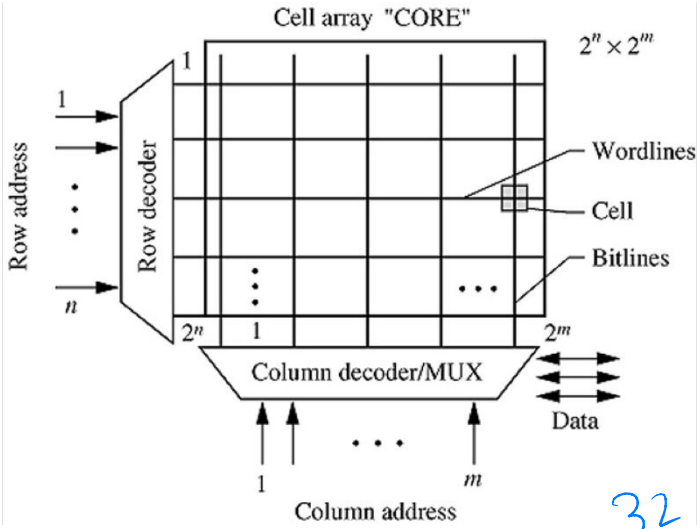
2. SRAM yield

We will analyze a 2MiB (i.e. 2^{20} Bytes) SRAM array, consisting of 128 x 128 bit subarrays. Four columns share one sense amplifier. Bitline capacitance is 1pF and the supply is 1V. For this problem, assume that all the SRAM cells in the array are identical (i.e. not affected by the random process variation) and I_{on} = 100μA, I_{off} = 400nA. Assume that the target access time of 1ns is dominated by the bitline discharge.

If the sense amplifier offset has normal distribution, with zero mean and standard deviation of 15mV, would you expect this array to have a high yield? How many redundant columns would need to be added per subarray to have >99% yield for the whole 2MB SRAM array (note that you may not have to do the exact calculation of this)?

SRAM Topology: Subarray

- Each subarray contains 128 x 128 bits



2^{20} bytes total

Each subarray has 2^{14} bits

$2^{20} \cdot 2^3 / 2^{14} = 2^9$ subarrays

128

32 senseamps

128

2^{14} senseamps

p is probability that one sense amp works

$p^{2^{14}} > 99\%$

SRAM Topology: Shared Sense Amp

- 4 columns share 1 sense amp

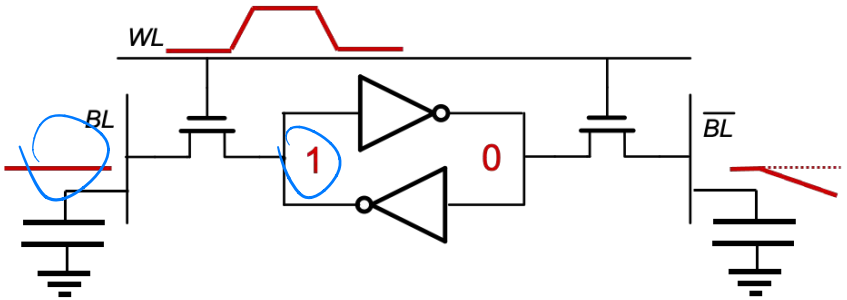
- redundant sense amp?

32 sense amps

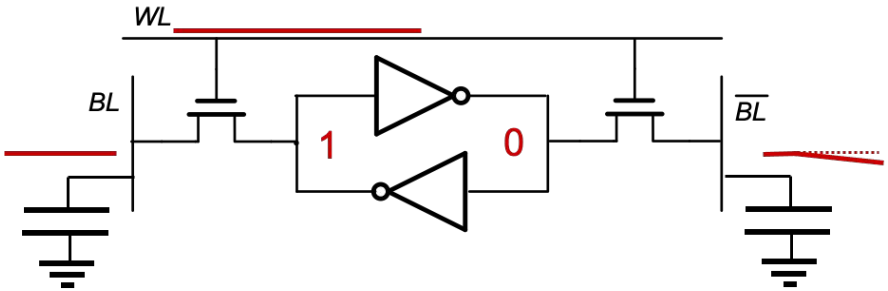
$$p^{32} + (1-p)\, p^{31} \cdot 32$$

SRAM Read

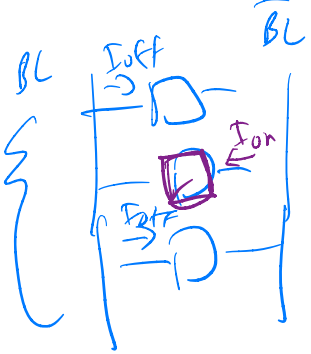
- WL enabled



- WL disabled



128 bitcells



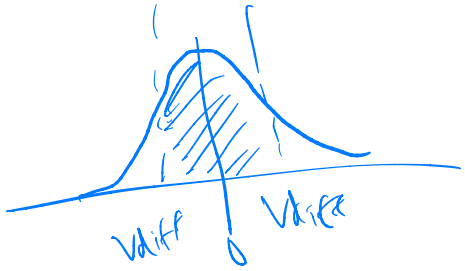
1 pF

VDD = 1 V

Ion = 100 μA

Ioff = 400 nA

$$\left(\frac{I_{on}}{C} - 127\,\frac{I_{off}}{C}\right) t = V_{diff}$$



Yield Computation (without redundancy)

1. Compute worst-case differential bitline voltage V_{BL}
2. Compute required sense amp offset for read failure
3. Find probability of single sense amp failing during read (sense amp yield)
4. Find subarray yield
    - Probability of all sense amps working (or 0 sense amps failing)
5. Find SRAM array yield
    - Probability of all subarrays working

Yield Computation (with *K* redundant columns)

1. Compute worst-case differential bitline voltage V_{BL}
2. Compute required sense amp offset for read failure
3. Find probability of single sense amp failing during read (sense amp yield)
4. **Compute number of redundant sense amps *L***
5. Find subarray yield
    - **Probability of 0 sense amps failing or 1 sense amp failing or … or *L* sense amps failing**
6. Find SRAM array yield
    - Probability of all subarrays working