

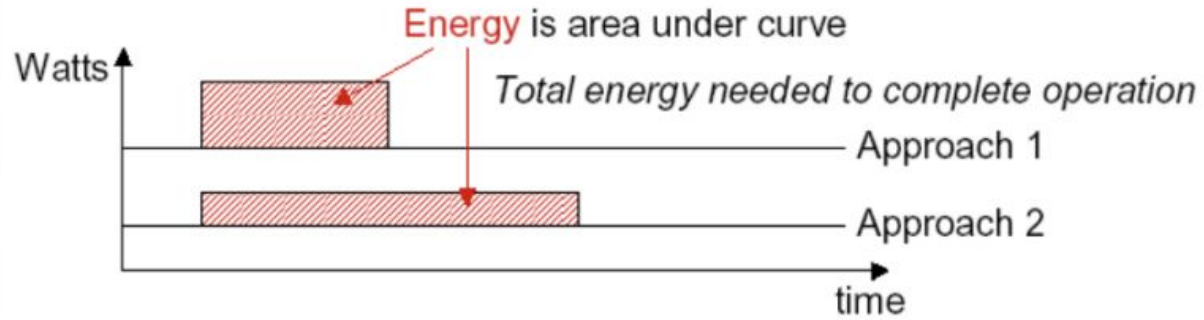
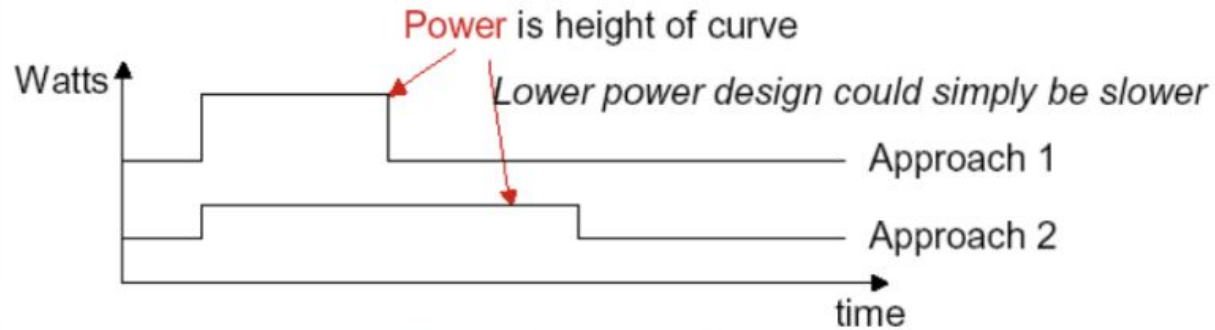
# Power

## Discussion 9

# Announcements

- Final next Thursday (4/26)
  - Some people will be in Moffitt 106, will post final room assignments on Ed
- Homework 5 due 4/23
  - No extensions past 4/23
- Final presentations 9AM-12PM 5/2 (probably in BWRC)

# Power vs. Energy



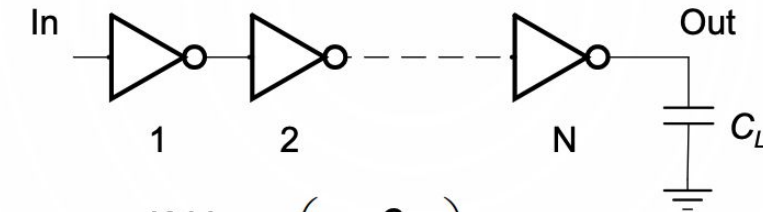
# Power dissipation sources

$$P \sim \underbrace{\alpha \cdot (C_L + C_{CS}) \cdot V_{swing} \cdot V_{DD} \cdot f}_{\text{Dynamic power}} + \underbrace{(I_{DC} + I_{Leak}) \cdot V_{DD}}_{\text{Static power}}$$

- $\alpha$  – switching activity
- $C_L$  – load capacitance
- $C_{CS}$  – short-circuit “capacitance”
- $V_{swing}$  – voltage swing
- $f$  – frequency
- $I_{DC}$  – static current
- $I_{leak}$  – leakage current

# Alpha-power delay scaling

- Since dynamic power is  $\sim CV_{DD}^2f$ , we can scale  $V_{DD}$  down to reduce power
- This also increases our delay, which reduces our frequency

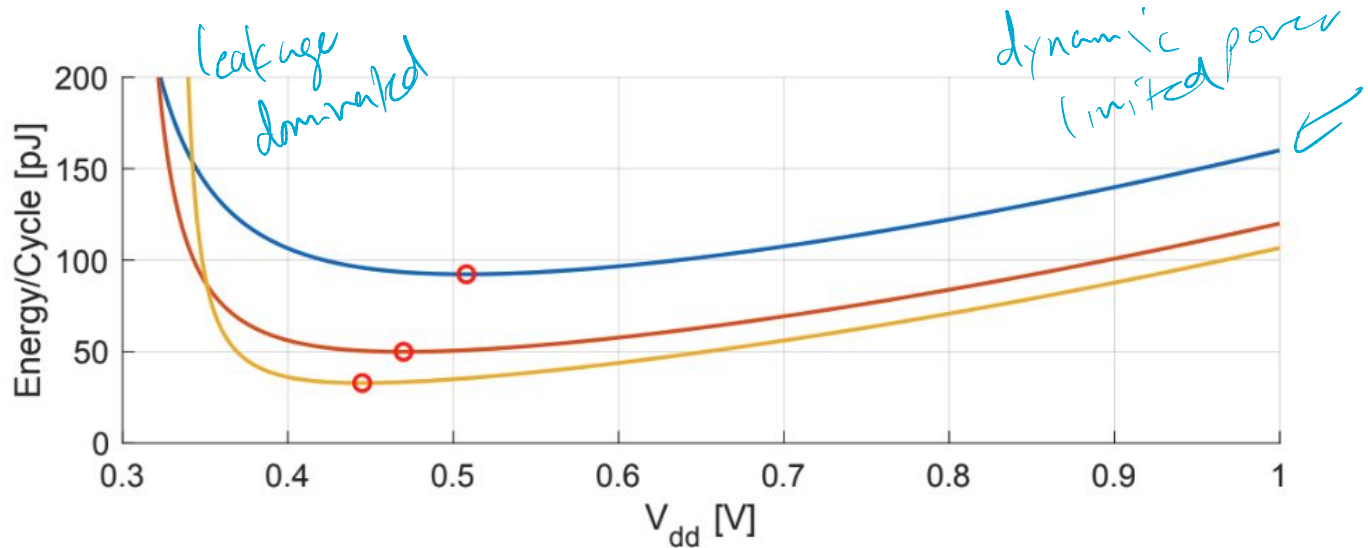


$$t_{pi} = \frac{K_d V_{DD}}{(V_{DD} - V_{Th})^\alpha} \left( 1 + \frac{C_{L,i}}{C_{in,i}} \right)$$

$$D = \sum t_{pi} = \sum \frac{K_d V_{DD}}{(V_{DD} - V_{Th})^\alpha} \left( 1 + \frac{W_{L,i}}{W_{in,i}} \right)$$

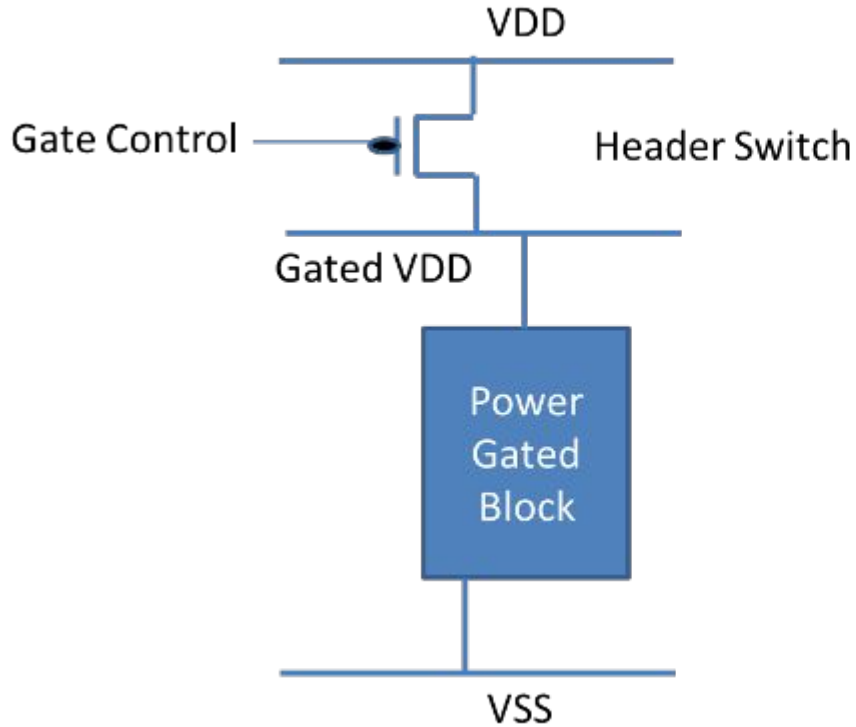
# Dynamic voltage-frequency scaling

- Though dynamic power goes down, energy per cycle goes up because leakage power remains relatively constant and cycles are longer

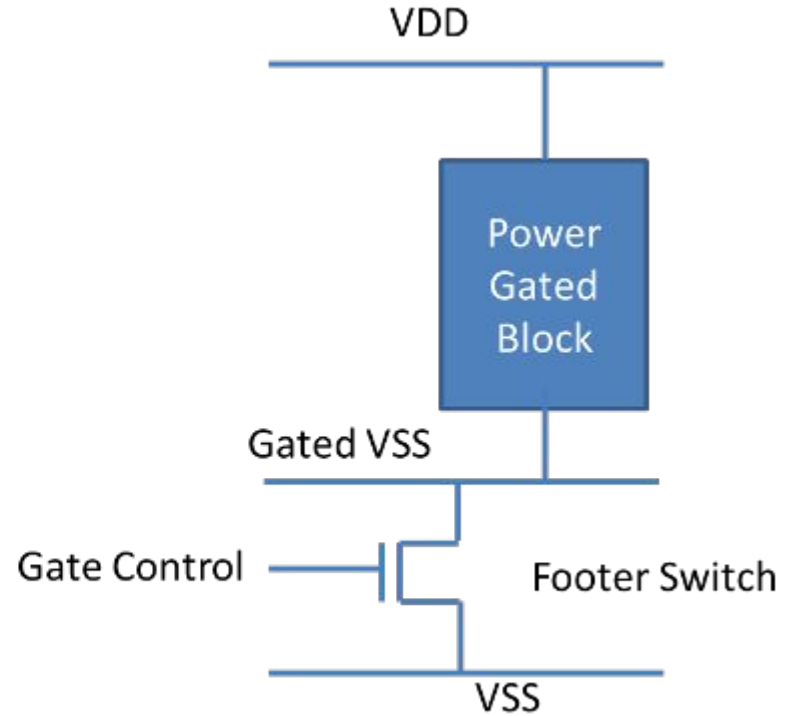


# Power gating

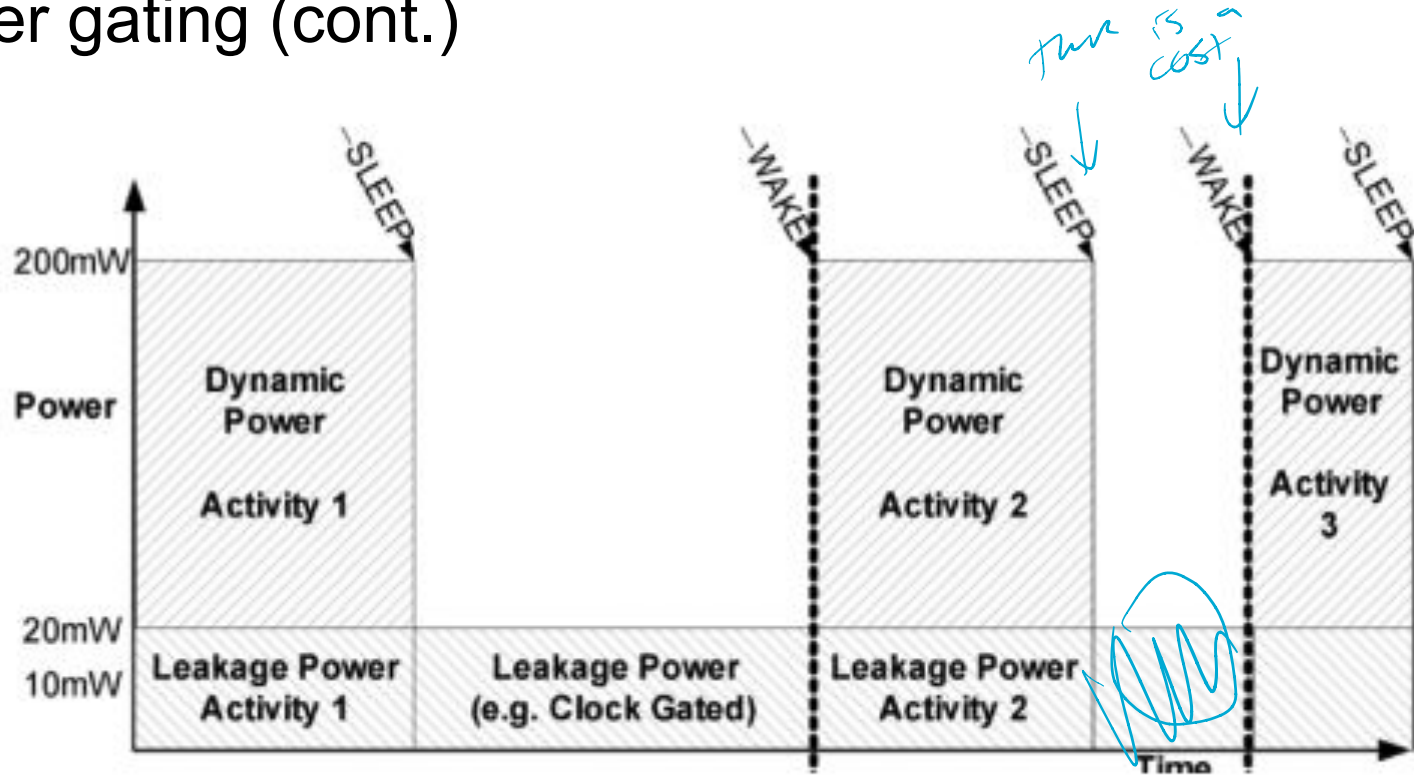
*high-side*



*low-side*



# Power gating (cont.)





# Hints for homework

- Maximum voltage droop is given by resistance of power gate times peak current ( $I_{pk} R_{pg}$ )
- Energy pulled from the supply to switch the power gate is energy required to charge gate to VDD ( $C_g V_{DD}^2$ )
- When turning off power gate, block + power gate + rail discharges energy
- Power gating can become inefficient if the energy needed to switch the power gate outweighs the leakage energy avoided