EECS251B : Advanced Digital Circuits and Systems

Lecture 12 – Standard Cells

Borivoje Nikolić

Aries v.3.0

The ARIES v3.0 is a fully indigenous and a "Made in India" product to get started with basic microprocessor programming and embedded systems. This board is built upon a RISC-V ISA compliant VEGA Processor with easy-to-use hardware and software. The VEGA SDK also provides full ecosystem with numerous examples and support documentation.

https://vegaprocessors.in/devboards/ariesv3.php

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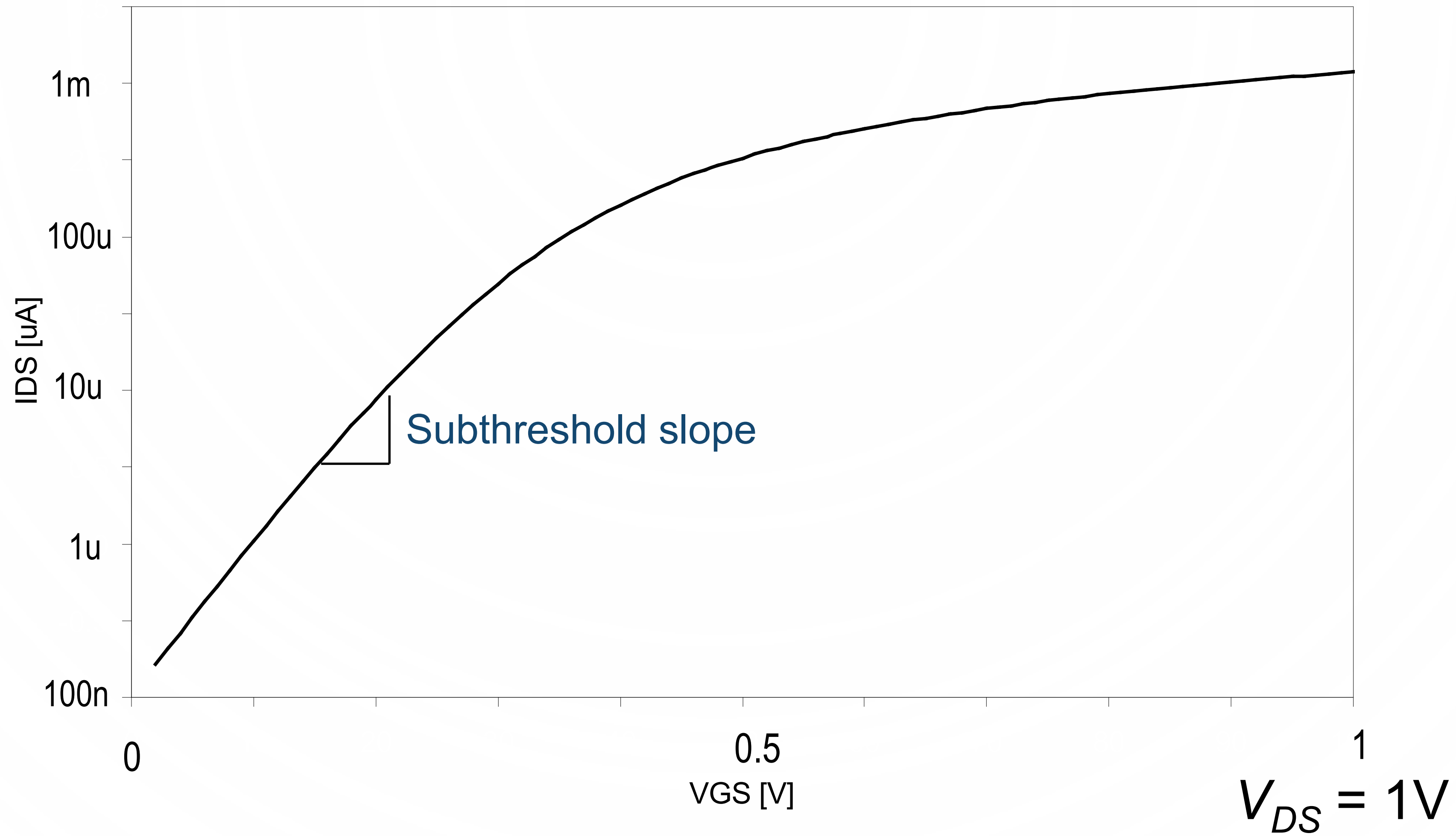
Announcements

- Lab 5 waiting on PDK correction
- Start project phase 1
- Homework 2 due next week
- Quiz 1 today!

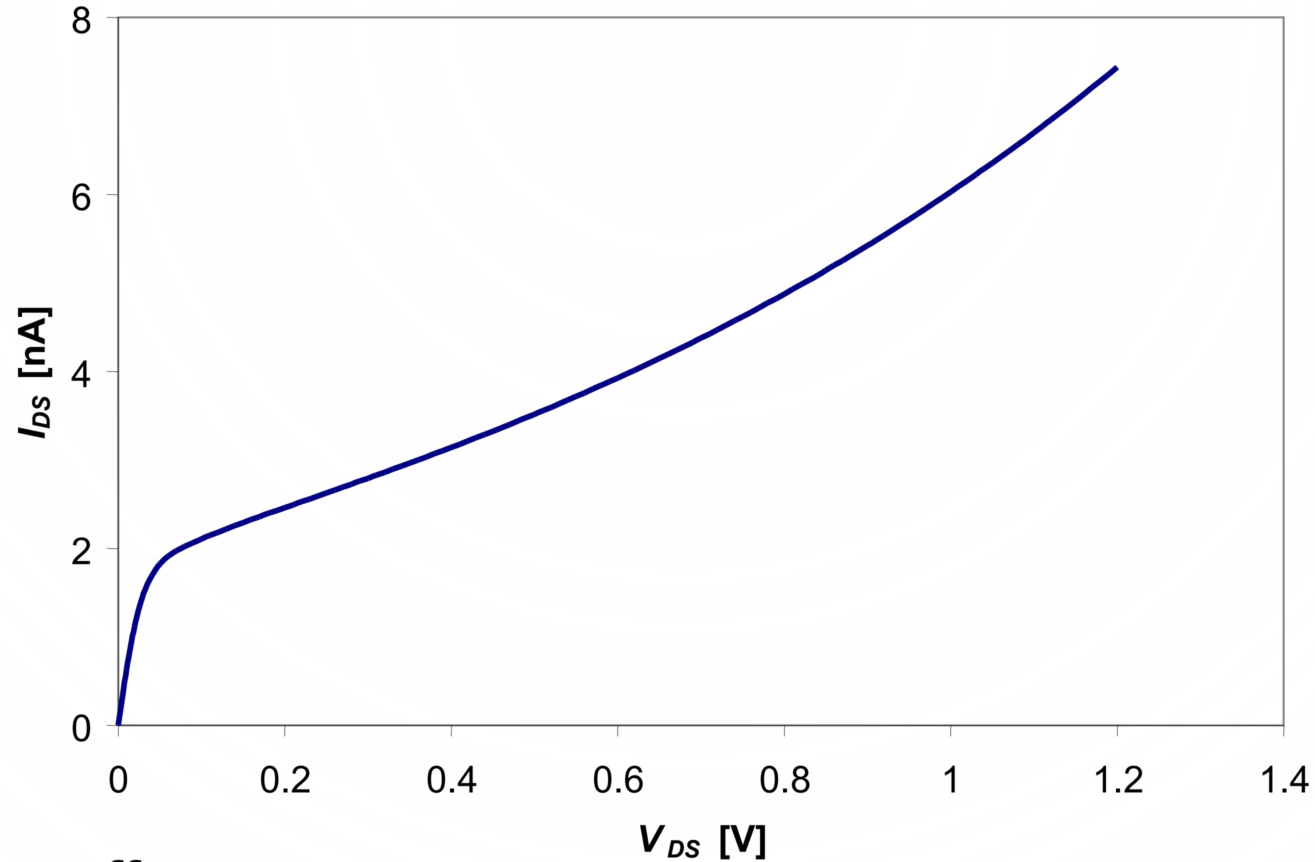
Transistor Leakage

Transistor Leakage



Leakage current is exponential with V_{GS}

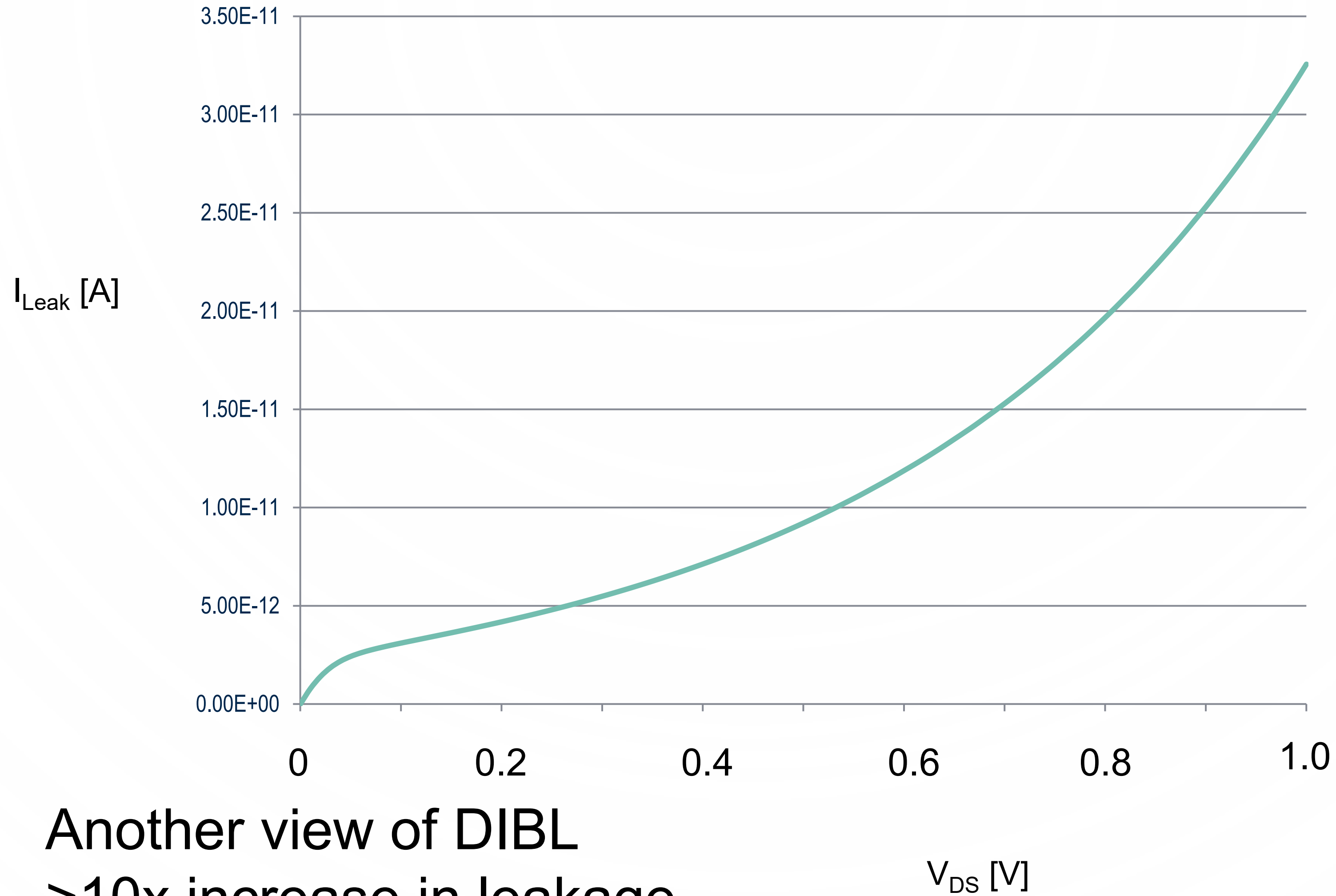
Transistor Leakage (130nm)



Two effects:

- diffusion current (like a bipolar transistor)
- exponential increase with V_{DS} (DIBL)

Transistor Leakage (32nm LP PTM)



Another view of DIBL

>10x increase in leakage

Subthreshold Current

- Subthreshold behavior can be modeled physically

$$I_{ds,subth} = \mu_{eff} C_{ox} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 e^{\frac{V_{GS}-V_{Th}}{mkT/q}}\left(1-e^{-\frac{Vds}{kT/q}}\right)$$

$$m = 1 + \frac{C_{dm}}{C_{ox}}$$ (m ~ 1.1-1.4)

Taur, Ning, Modern VLSI Devices

Or (approx):

$$I_{ds,subth} = I_0 \frac{W}{W_0} 10^{\frac{(V_{gs}-V_{Th})+\gamma V_{ds}}{S}}$$

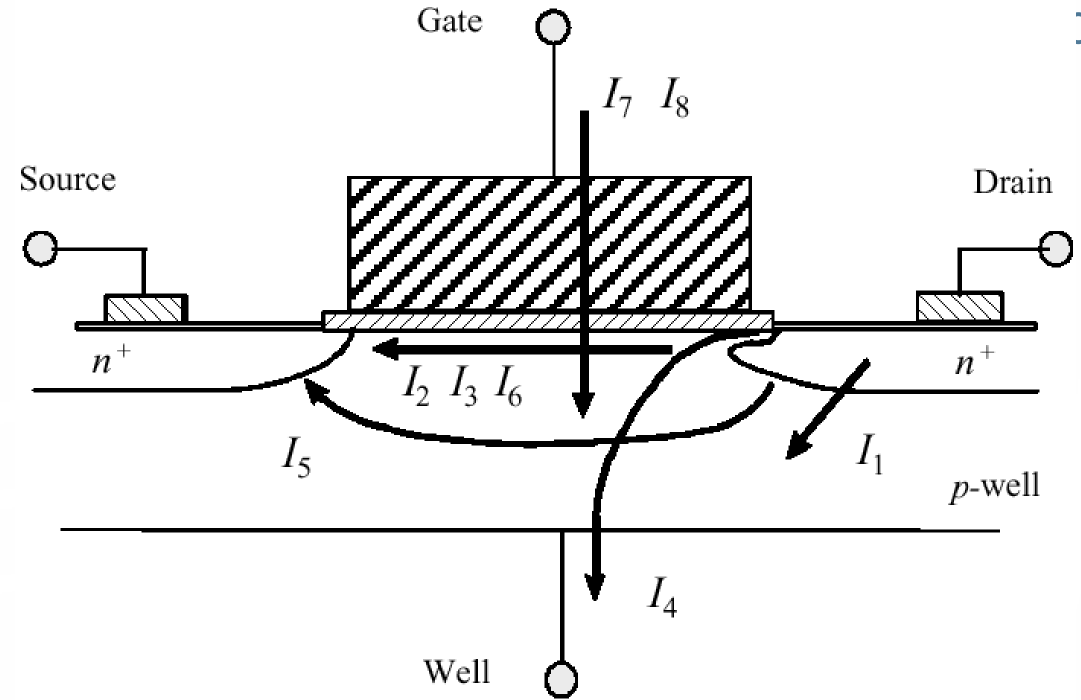
$$S = 2.3m\frac{kT}{q}$$

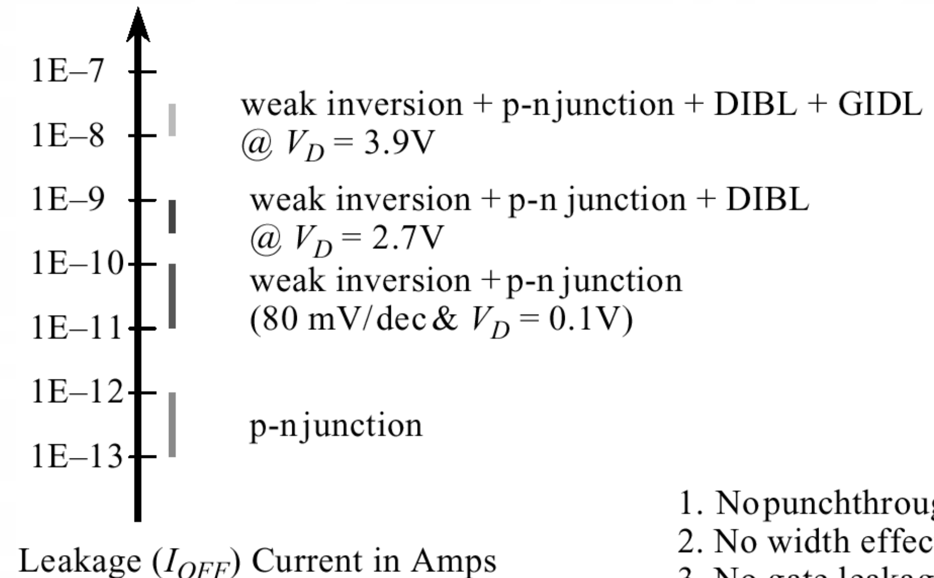
Added Leakage Components

- Drain-induced barrier lowering (DIBL)
  - Voltage at the drain lowers the source potential barrier
  - Lowers V_{Th}, no change on S
- Gate-induced drain leakage (GIDL)
  - High field between gate and drain increases injection of carriers into substrate -> leakage
    (band-to-band leakage)

Leakage Components (250nm)

1. pn junction reverse bias current
2. Weak inversion
3. Drain-induced barrier lowering (DIBL)
4. Gate-induced drain leakage (GIDL)
5. Punchthrough
6. Narrow width effect
7. Gate oxide tunneling
8. Hot carrier injection

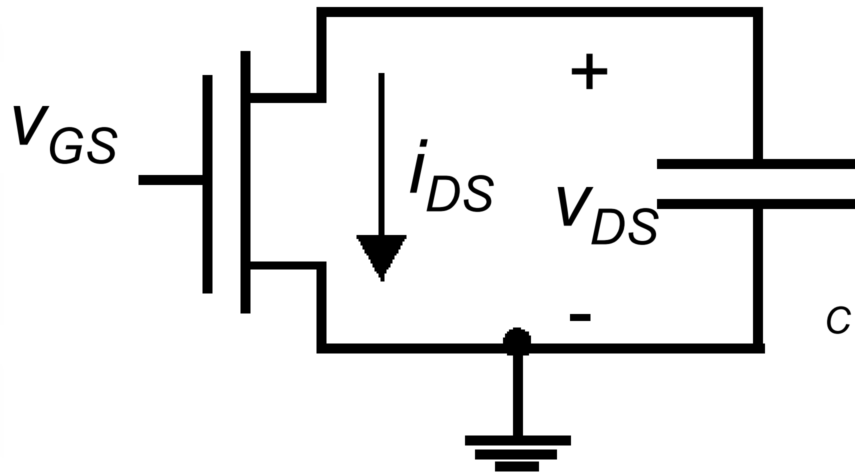




Transistor C-V

MOS Transistor as a Switch

Discharging a capacitor



- Can solve:

$$i_{DS} = i_{DS}\left(v_{DS}\right)$$

$$i_{DS} = C\left(v_{DS}\right)\frac{dv_{DS}}{dt}$$

- Prefer using equivalent resistances
- Find t_{pHL}
- Find equivalent C, R

$$t_{pHL} = \int \frac{C(v_{DS})\,dv_{DS}}{i_{DS}\left(v_{GS}, v_{DS}\right)}$$

MOS Capacitances

- Gate capacitance
  - Non-linear channel capacitance
  - Linear overlap, fringing capacitances
  - Miller effect on overlap, fringing capacitance
- Non-linear drain diffusion capacitance
  - PN junction
- Wiring capacitances
  - Linear

Gate and Drain Capacitances

Gate capacitance

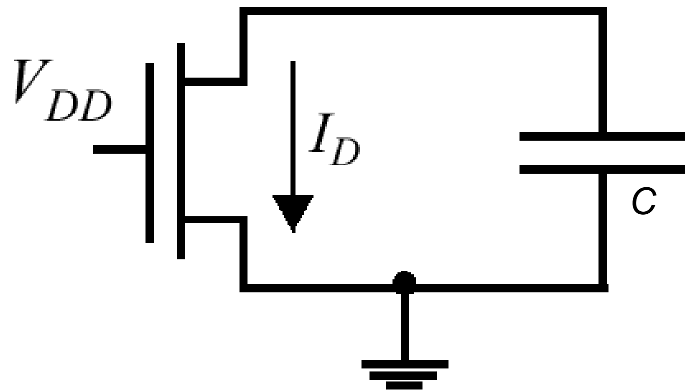
Drain capacitance

Gate Capacitances

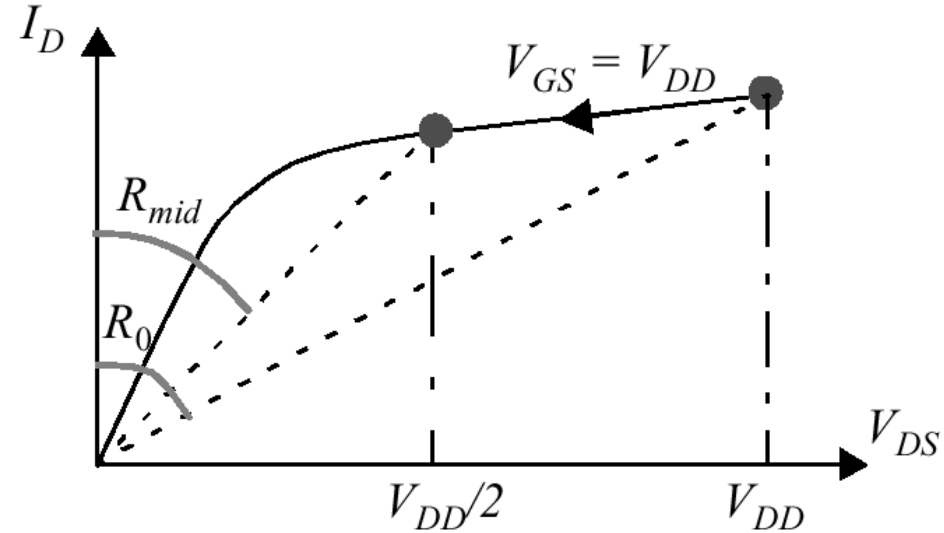
- Gate capacitance is non-linear
  - First order approximation with $C_{ox}WL$ ($C_{ox}L$ = 2fF/μm)
- Need to find the actual equivalent capacitance by simulating it
- Since this is a linear approximation of non-linear function, it is valid only over the certain range
  - Different capacitances for HL, LH transitions and power computation
- Drain capacitance non-linearity compensates
  - But this changes with fanout

Delay Revisited

MOS Transistor as a Switch (EECS251A)



Traversed path



$$R_{eq} = \text{average}_{t = t_1 \dots t_2}(R_{on}(t)) = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} R_{on}(t)dt = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)}dt$$

$$\approx \frac{1}{2}(R_{on}(t_1) + R_{on}(t_2))$$

MOS Transistor as a Switch (EECS251A)

Solving the integral:

$$R_{eq} = \frac{1}{-V_{DD}/2} \int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT}(1+\lambda V)} dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

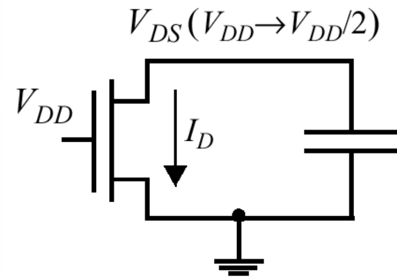
with appropriately calculated I_{dsat}

Averaging resistances:

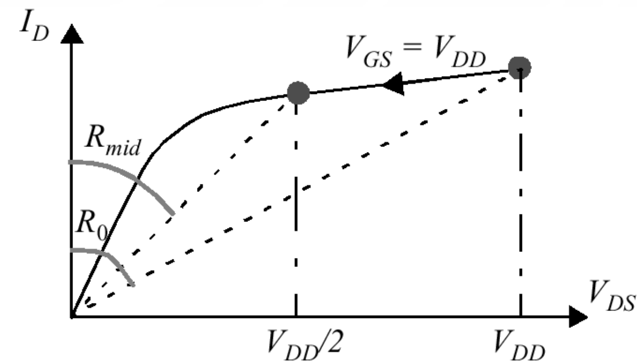
$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

CMOS Performance

Propagation delay: $t_{pHL} = (\ln 2) R_{eqn} C_L \quad t_{pLH} = (\ln 2) R_{eqp} C_L$



(a) schematic

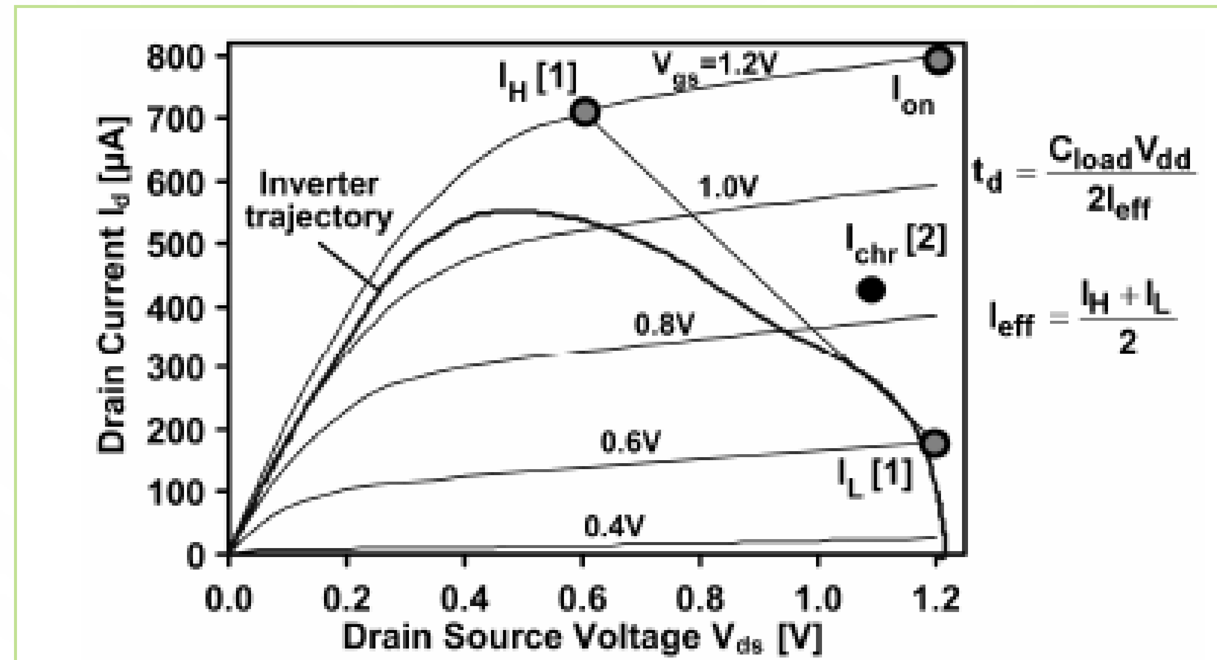


(b) trajectory traversed on ID-VDS curve.

ln2 = 0.7

Effective Current

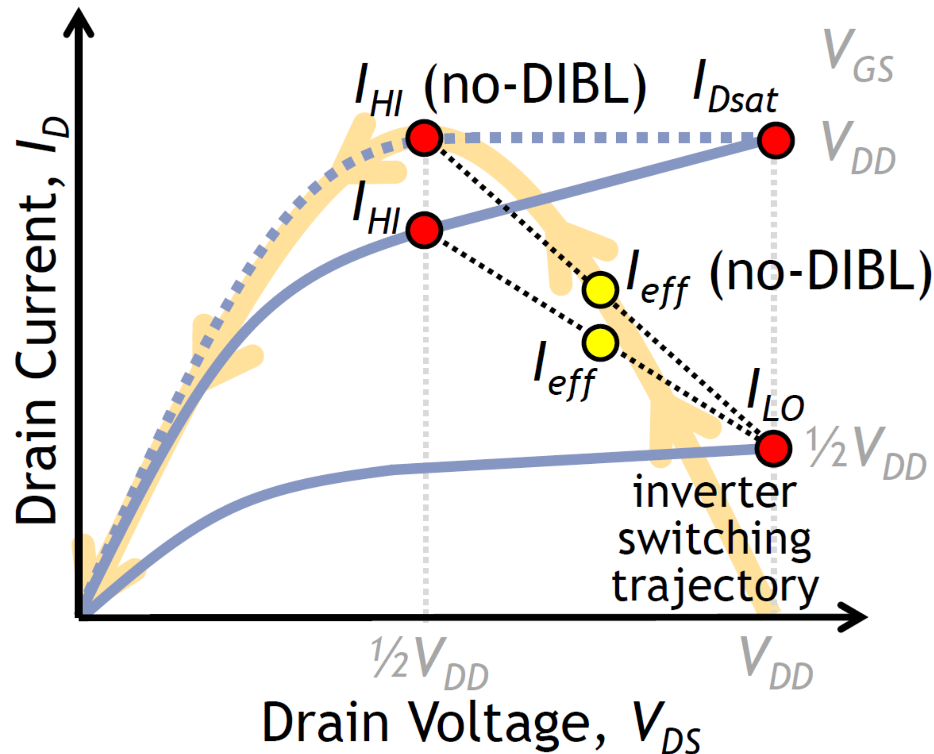
- $I_{on}(V_{DD})$ is never reached
- Define $I_{eff} = (I_H + I_L)/2$
- $I_L = I_{DS}(V_{GS}=V_{DD}/2, V_{DS}=V_{DD})$; $I_H=I_{DS}(V_{GS}=V_{DD}, V_{DS}=V_{DD}/2)$,



Na, IEDM'2002
Von Arnim, IEDM'2007

DIBL Matters

- A. Loke, VLSI'16
  - FinFET, FDSOI – less DIBL



$$I_{eff} = \frac{I_{LO} + I_{HI}}{2}$$

I_{LO} @ V_{GS}=½V_{DD}, V_{DS}=V_{DD}

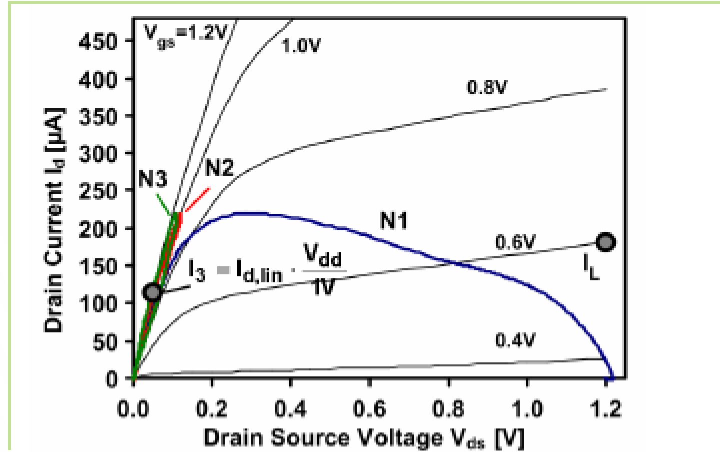
I_{HI} @ V_{GS}=V_{DD}, V_{DS}=½V_{DD}

I_{eff} is better than I_{Dsat} for estimating inverter CV/I switching delay

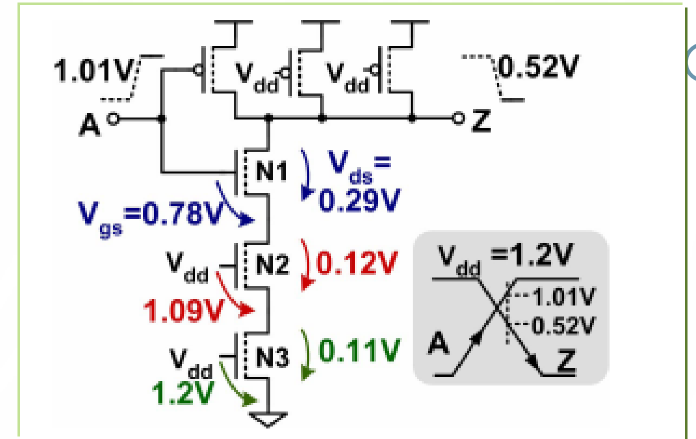
Less DIBL → higher I_{eff} & r_{out} for same I_{Dsat}

Effective Current in Stacks

- Add linear current, I_3



	V_{gs}	V_{ds}
I_H	V_{dd}	$V_{dd}/2$
I_L	$V_{dd}/2$	V_{dd}
I_3	V_{dd}	$0.05 \cdot V_{dd}$

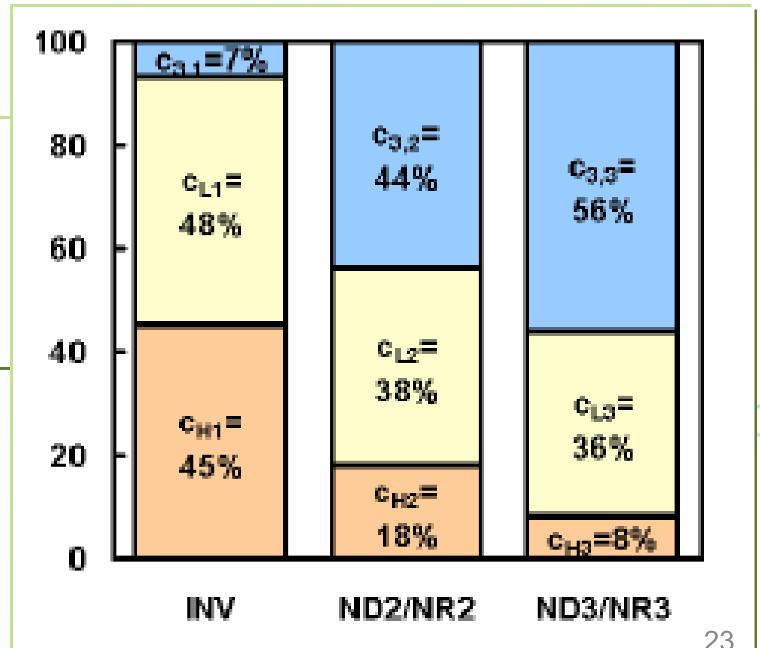


Model: $I_{stack,i} = c_{H,i} I_H + c_{L,i} I_L + c_{3,i} I_3 \Rightarrow$

Inverter: $I_{stack1} = 0.45 \cdot I_H + 0.48 \cdot I_L + 0.07 \cdot I_3$

NAND2/NOR2: $I_{stack2} = 0.18 \cdot I_H + 0.38 \cdot I_L + 0.44 \cdot I_3$

NAND3/NOR3: $I_{stack3} = 0.08 \cdot I_H + 0.36 \cdot I_L + 0.56 \cdot I_3$

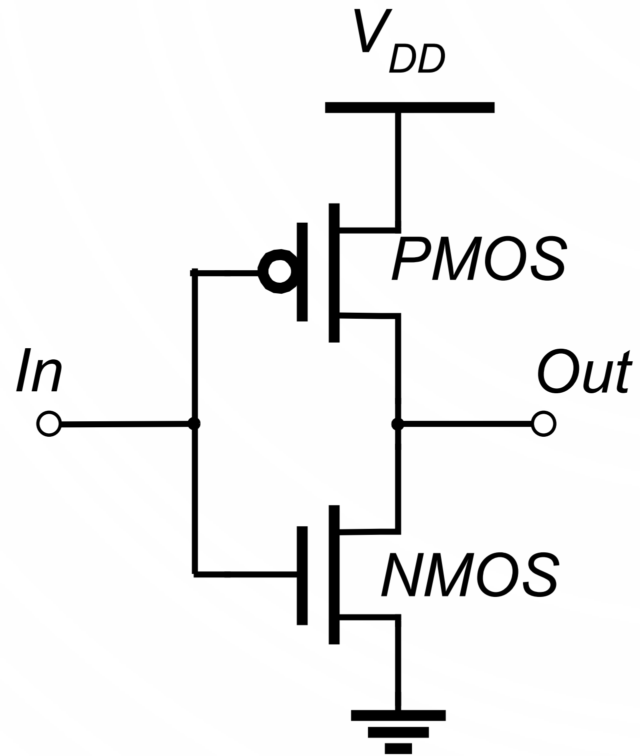


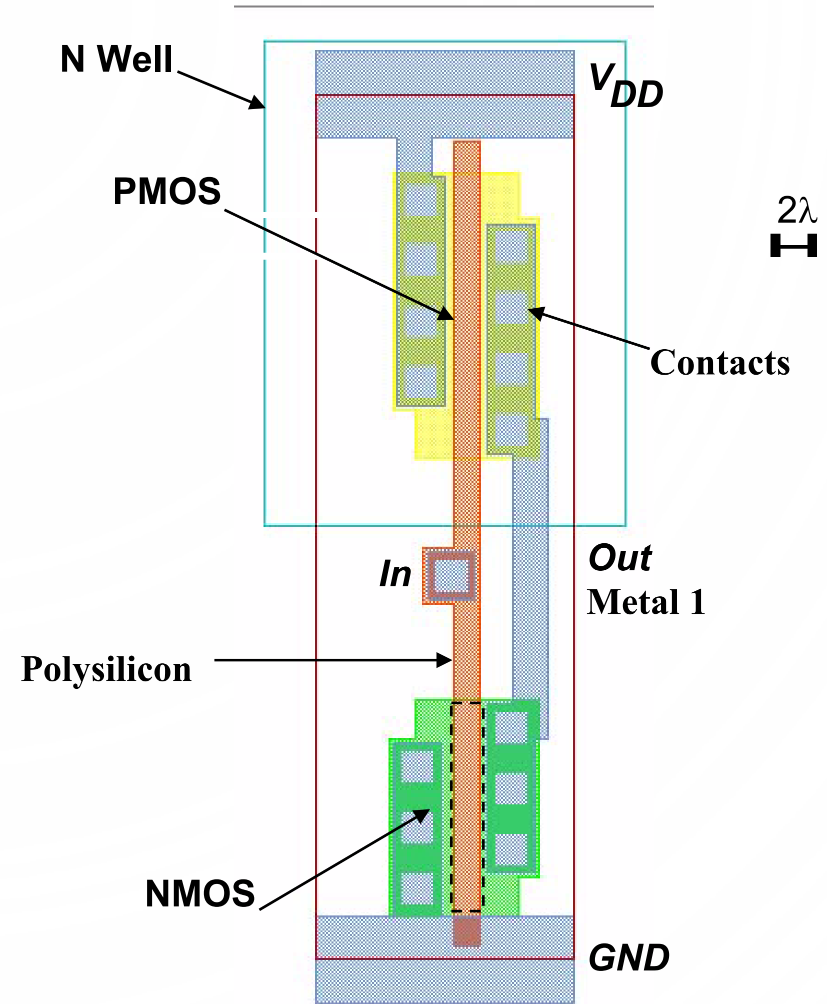
Von Arnim, IEDM'2007

Standard Cells

Standard Cell Inverter

- Schematic and layout
  (in a planar bulk process, ~250nm)



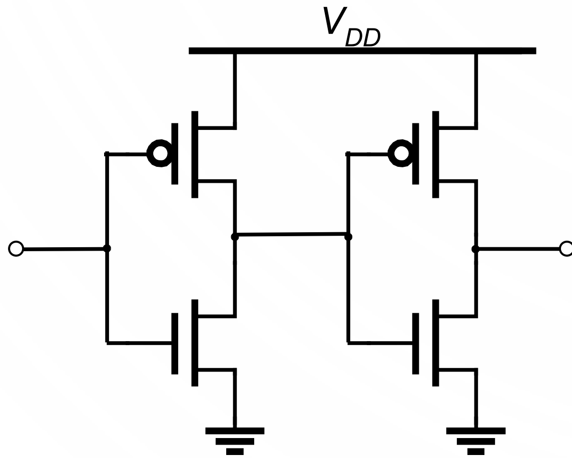


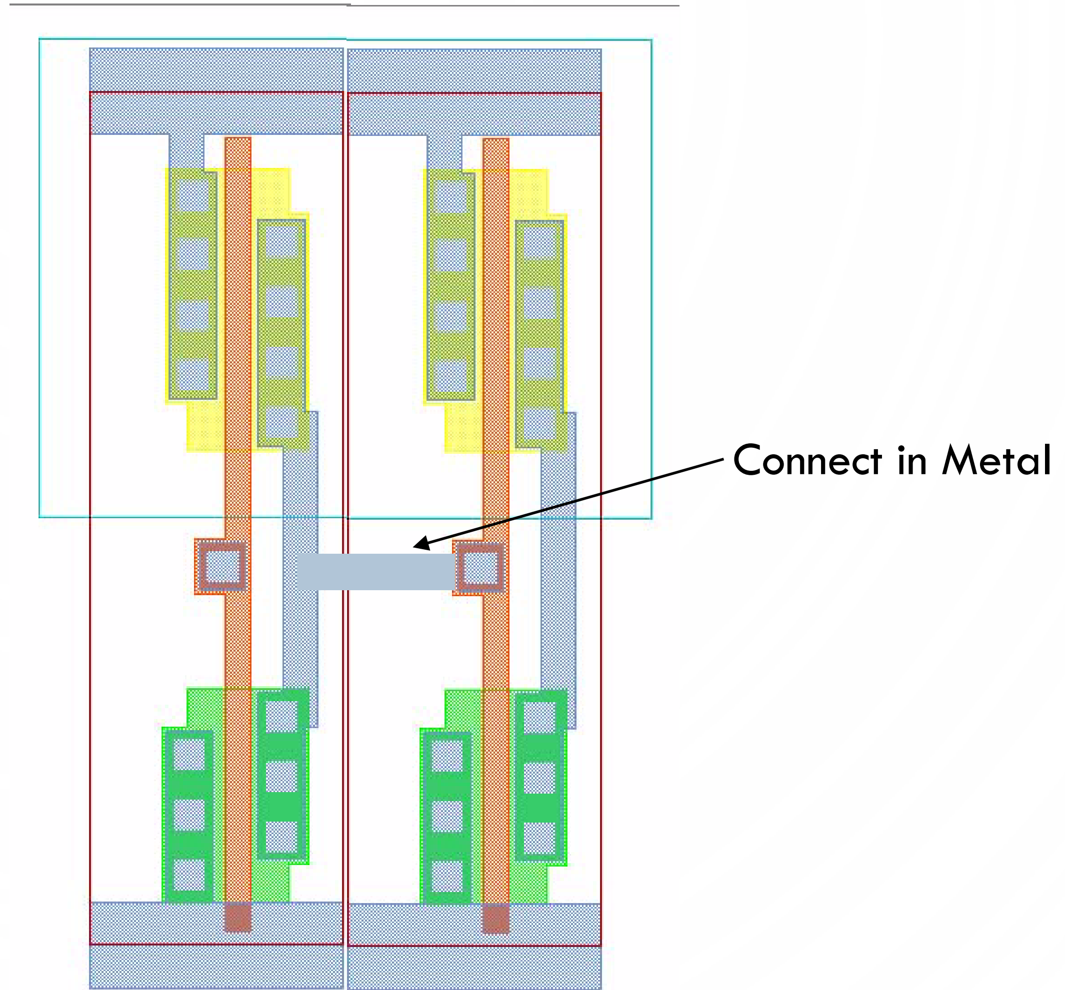
- Pitches are integer multiples of λ

Two Inverters

Share power and ground

Abut cells





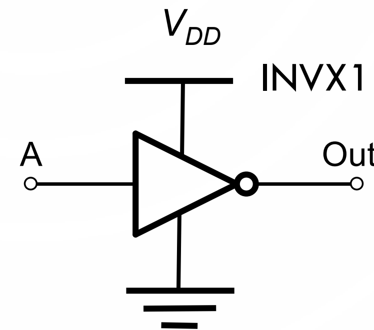
- Delay is additive

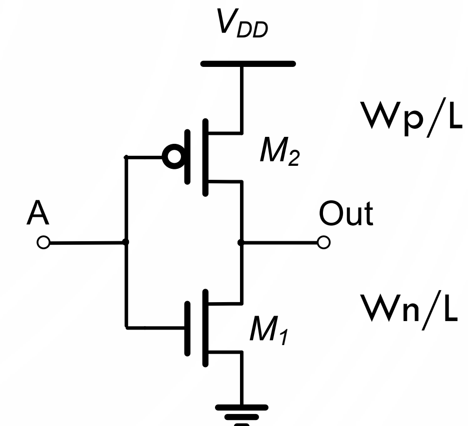
SkyWater 130nm Standard Cells

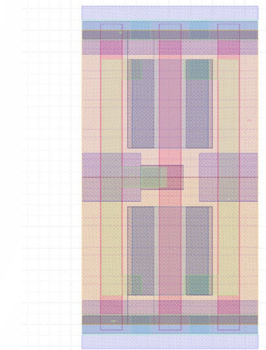
- Library options

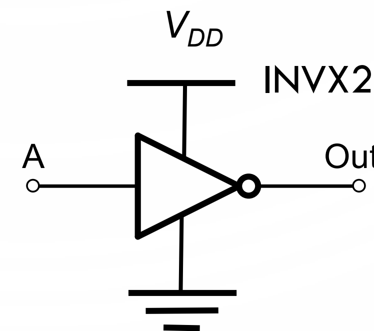
Architecture Comparison	Low Speed	High Density	High Density Low Leakage	High Voltage
TAP BAR	NO	NO	NO	YES
X-GRID	0.480	0.460	0.460	0.480
Y-GRID	0.370	0.340	0.340	0.370
CELL HEIGHT	9 GRIDS	8 GRIDS	8 GRIDS	11 GRIDS
CELL HEIGHT	3.330	2.720	2.720	4.07
NAND2 WIDTH	3 GRIDS	3 GRIDS	4 GRIDS	5 GRIDS
NAND2 WIDTH	1.440	1.380	1.840	2.400
NAND2 AREA	4.7952	3.7536	5.0048	9.770
WPMAX	1.120	1.000	1.000	1.500
WNMAX	0.740	0.650	0.650	0.75

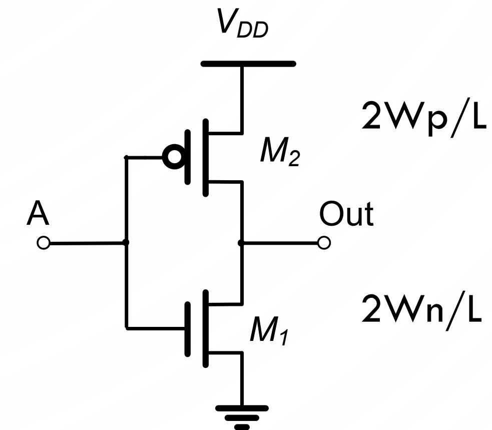
- Multiple gate sizes within a library
  - Symbol
  - Schematic
  - Layout

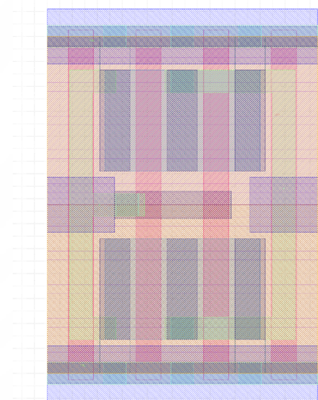










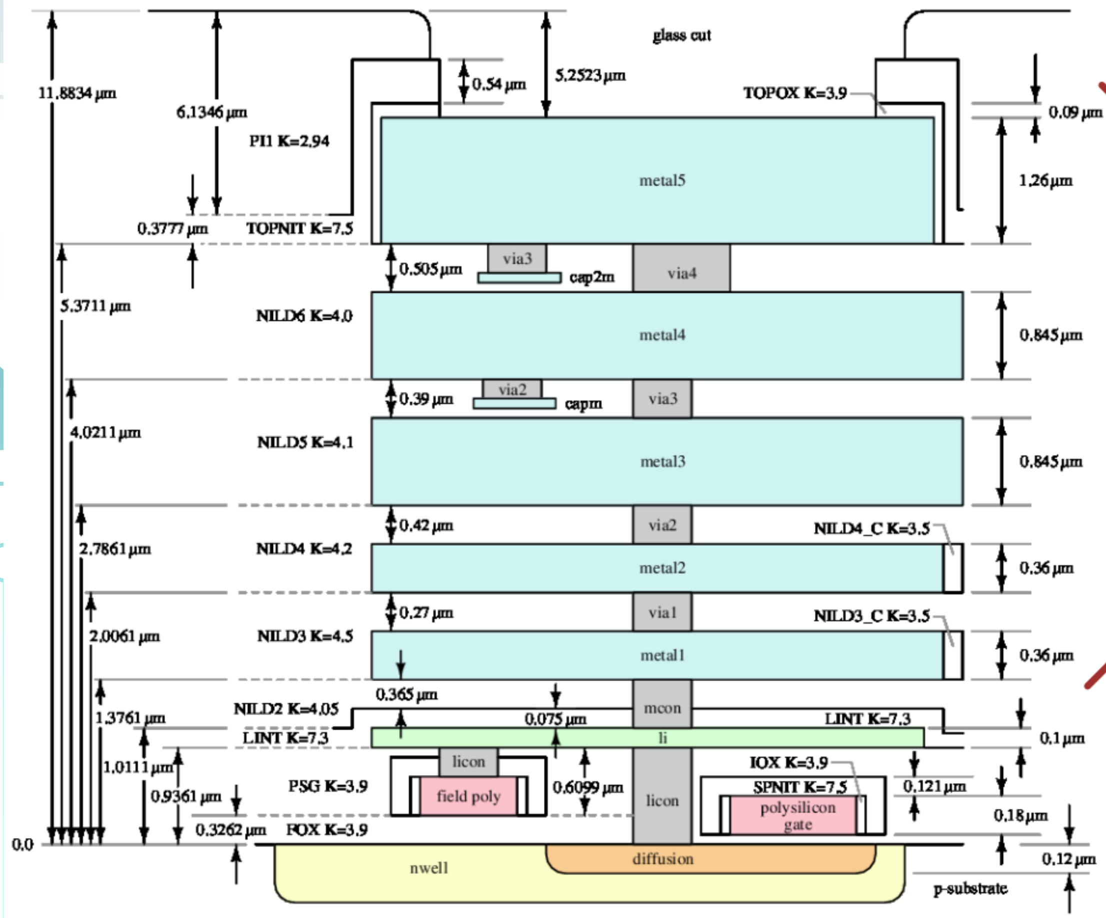


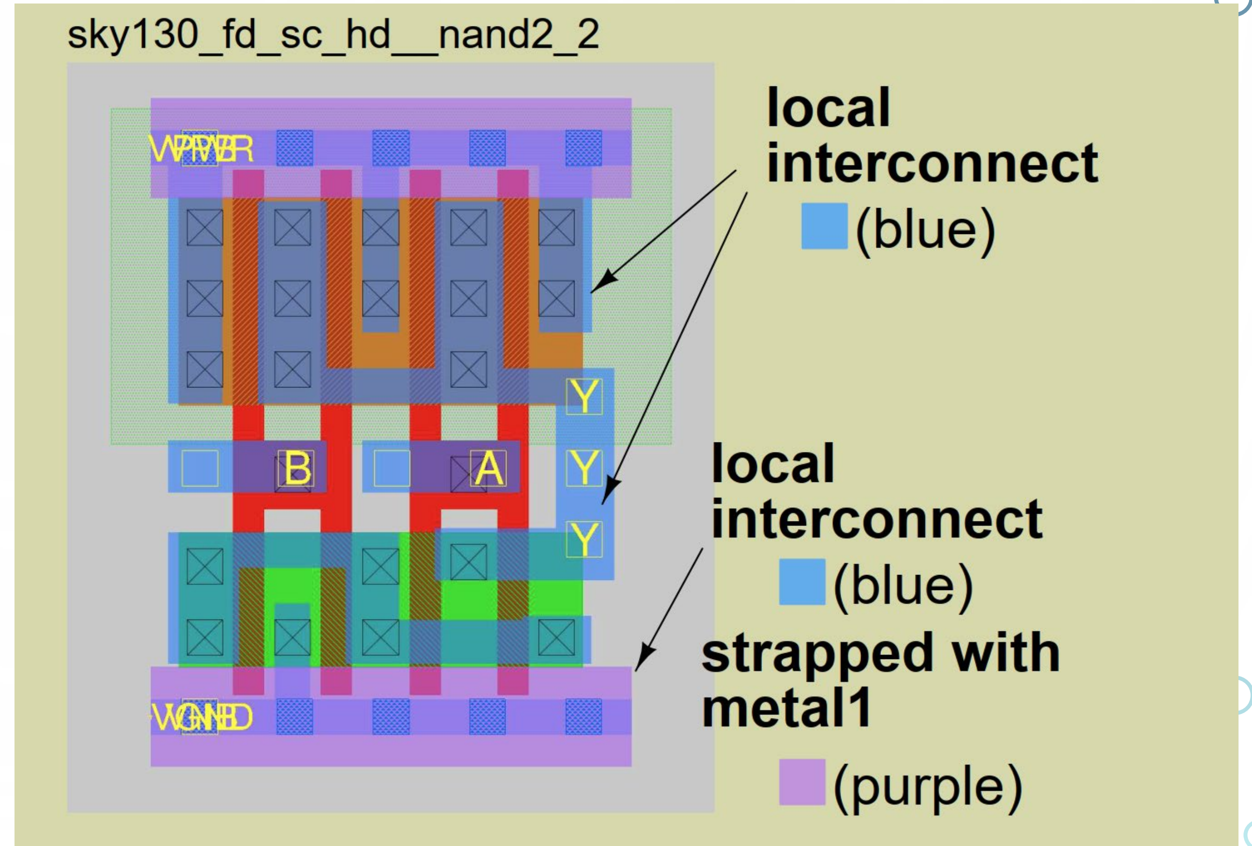
INVX3,

INVX4,…

SkyWater 130nm Standard Cells

Local interconnect





https://isn.ucsd.edu/courses/beng207/lectures/Tim_Edwards_2021_slides.pdf

FinFET Standard Cells

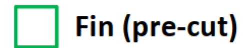
ASAP7

- **Standard cell height selection is application specific**
  - **Related to fins/gate, i.e. drive strength**
- **Gear ratio: fin-to-metal pitch ratio**
  - **Cell height needs to be integer # of fins and (mostly) an integer # of metals accessing the cell pins (e.g. M2)**

V. Vashishtha, ICCAD'17

ASAP7 Standard Cells

- **Cell architecture**
  - **7.5 M2 track height**
    - **Provides good gear ratio with fin, poly, and M2 pitch**



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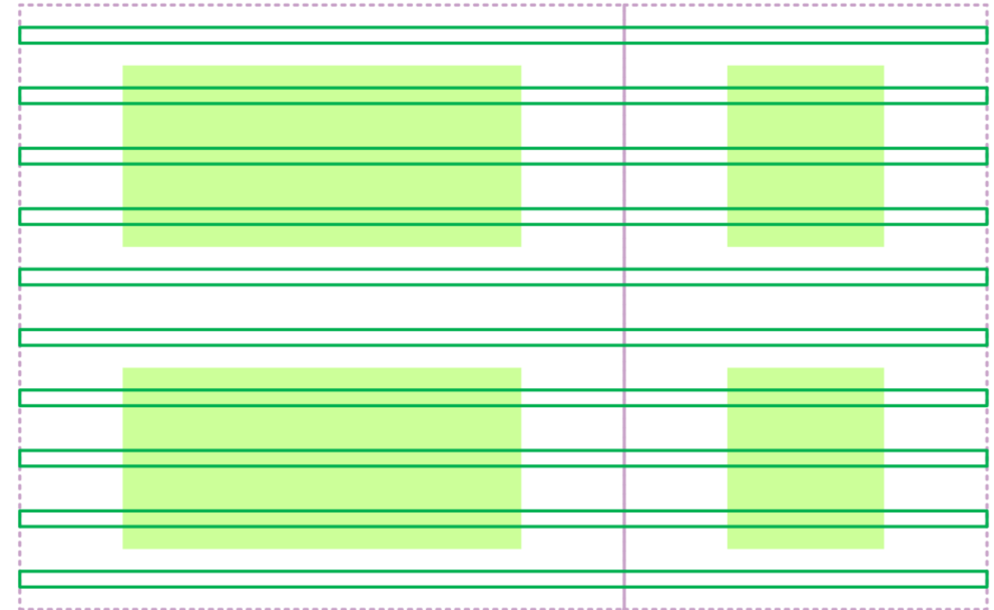

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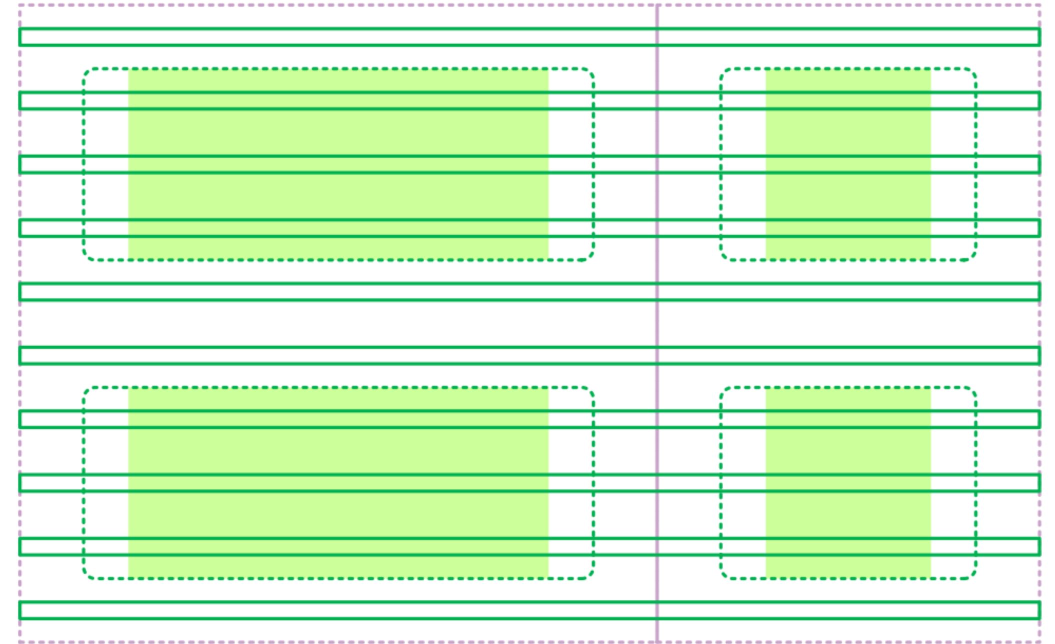

Fin (pre-cut)

Active (drawn)

Active (actual fin block mask)

Cell Boundary

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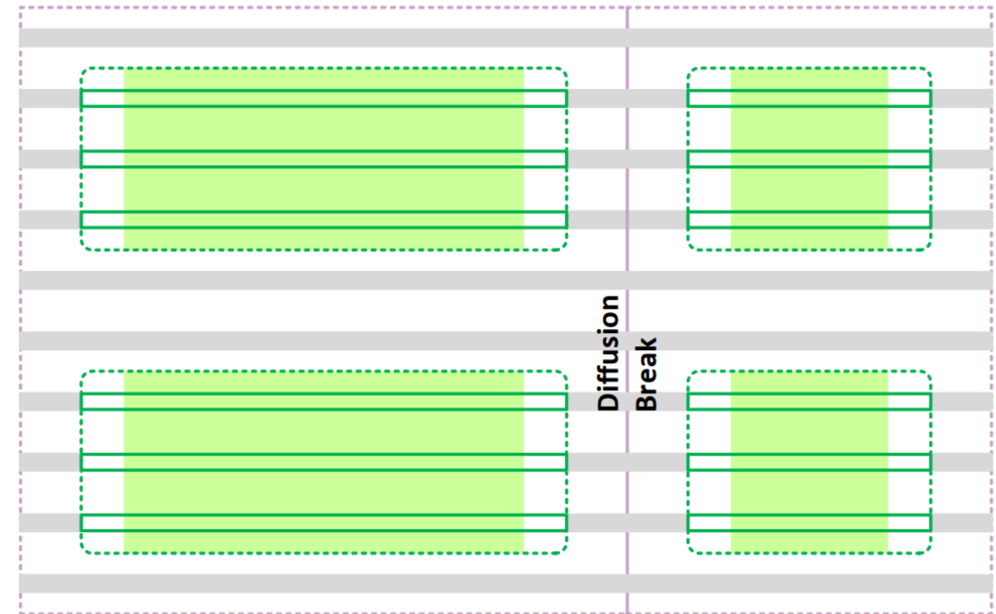
  - **Design rules check for connectivity**



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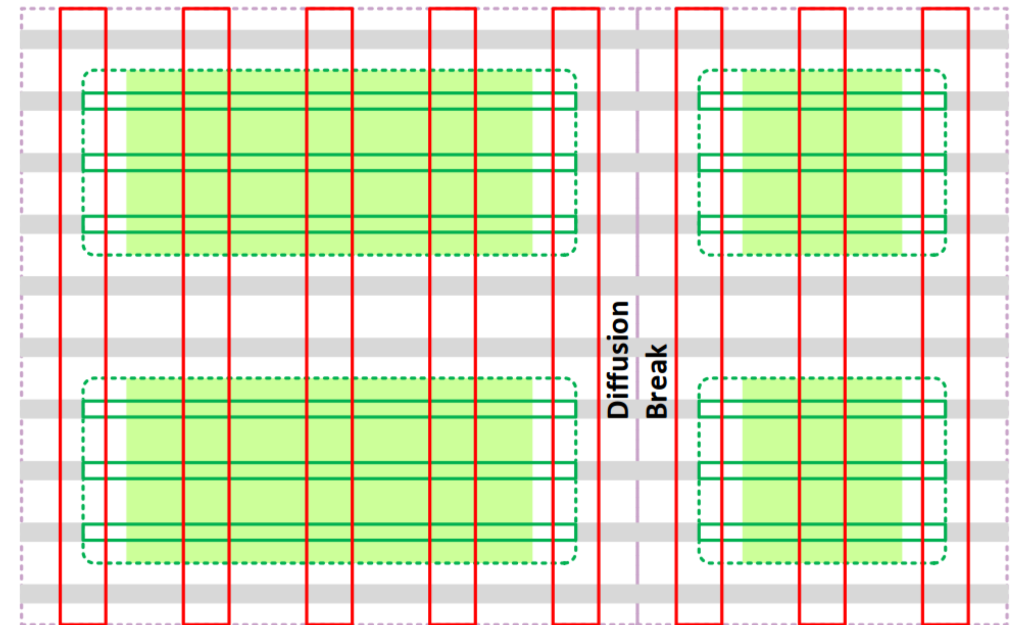

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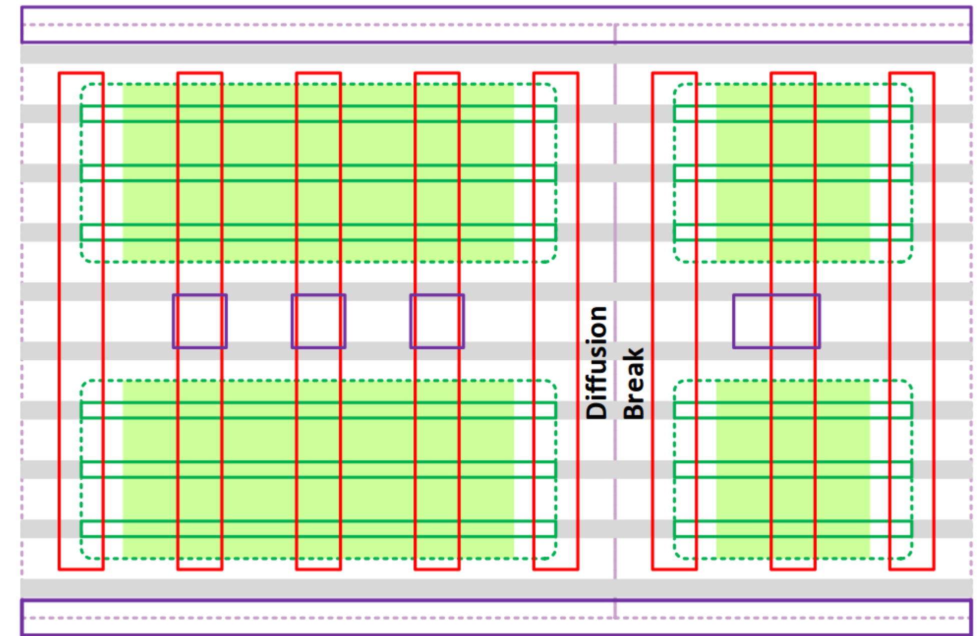

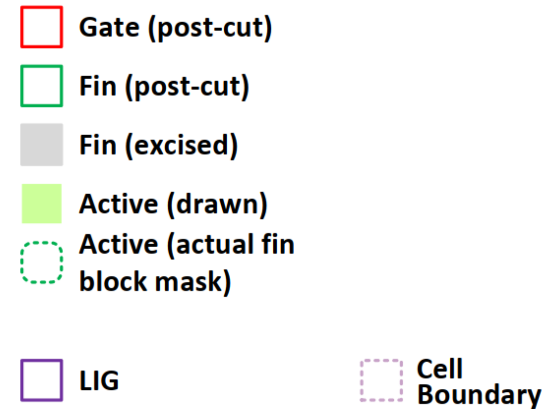

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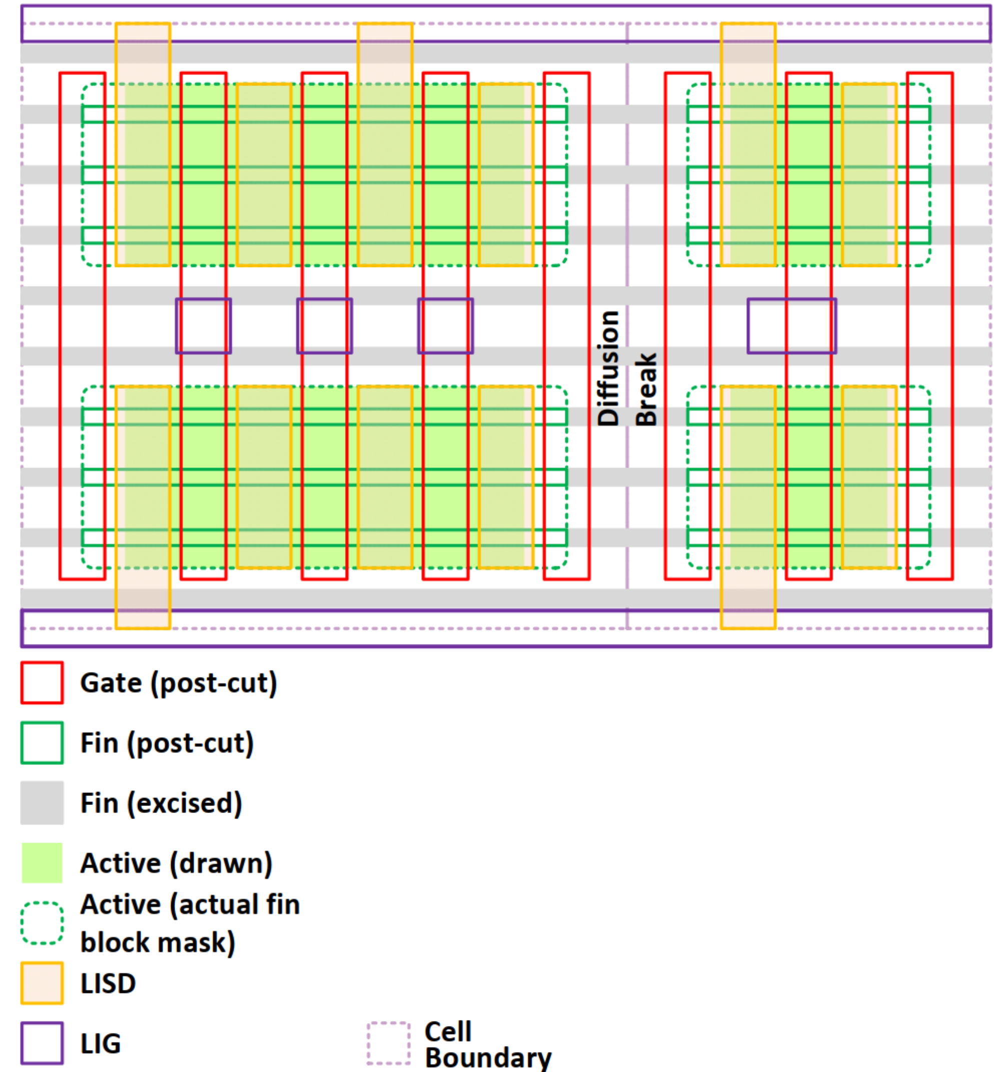

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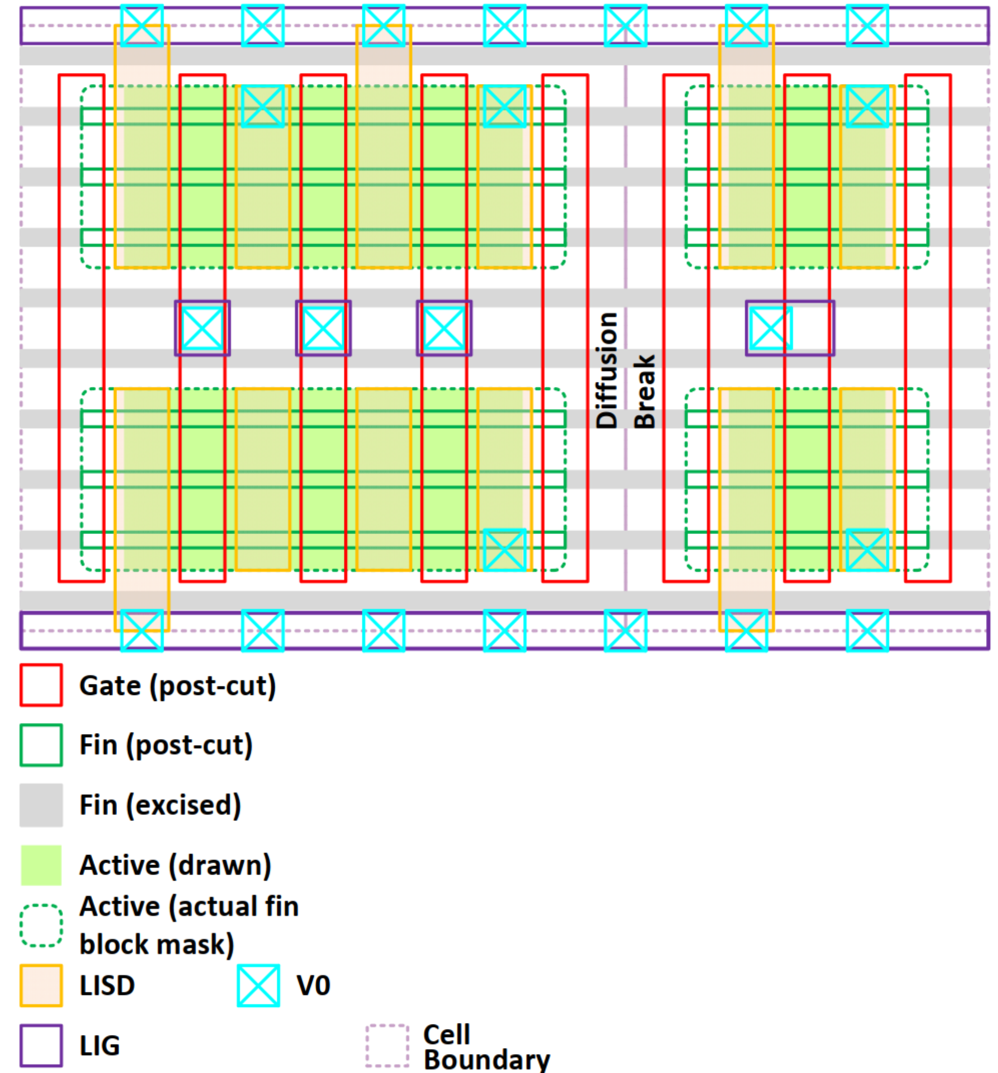

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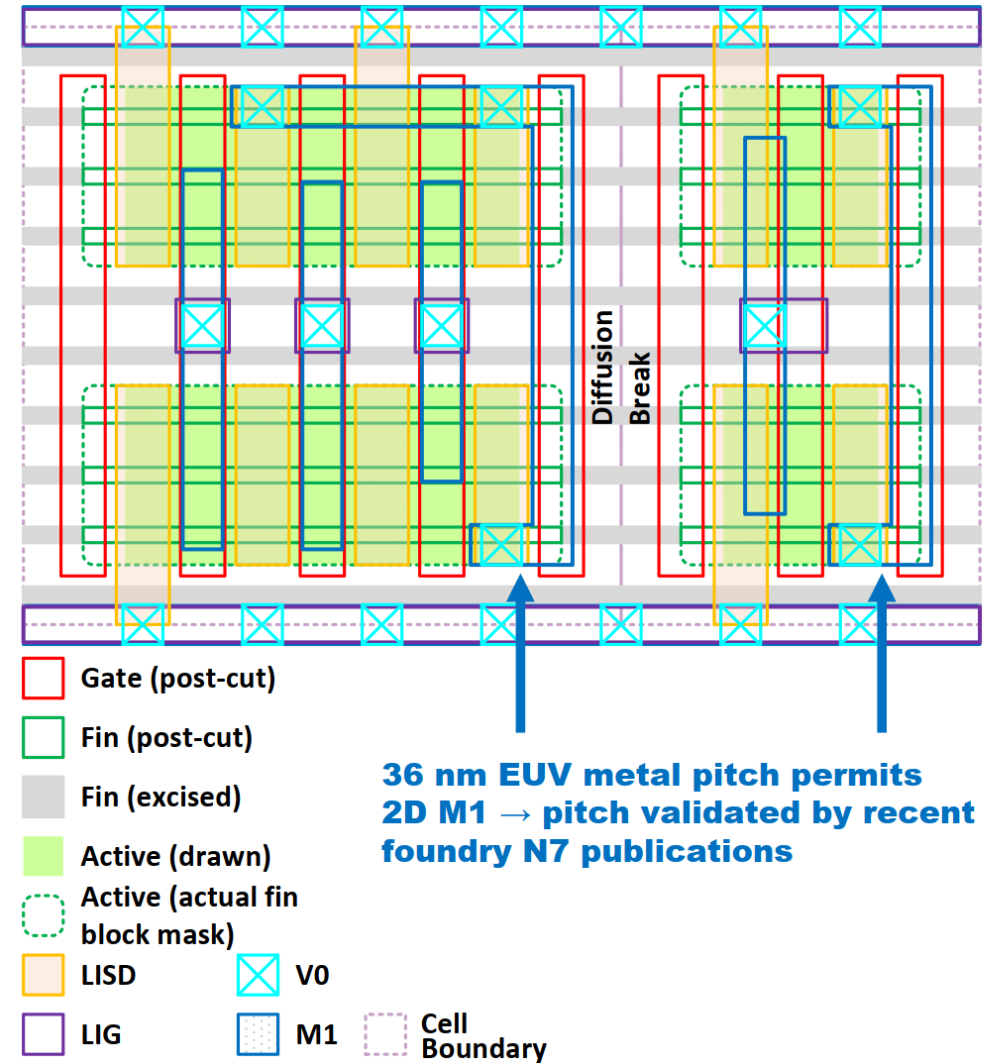

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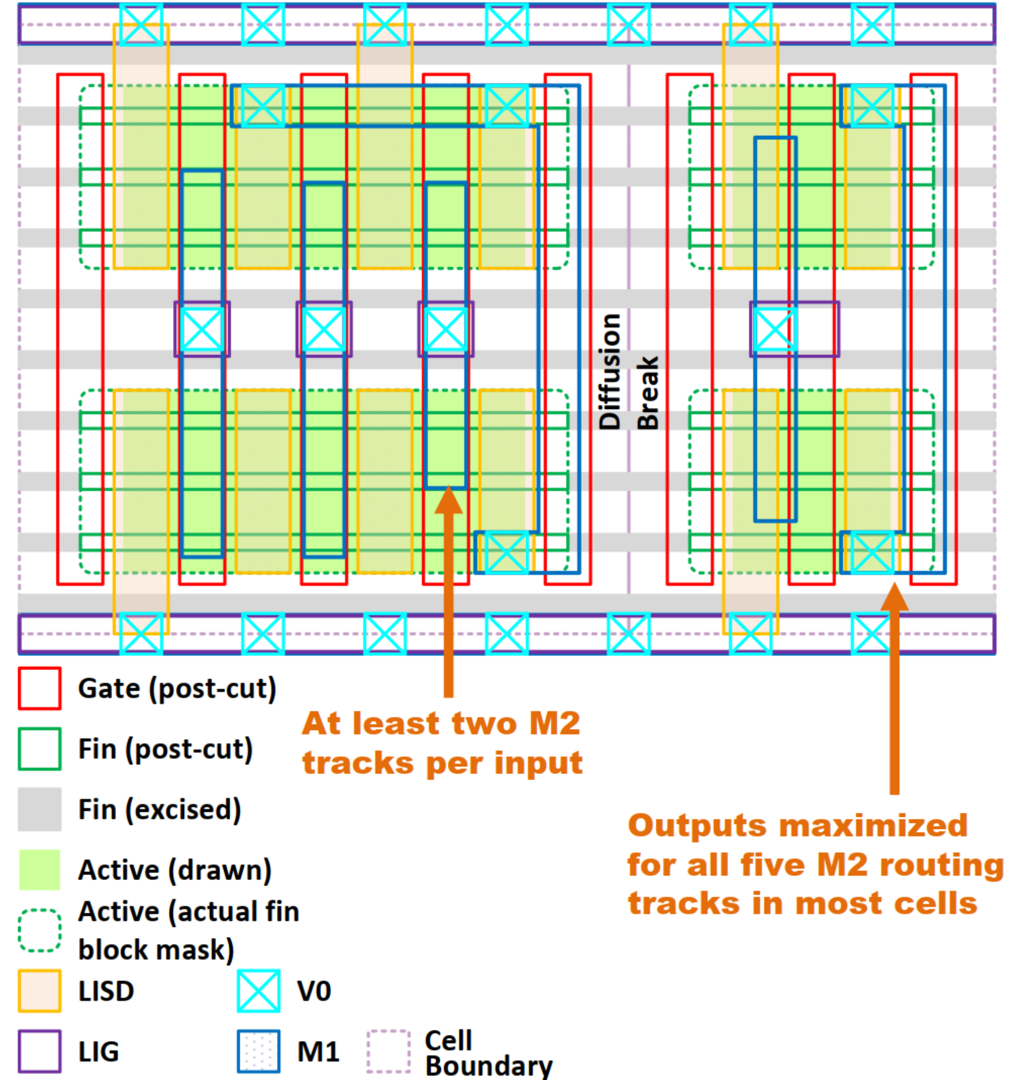

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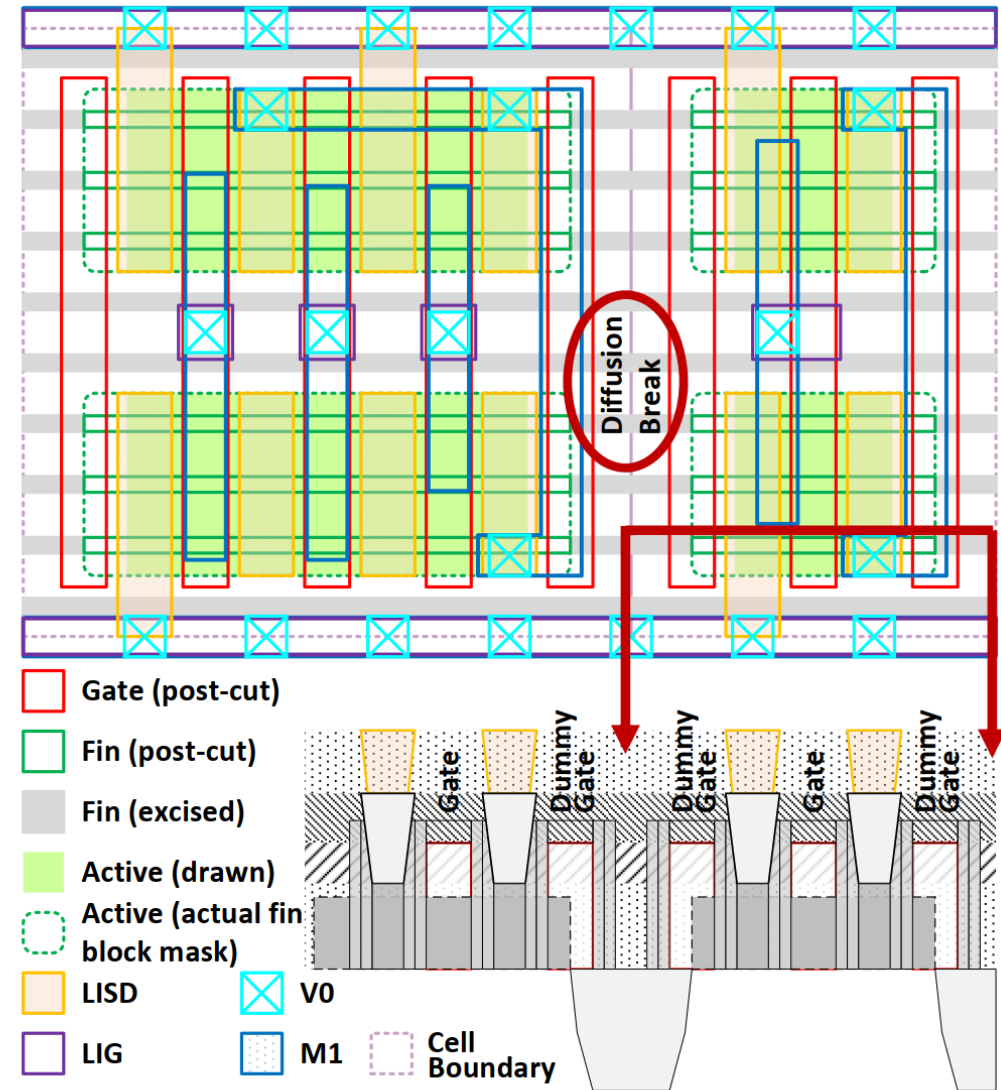
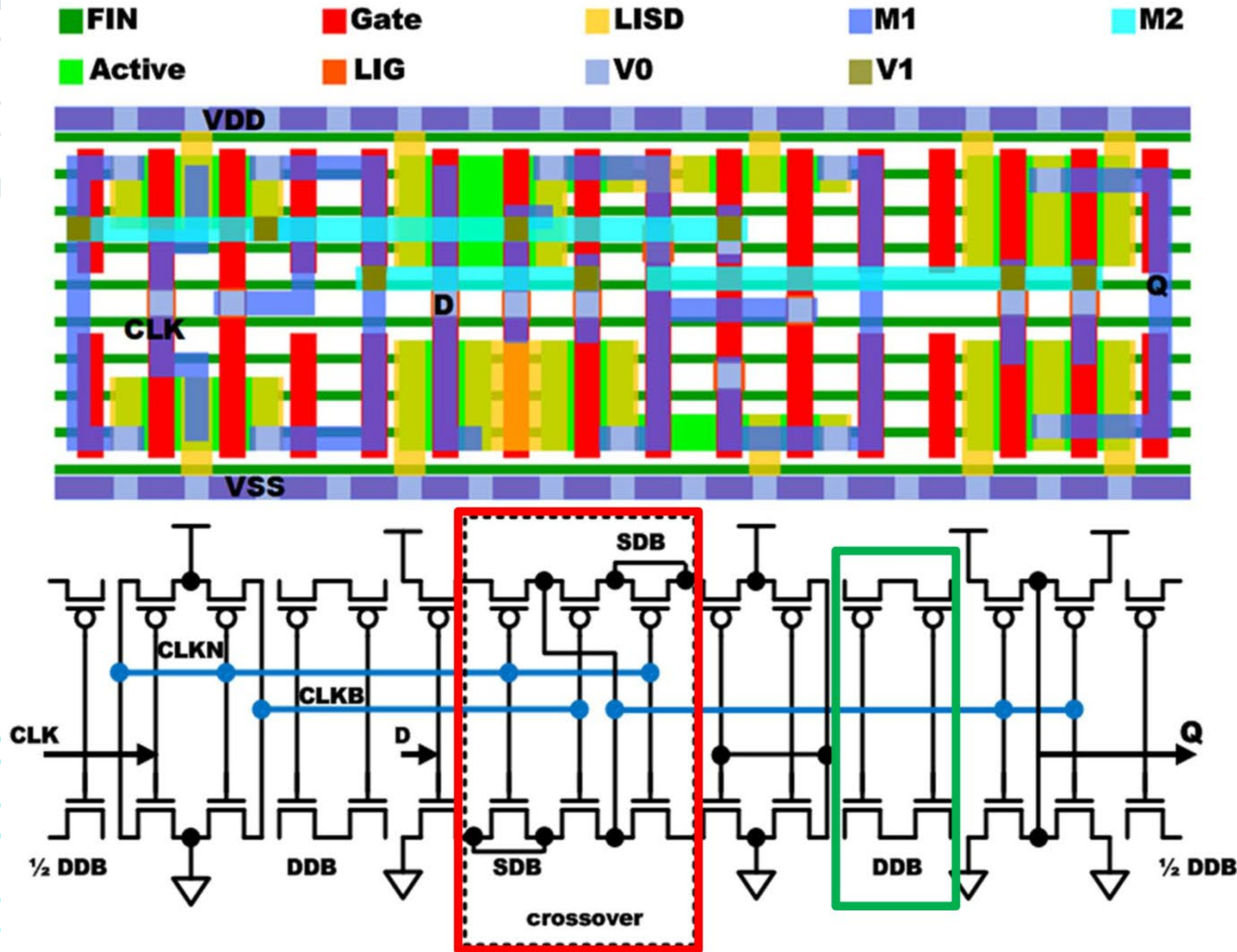
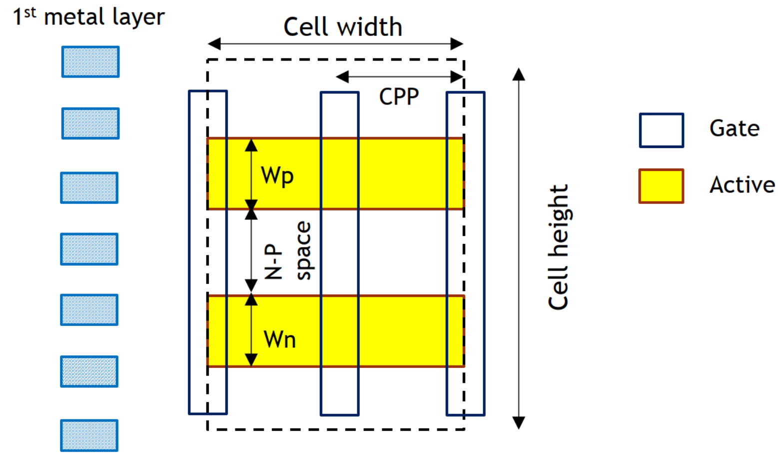


ASAP7 Latch

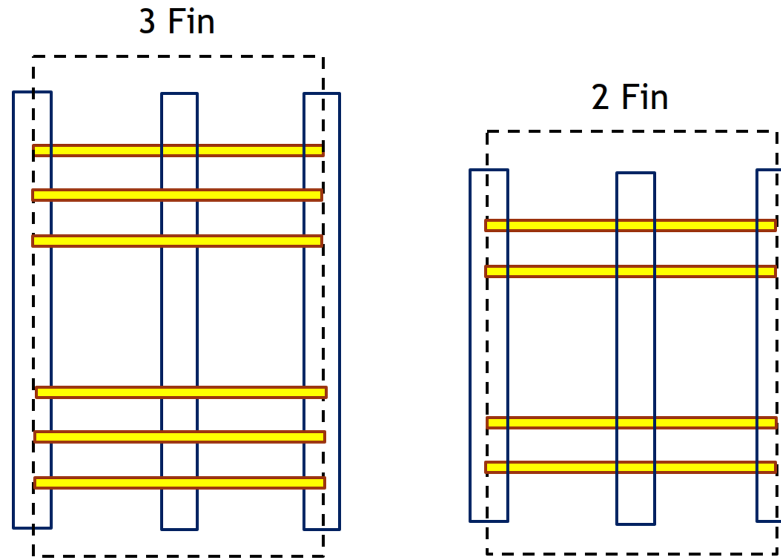


- **This demonstrates a crossover**
  - **Note single diffusion breaks (SBDs)**
  - **Horizontal M2 can only support limited tracks**
- **Intel, Samsung support SDBs (no DDBs) at N10/N7 [EETimes]**

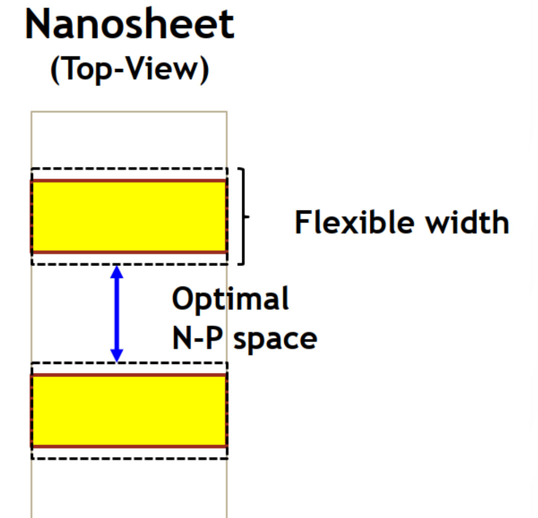
Standard Cell Scaling Beyond N3



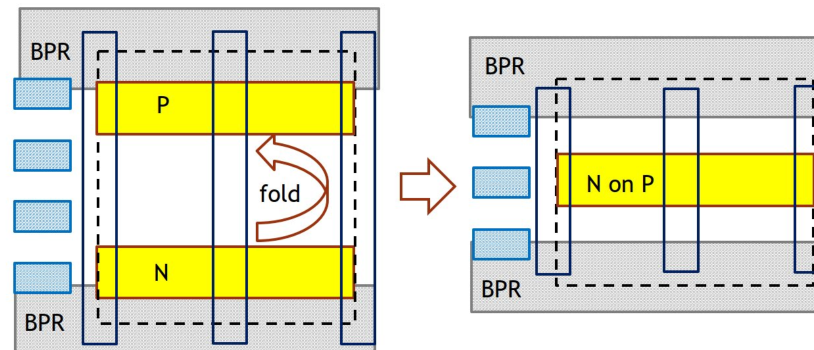
- Fin depopulation



- Nanosheet cell



- Stacked CMOS with buried power rails



Summary

- Leakage is hugely important
- Delay is modeled through equivalent R, C
  - We will see other models later
- Standard cells are an established abstraction layer today

Next Lecture

- Gate models

cc BY NC SA