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EECS251B : Advanced Digital Circuits and Systems

Lecture 16 – Flip-Flops, Variability

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How the A.I. That Drives ChatGPT Will Move Into the Physical World

March 11, 2024, Cade Metz, NY Times. Companies like OpenAI and Midjourney build chatbots, image generators and other artificial intelligence tools that operate in the digital world.

Now, a start-up founded by three former OpenAI researchers is using the technology development methods behind chatbots to build A.I. technology that can navigate the physical world.

Covariant's headquarters in Emeryville, Calif. From left, Andrew Sohn, product manager; Daniel Adelberg, senior software engineer; and Anusha Nagabandi, a research scientist. (NY Times)

Announcements

- Project
  - Midterm reports due next week
  - Preliminary design review after Spring break
- Homework 3 due next week
  - Quiz 2 today

Flip-Flops

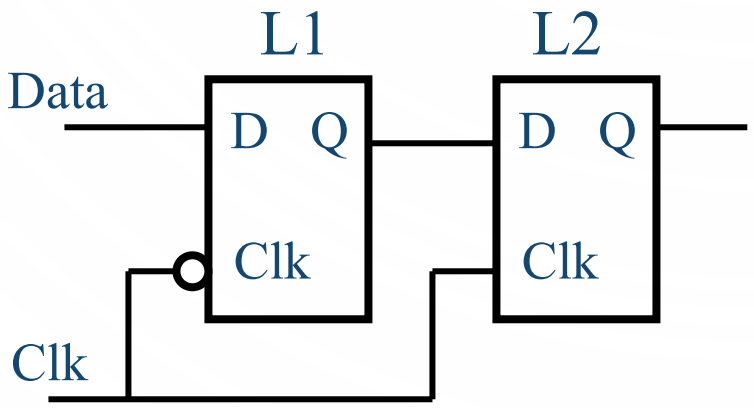
Flip-Flops

- Performance metrics
- Delay metrics
  - Insertion delay
  - Inherent race immunity
  - 'Softness' (Clock skew absorption)
  - Inclusion of logic
  - Small (+constant) clock load
- Power/Energy Metrics
  - Power/energy
- Design robustness
  - Noise immunity

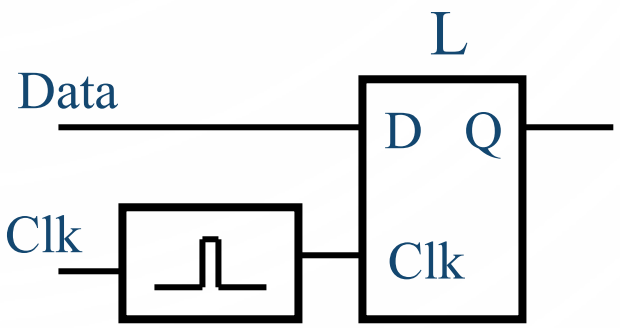
Types of Flip-Flops

- Two ways to design a flip-flop
  - Latch pair (large majority)
  - Pulsed latch

Latch Pair

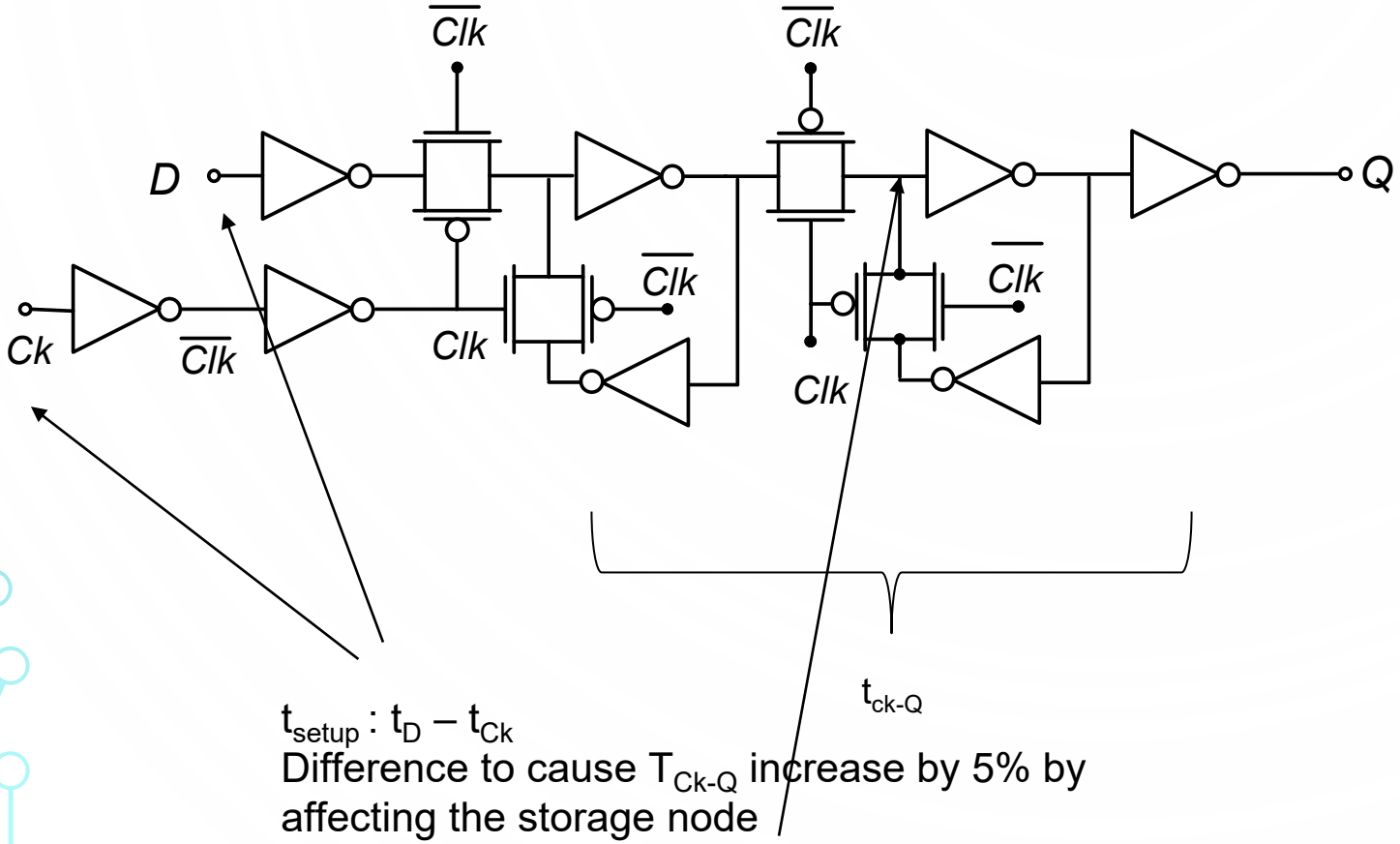


Pulse-Triggered Latch



Flip-Flop (Latch Pair) Clk-Q, setup, hold

Calculation is nearly identical to that of a latch (ignore feedback inverters).
$t_{Clk\text{-}Q}$ is the delay of the second latch, which is about 1FO4;
note that $t_{Ck\text{-}Q}$ should include the delay of the inverter fork



t_{setup} : $t_D - t_{Ck}$
Difference to cause $T_{Ck\text{-}Q}$ increase by 5% by affecting the storage node

Setup time calculation goes the same way!

Flip-Flop Library Timing Characterization

- Combinational logic delay is a function of output load and input slope
- Sequential timing (flip-flop):
  - t_{clk-q} is function of output load and clock rise time
  - t_{Su}, t_H are functions of D and Clk rise/fall times
  - Flip-flop has multiple stages, so the delay is less sensitive to input slope

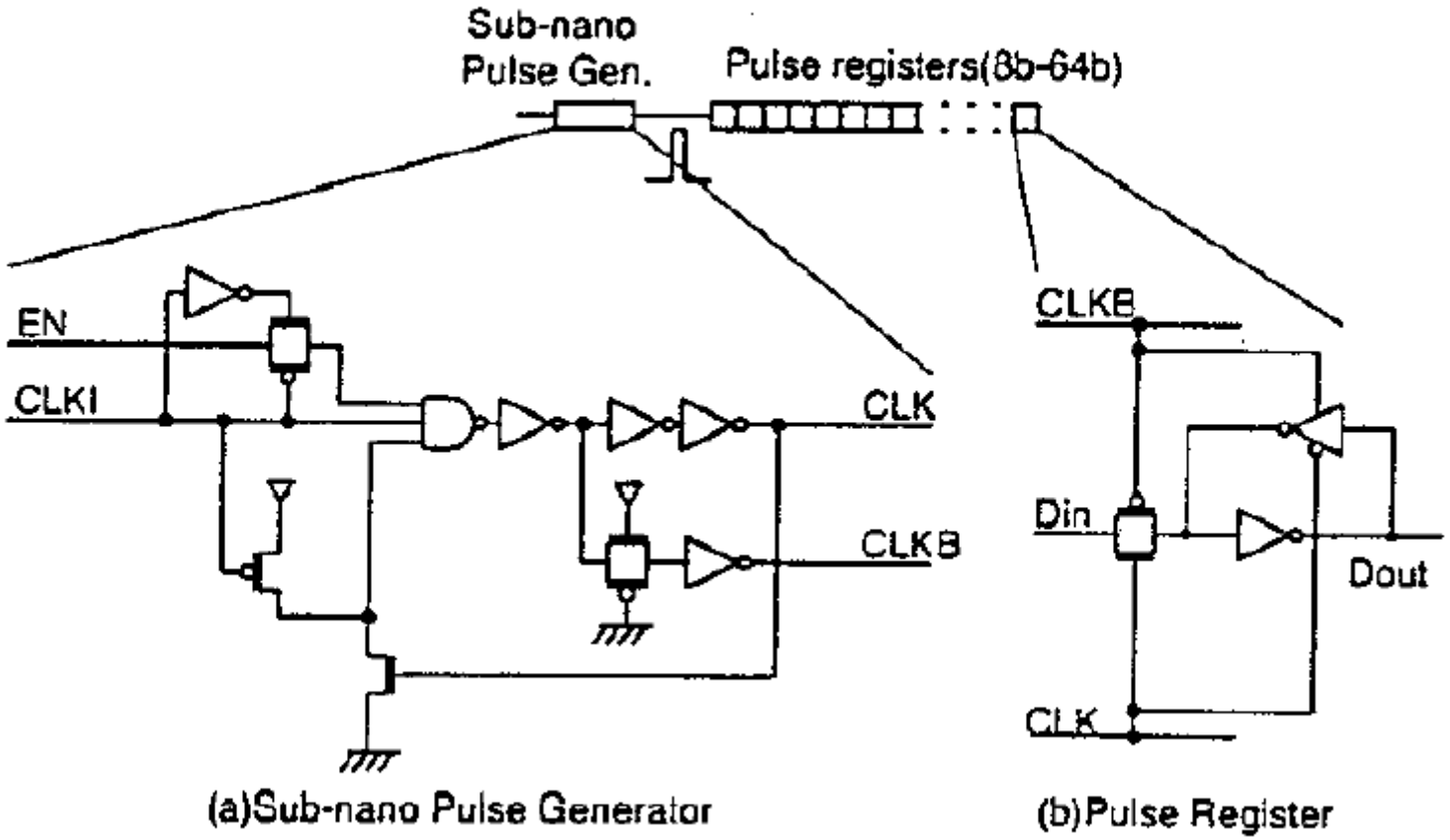
Pulse-Triggered Latches

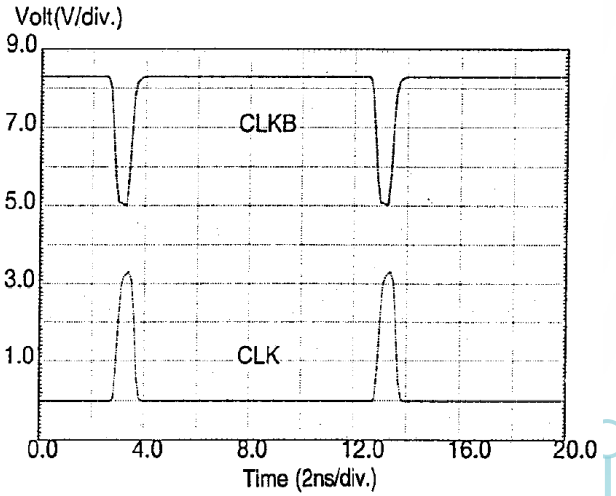
- First stage is a pulse generator
  - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
  - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
- Frequently exhibit a soft edge property

- Note: power is always consumed in the pulse generator
  - Often shared by a group (register)

Pulsed Latch

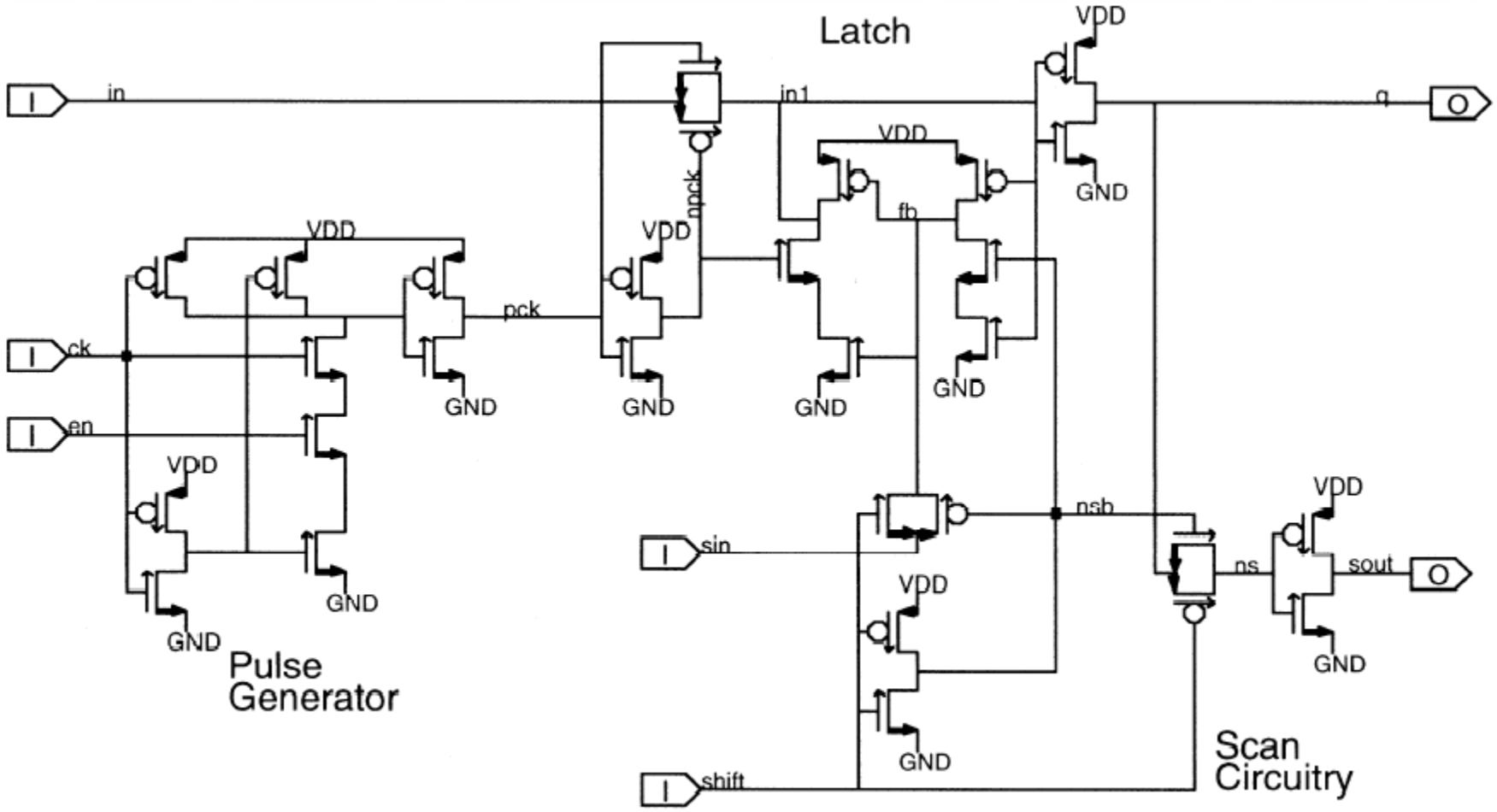
Simple pulsed latch





Kozu, ISSCC'96

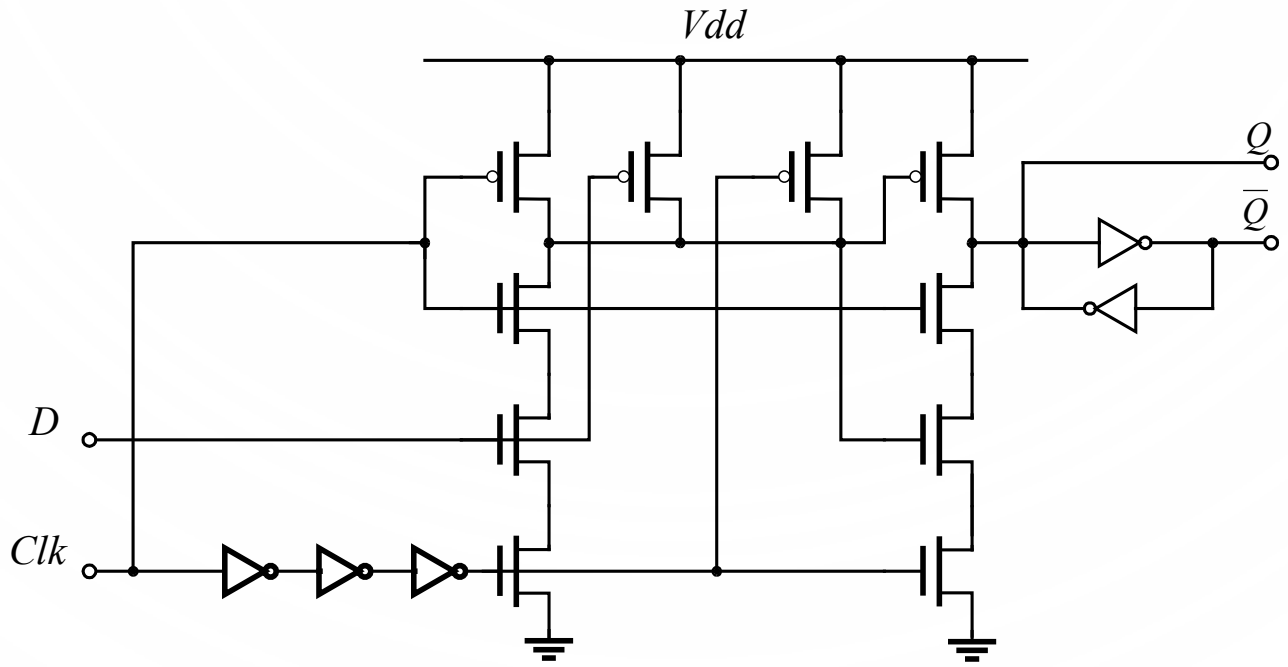
Intel/HP Itanium 2



Naffziger, ISSCC'02

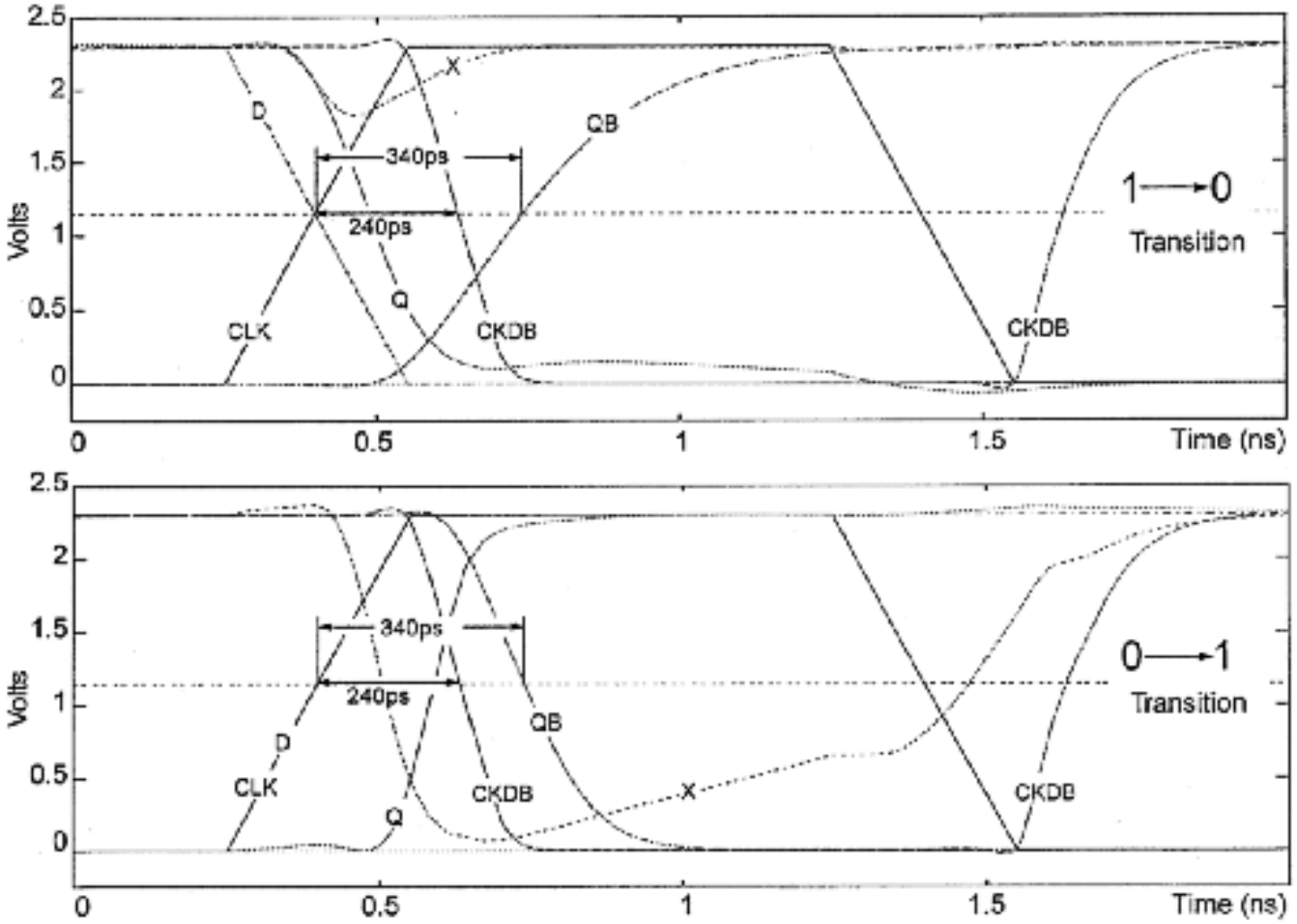
Pulsed Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC'96



HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time

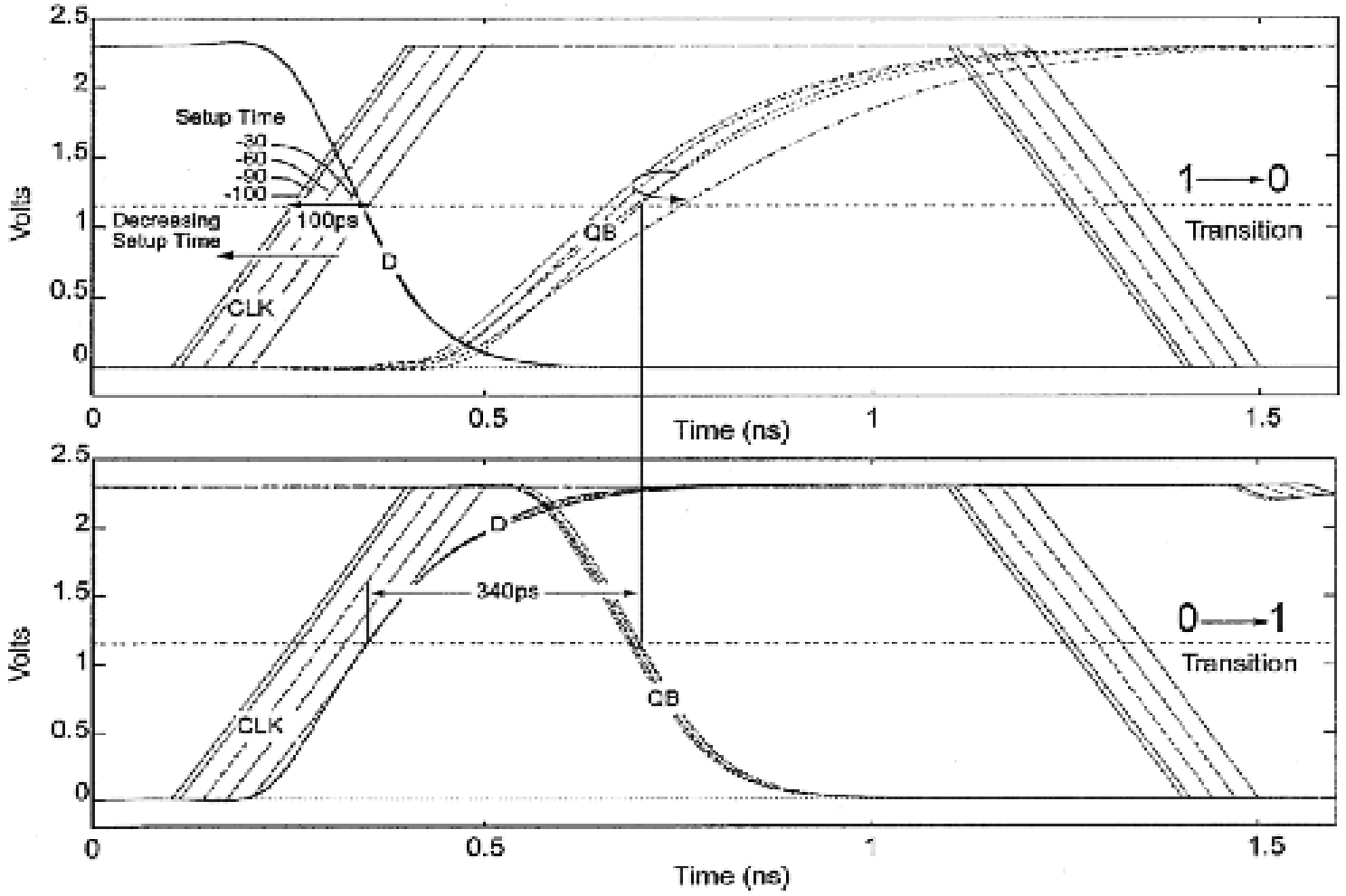


VDD=2.3v, 85°C, Typical Devices
$C_{clk} = 60ff$, $C_{qb} = 300ff$

$T_{cq} = T_{dq} = 340ps$
$T_{hold} = 180ps$
$T_{su(min)} = -90ps$

Hybrid Latch Flip-Flop

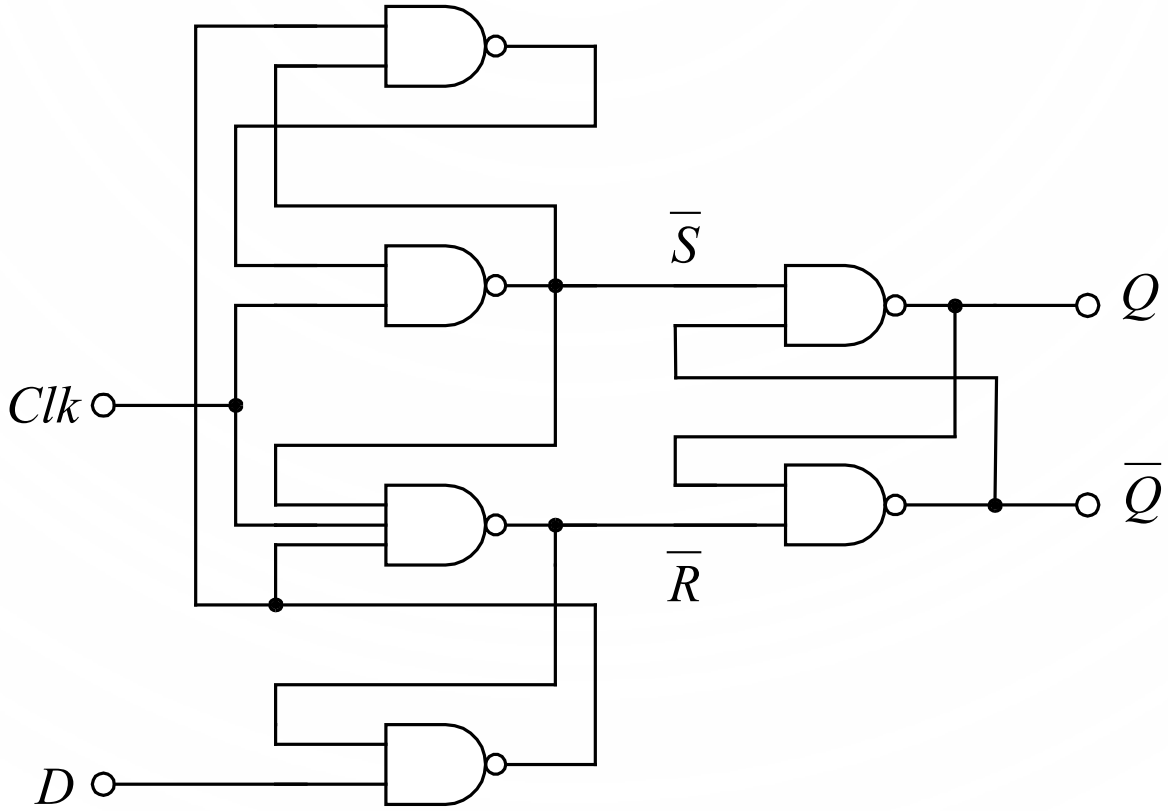
Skew absorption



Partovi *et al*, ISSCC'96

Pulsed Latches

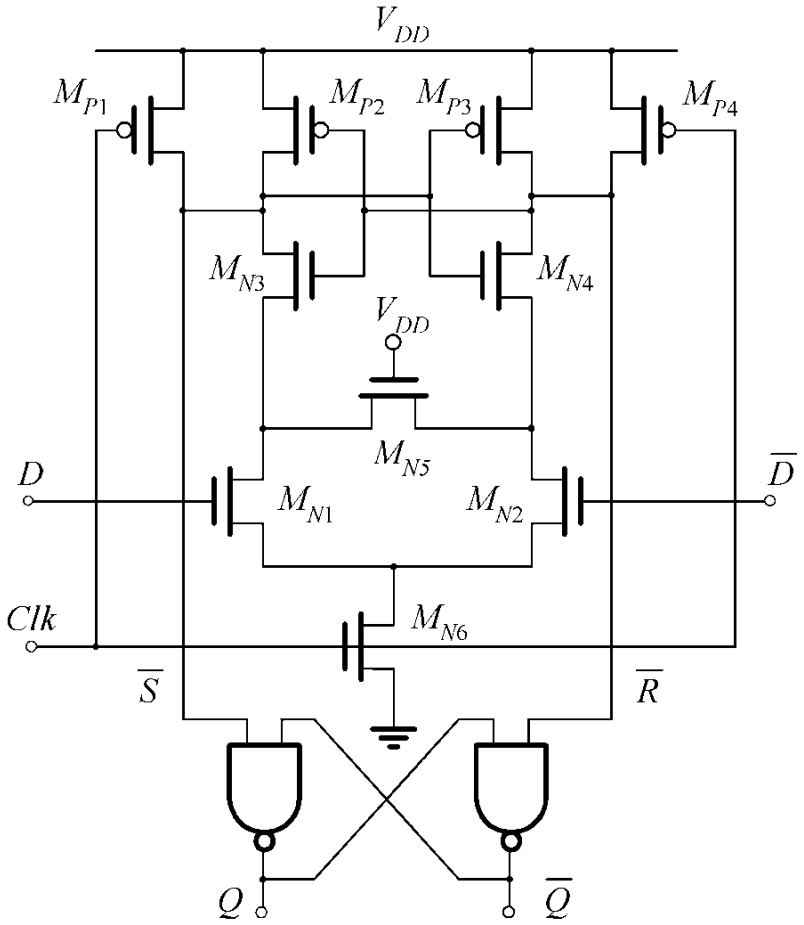
7474, from mid-1960's



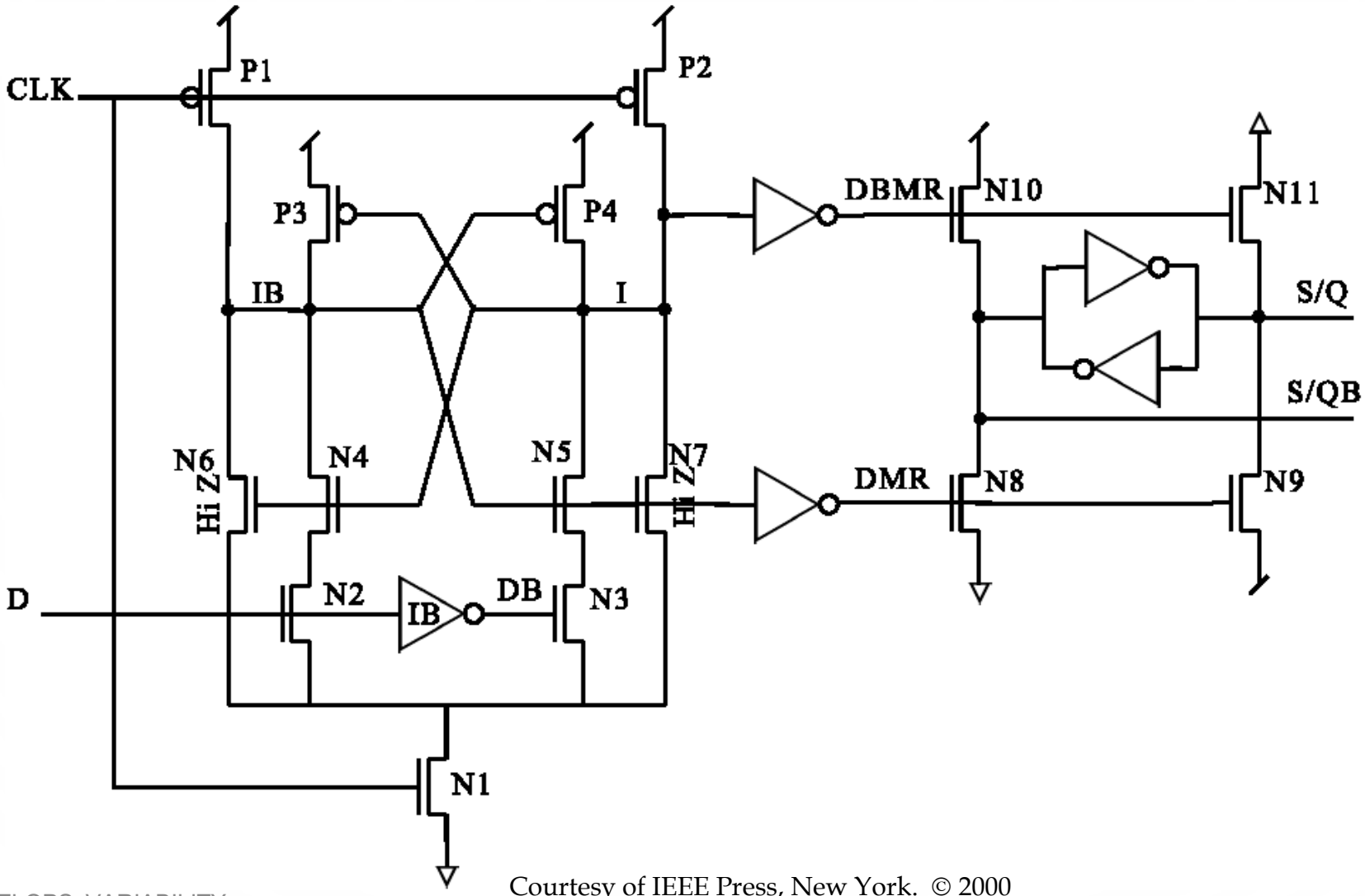
Pulsed Latches

Sense-amplifier-based flip-flop, Matsui 1992.
DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to high, when *Clk* = 0
After rising edge of the clock sense amplifier generates the pulse on
S or *R*
The pulse is captured in
S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges

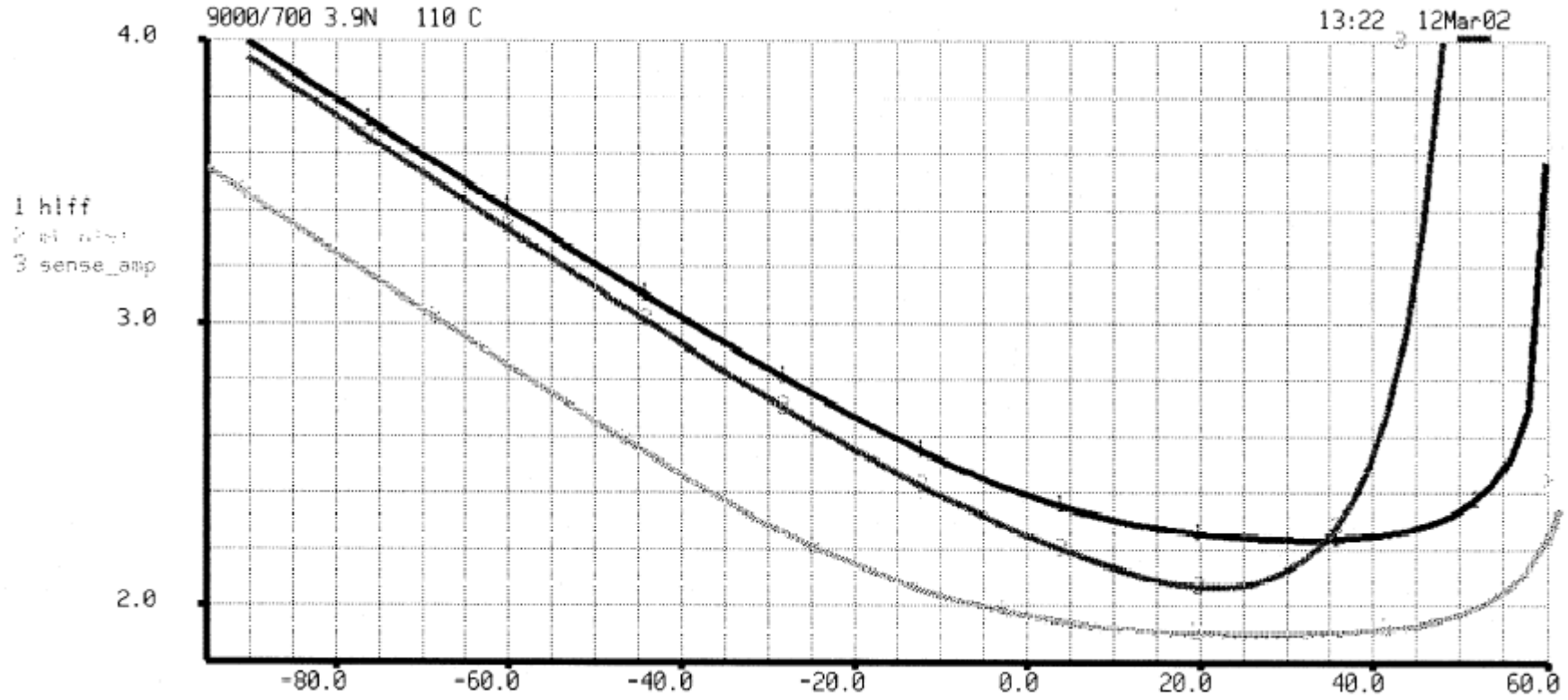


Sense Amplifier-Based Flip-Flop



Courtesy of IEEE Press, New York. © 2000

Sampling Window Comparison



Naffziger, JSSC 11/02

Design Variability Sources and Impact on Design

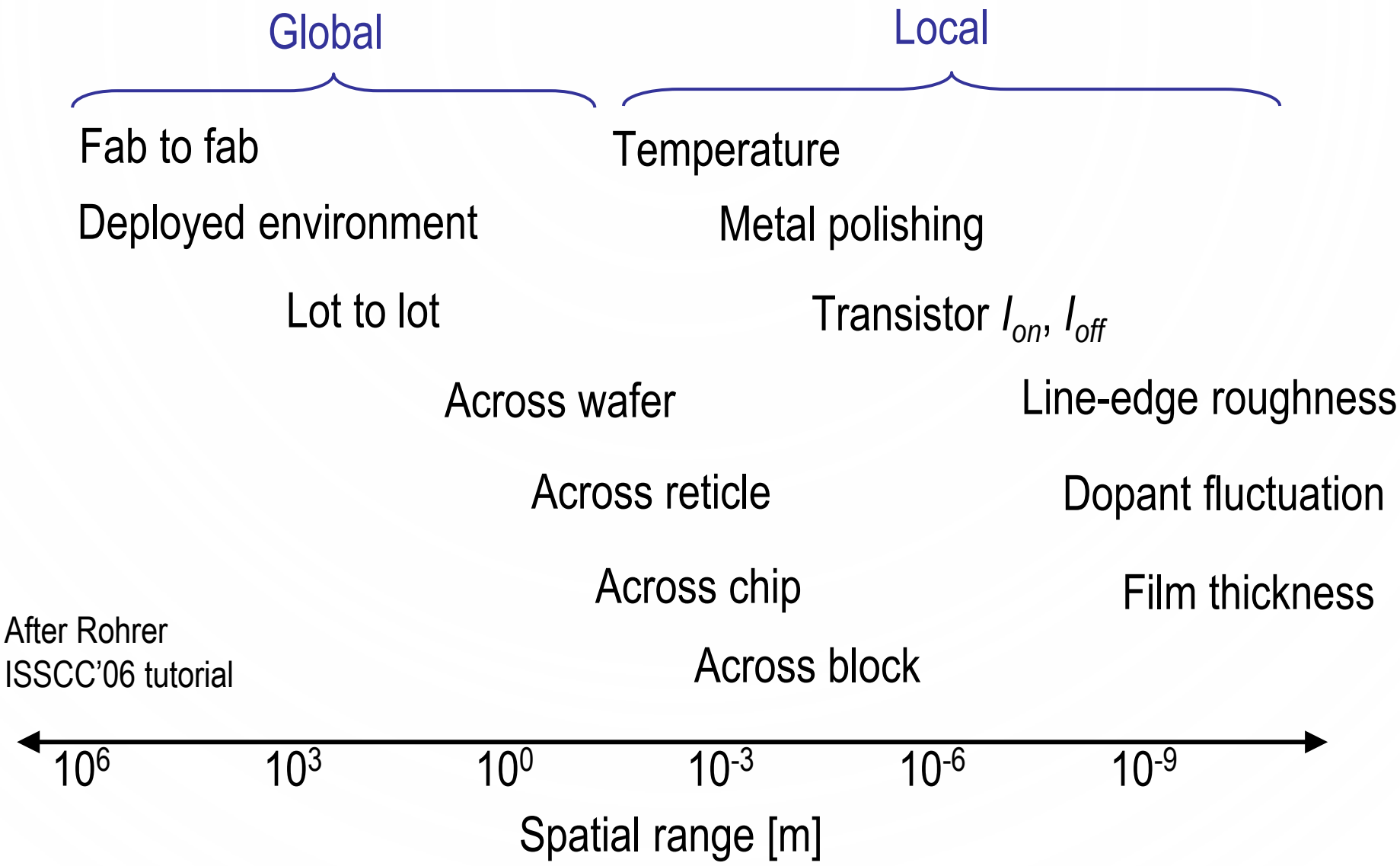
Variability Classification

- Nature of process variability
  - Within-die (WID), Die-to-die (D2D), Wafer-to-wafer (W2W), Lot-to-lot (L2L)
  - Systematic vs. random
  - Correlated vs. non-correlated
- Spatial variability/correlation
  - Device parameters (CD, t_{ox}, …)
  - Supply voltage, temperature
- Temporal variability/correlation
  - Within-node scaling, Electromigration, Hot-electron effect, NBTI, self-heating, temperature, SOI history effect, supply voltage, crosstalk
    [Bernstein, IBM J. R&D, July/Sept 2006]
- Known vs. unknown
  - Goal of model-to-hw correlation is to reduce the unknowns

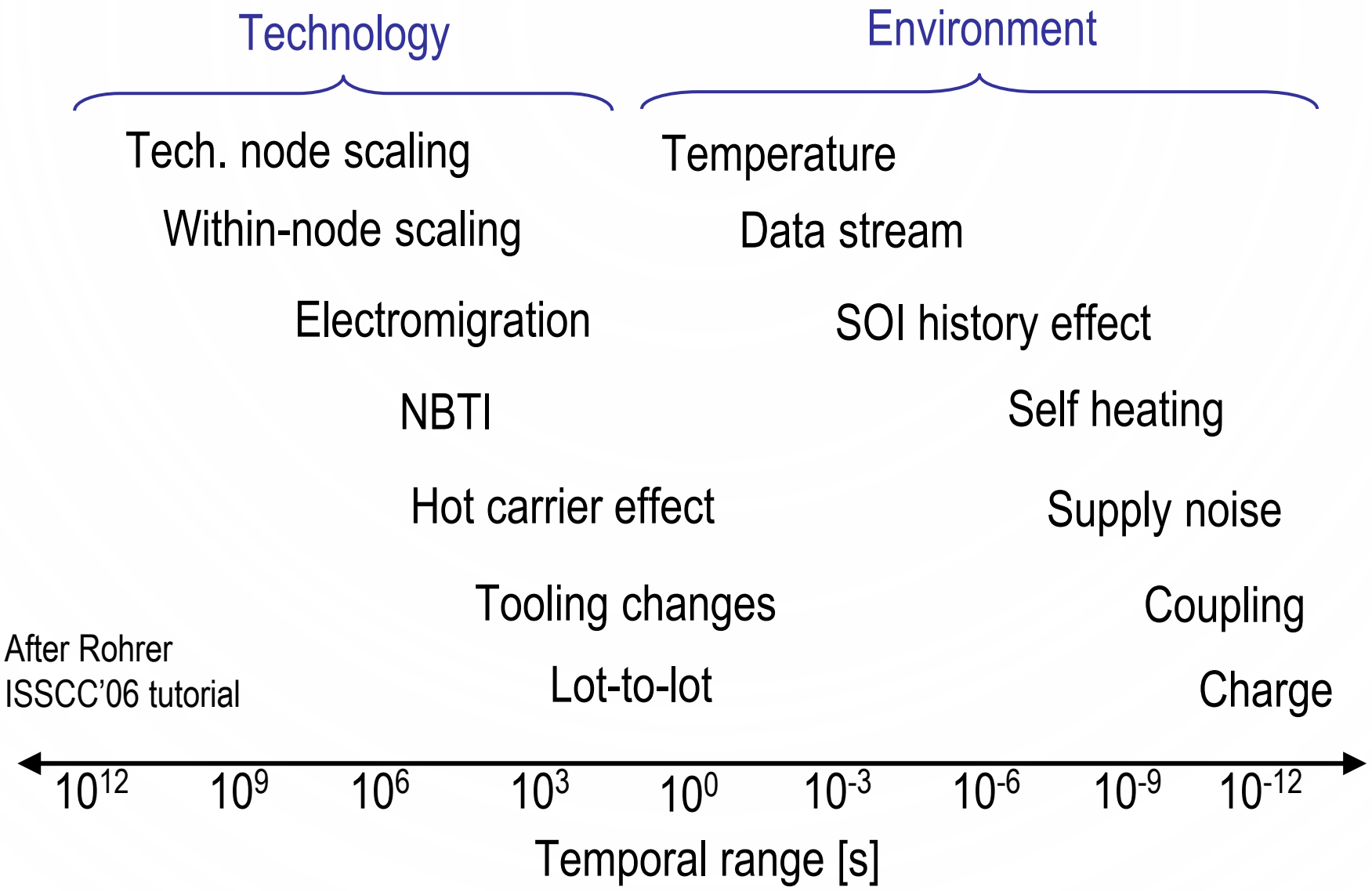
Sources of Variability

- Technology
  - Front-end (Devices)
    - Systematic and random variations in Ion, Ioff, C, …
  - Back-end (Interconnect)
    - Systematic and random variations in R, C
- Environment
  - Supply (IR drop, noise)
  - Temperature

Spatial Variability



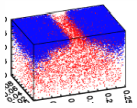
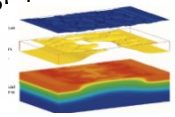
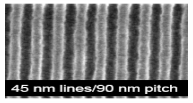
Temporal Variability



Systematic vs. Random Variations

- Systematic
  - A systematic pattern can be traced down to lot-to-lot, wafer-to-wafer, within reticle, within die, from layout to layout,…
  - Within-die: usually spatially correlated
- Random
  - Random mismatch (dopant fluctuations, line edge roughness,…)
  - Things that are systematic, but e.g. change with a very short time constant (for us to do anything about it). Or we don't unedrstand it well enough to model it as systematic. Or we don't know it in advance ("How random is a coin toss?").
- Unknown

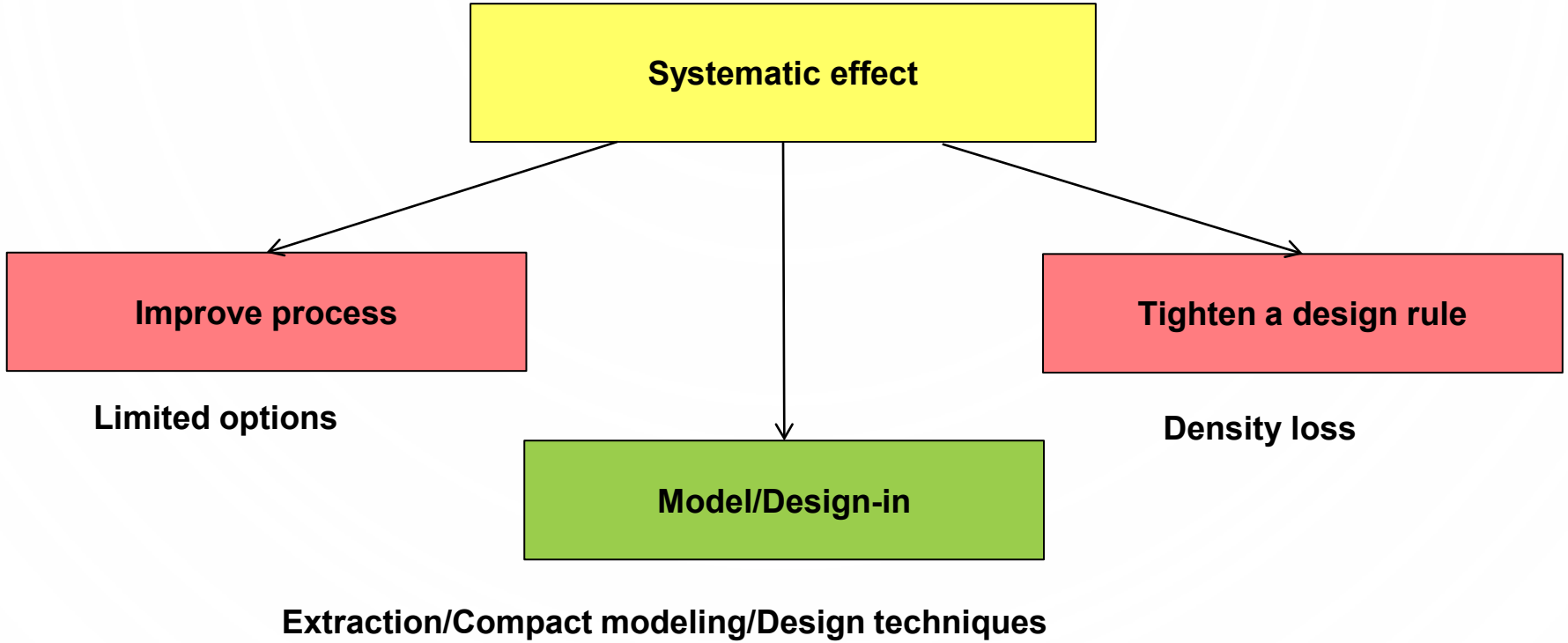
Systematic and Random Device Variations

Parameter	Random	Systematic
Channel Dopant Concentration Nch	Affects σ_{VT} [1] 	Non uniformity in the process of dopant implantation, dosage, diffusion
Gate Oxide Thickness Tox	Si/SiO_2 & SiO_2/Poly-Si interface roughness[2] 	Non uniformity in the process of oxide growth
Threshold Voltage V_T (non Nch related)	Random anneal temperature and strain effects	Non-uniform annealing temperature[5] (metal coverage over gate) Biaxial strain
Mobility μ	Random strain distributions	Systematic variation of strain in the Si due to STI, S/D area, contacts, gate density, etc
Gate Length L	Line edge roughness (LER)[3] 	Lithography and etching: Proximity effects, orientation[4]
Fin geometry/ film thickness variations	Rounding, etc, σ_{VT} , mobility.	Systematic fin thickness Systematic Si film/BOX variations

[1] D. Frank et al, *VLSI Symposium*, Jun. 1999 . [2] A. Asenov et al, *IEEE Trans on Electron Devices,* Jan. 2002.
[3] P. Oldiges et al, *SISPAD 2000,* Sept. 2000. [4] M. Orshansky et al, *IEEE Trans on CAD*, May 2002. [5] Tuinhout et al, *IEDM*, Dec 1996

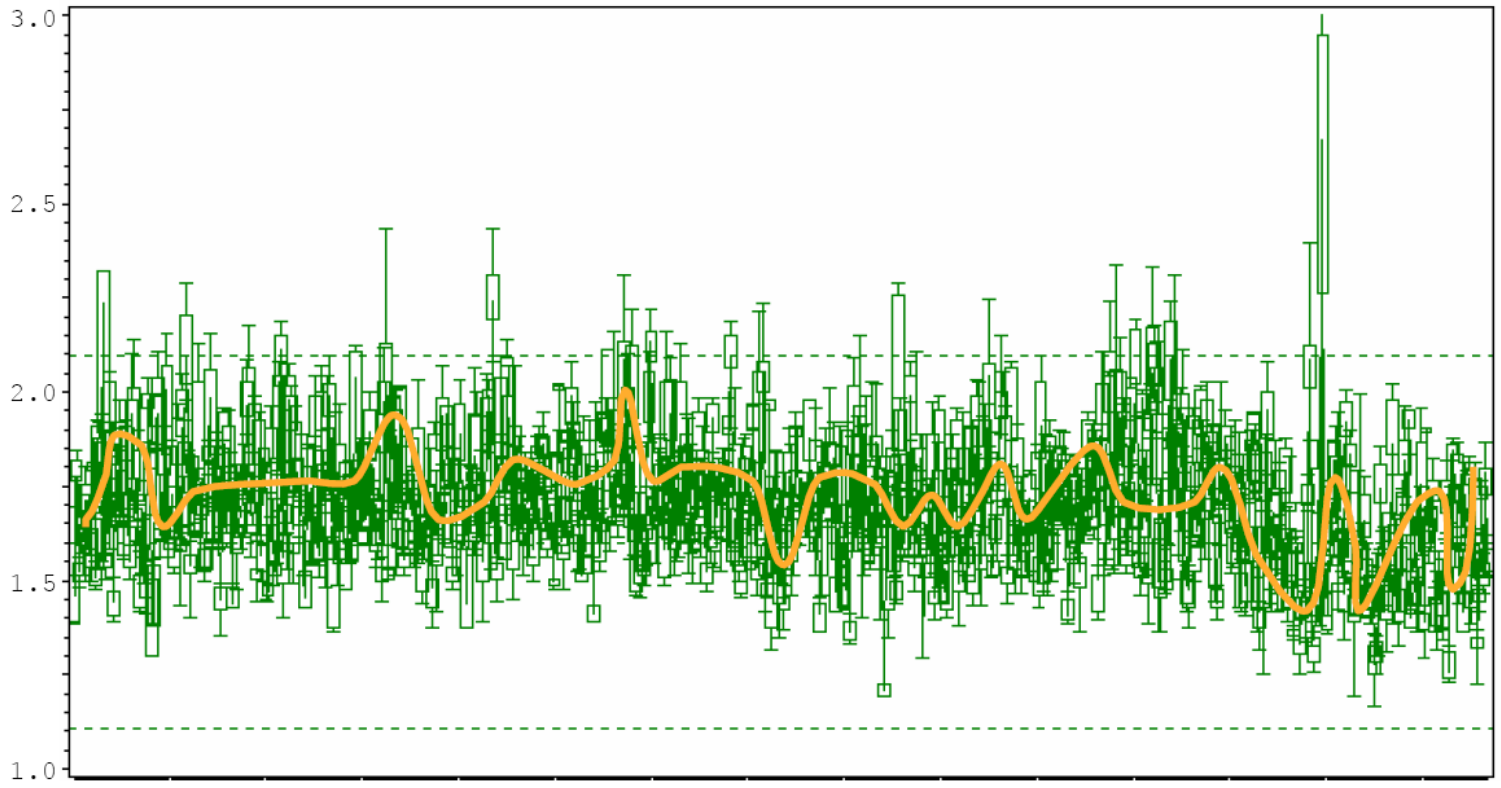
Dealing with Systematic Variations

- Model-to-hardware correlation classifies unknown sources



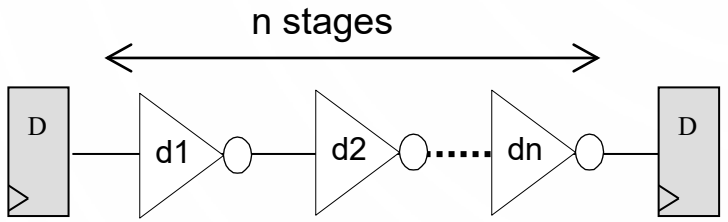
Systematic (?) Temporal Fabrication Variability

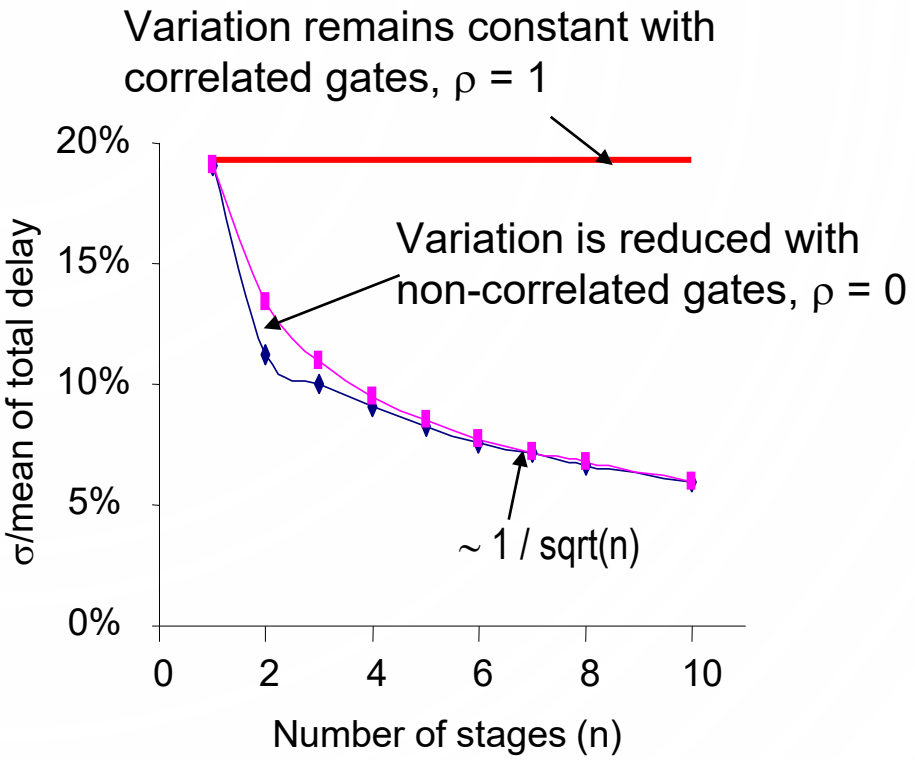
Metal 3 resistance over 3 months



P. Habitz, DAC'06 tutorial

Chip Yield Depends on Inter-Gate Correlation



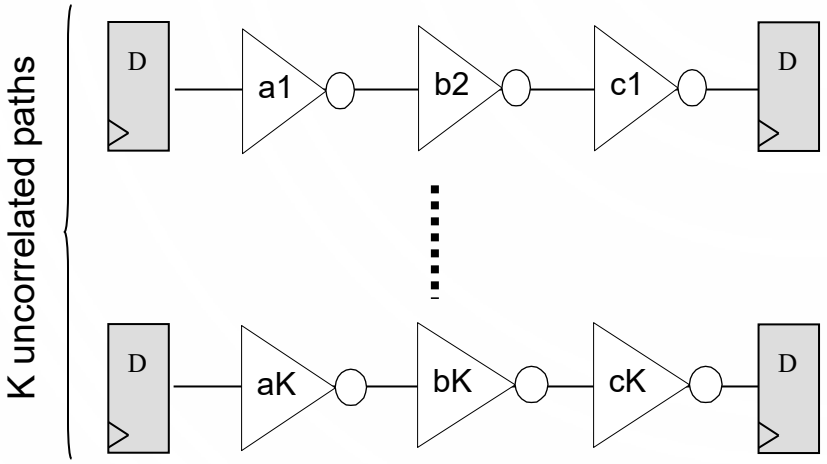


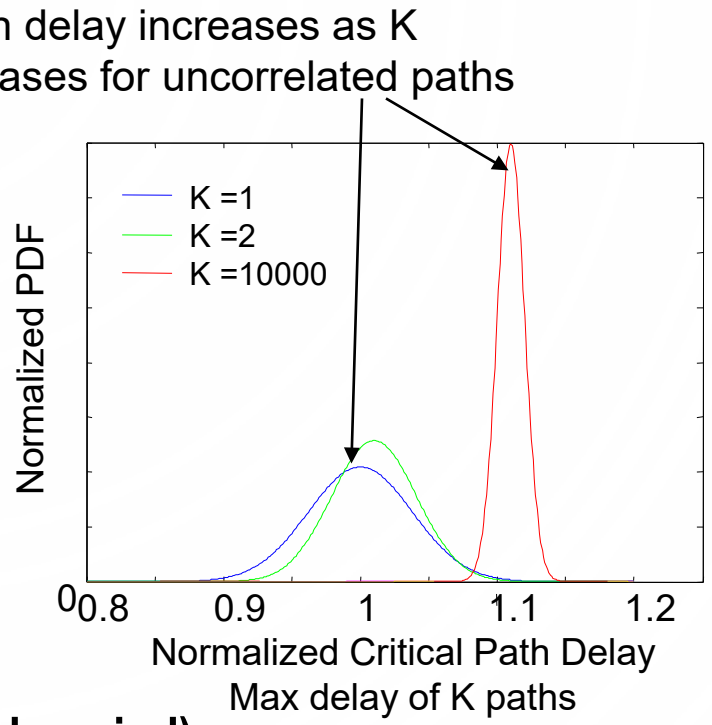
- **Yield = Pr (sum of n delays < clock period)**
- **ρ = 0 gives highest yield through averaging**

Non-correlated gates in a path reduce impact of variation

Bowman et al, *JSSC*, Feb 2002 .

Chip Yield Depends on Inter-Path Correlation





- **Yield = Pr (max delay of K paths < clock period)**
- **K = 1 gives highest yield**

Correlated paths reduce impact of variation

Bowman et al, *JSSC*, Feb 2002 .

Summary

- Logical effort can be used to analyze latch and flip-flop timing
- Flip-flops can be designed as latch pairs or pulsed latches
- There is also asynchronous design
- Variability: Systematic and random

Next Lecture

- Variability
- Memory