Course Evaluations Time!

...Reviewers note that, in some of Nikolić's courses, the return rate for student evaluations is low. They encourage him to consult the website of the Center for Teaching and Learning (https://teaching.berkeley.edu/how-can-instructors-encourage-students-complete-course-evaluations-and-provide-informative-responses) for suggestions on how to increase response rates...

Victoria C. Plaut
Vice Provost for the Faculty
Announcements

• Homework 5 due next week
  • Quiz 4 today

• Project
  • Pay attention to integration with other teams!
  • Final presentations: May 2, 9am-12pm

• Final exam: April 26, in class
Optimal $V_{DD}$, $V_{Th}$
Dynamic Voltage Scaled Microprocessor

External $V_{DD}$ 3.3V±10%
Internal $V_{DDL}$ 0.8V~2.9V ±5%

User Logic PLL

Power Dissipation (mW) vs Operating Frequency (MHz)

Measurement Theory

CMOS: $V_{DD}$=3.3V

VS scheme: Internal $V_{DD}$ optimized

Courtesy: Prof. Kuroda
Adapting $V_{DD}$ and $V_{TH}$ during runtime

- $V_{TH}$ is much less sensitive

-Miyazaki, ISSCC'02
Adapting $V_{DD}$ and $V_{TH}$

Miyazaki, ISSCC'02

![Graph showing the relationship between power (µW) and frequency (MHz) with dynamic voltage scaling and adaptive supply and body bias.](image)
Optimal $V_{DD}, V_{Th}$

• Adjusting $V_{DD}, V_{Th}$ trades of energy and delay

• We studied energy-limited design
  • And alternate ways for optimizing energy and delay together
  • E.g. energy-delay product (EDP)
  • Or $E^n D^m$, $n, m > 1$
Optimal EDP Contours

- Plot of EDP curves in $V_{\text{DD}}, V_{\text{Th}}$ plane

Gonzalez, JSSC 8/97
Reference Design: 

\[ D_{\text{ref}} (V_{dd}^{\text{max}}, V_{th}^{\text{ref}}) \]

<table>
<thead>
<tr>
<th>Topology</th>
<th>Inverter</th>
<th>Adder</th>
<th>Decoder</th>
</tr>
</thead>
<tbody>
<tr>
<td>( (E_{Lk}/E_{SW})^{\text{ref}} )</td>
<td>0.1%</td>
<td>1%</td>
<td>10%</td>
</tr>
</tbody>
</table>

Large variation in optimal circuit parameters \( V_{dd}^{\text{opt}}, V_{th}^{\text{opt}}, w^{\text{opt}} \)

Technology parameters \( (V_{dd}^{\text{max}}, V_{th}^{\text{ref}}) \) rarely optimal
Result: E-D Tradeoff in an Adder

Energy efficient curve $f(W, Vdd, Vth)$

**Table: Sensitivity**

<table>
<thead>
<tr>
<th>Sensitivity</th>
<th>W</th>
<th>Vdd</th>
<th>Vth</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{ref}, E_{ref}$</td>
<td>$\infty$</td>
<td>1.5</td>
<td>0.2</td>
</tr>
<tr>
<td>$D_{ref}, E_{min}$</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$D_{min}, E_{ref}$</td>
<td>22</td>
<td>16</td>
<td>22</td>
</tr>
</tbody>
</table>

- 80% of energy saved without delay penalty
- 40% delay improvement without energy penalty
Energy-constrained delay

• Active power

\[ P_{act} = \alpha f CV_{DD}^2 \]

\[ f = 1/L_D t_p \]

• Leakage power

\[ P_{leak} = I_0 e^{-\frac{V_{Th} - \gamma V_{DD}}{S V_{DD}}} \]

• Eliminate one variable \( V_{Th} \) and find \( P_{min}(V_{DD}) \)

Nose, ASP-DAC’00
Minimum energy: \( E_{Sw} = 2E_{Lk} \)

- Large \( (E_{Lk}/E_{Sw})_{opt} \)
- Flat \( E_{Op} \) minimum
- Topology dependent

Optimal designs have high leakage \( (E_{Lk}/E_{Sw} \approx 0.5) \)

\[
(E_{Lk}/E_{Sw})_{opt} = \frac{2}{\ln \left( \frac{L_d}{\alpha_{avg}} \right) - K}
\]
Phase Locked Loops
Phase-Locked Loop

- PLL is locked when the phase difference is zero
- Second/third order loop
- ÷N for frequency synthesis (and x M)
- Filters input jitter
- Accumulates phase error
Voltage-Controlled Oscillator

- Oscillation frequency controlled by voltage

\[ \omega_{out} = \omega_{FR} + K_{VCO} V_{ctrl} \]

\[ y_{out}(t) = A \cos \left( \omega_{FR} t + K_{VCO} \int_{-\infty}^{t} V_{ctrl} dt \right) \]

\( \omega_{FR} \) – free-running frequency
Example VCO

- Ring-oscillator-based VCO: RC loaded

![Ring-oscillator-based VCO: RC loaded](image)

- Ring-oscillator-based VCO: Current-starved

![Ring-oscillator-based VCO: Current-starved](image)
Example VCO

- Ring-oscillator-based VCO: Supply-regulated

![Diagram of a VCO with PFD, dividers, and a ring oscillator](image-url)
PLL vs. DLL Dynamics

- The key difference is in the VCDL vs. VCO transfer characteristics
- VCO integrates (accumulates) phase

\[ H_{VCO}(s) = \frac{K_{VCO}}{s} \]
Linear Phase-Frequency Detector

(a) Linear phase-frequency detector circuit diagram.

(b) Waveforms showing the input and output signals.

(c) Voltage output waveform corresponding to phase difference.

Razavi'2001
Charge Pump

- Push/pull current source operation

\[ V_{DD} \]
\[ \text{UP} \quad \text{To VCO Control Input} \]
\[ \text{DN} \]

\[ T_{in} \]
\[ A \]
\[ B \]
\[ Q_A \]
\[ V_{out} \]

\[ \frac{1}{2\pi C_P} \quad \frac{I_P}{\phi_0} \]

Razavi'2001
Charge-Pump PLL

\[ H(s) = \frac{\Phi_{out}}{\Phi_{in}} = \frac{\frac{K_{PFD}}{s} \cdot \frac{K_{VCO}}{s}}{1 + \frac{K_{PFD}}{s} \cdot \frac{K_{VCO}}{s}} = \frac{K_{PFD}K_{VCO}}{s^2 + K_{PFD}K_{VCO}} \]

Phase transfer function
Charge Pump PLL with a Zero

- Charge pump PLL has a stability problem
- Compensation by adding a zero

\[ \begin{align*}
C_p & \\
\downarrow & \\
\end{align*} \quad \rightarrow \quad \begin{align*}
C_p & \\
R & \\
\downarrow & \\
\end{align*} \]
Charge Pump PLL with a Zero

\[ \omega_n = \sqrt{\frac{I}{2\pi C_P}} K_{VCO} \]

\[ \zeta = \frac{R}{2} \sqrt{\frac{I C_P}{2\pi}} K_{VCO} \]

\[ H(s) = \frac{K_{VCO} \cdot I}{2\pi C_P} \cdot (R C_P s + 1) \]

\[ s^2 + \frac{I}{2\pi} K_{VCO} R_S + \frac{I}{2\pi C_P} K_{VCO} \]
Higher Order Loops

- Another pole naturally exists
  - Filters the control voltage $V_{CTRL}$
  - Lowers phase margin
  - Reduces the lock range
Phase Noise at the PLL Input

- Low-pass characteristic

\[ H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]

\[ |\log(\Phi_{\text{out}}/\Phi_{\text{in}})| \]
VCO Phase Noise – Noise Transfer Function

- High-pass characteristic noise transfer function

\[ \Phi_{\text{in}} = 0 \quad \Phi_{\text{out}} \quad \Phi_{\text{VCO}} \]

\[ \Phi_{\text{out}}(s) = \frac{s(s + \omega_{\text{LPF}})}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]

\[ |\log(\Phi_{\text{out}}/\Phi_{\text{VCO}})| \]
Adding clock buffers – all noise transfer functions

• Noise Transfer Functions (NTFs)
  • Low-pass from refclk
  • Band-pass from VCO supply
  • High-pass from clock buffer supply
Resulting Output Phase noise spectrum

- Set by reference clock $f < \text{loop bandwidth}$
- Set by supply noise $f > \text{loop bandwidth}$
Digital PLLs
Digital PLL

- Replace analog functions with digital equivalents

Digitally-controlled oscillator (DCO)
Digital vs Analog PLL
Digital PLL Quantization noise

- Limit cycle phase noise adds to the linearized model phase noise

\[ \phi_{out,lc,p-p} = T_{ref} \cdot K_{DCO} \cdot (2P_{BB} + I_{BB}) \]

\[ \phi_{out,lc,rms} = \frac{T_{ref} \cdot K_{DCO}}{\sqrt{3}} \cdot \sqrt{P_{BB}^2 + P_{BB} \cdot I_{BB} + \frac{I_{BB}^2}{2}} \]
Digital PLL Analysis

- Loop parameters can be matched to the analog PLL

\[
P_{\text{BB}} = \frac{P \cdot K_{\text{VCO}}}{\text{Gain}_{\text{BB}} \cdot K_{\text{DCO}}}
\]

\[
I_{\text{BB}} = \frac{I \cdot T_{\text{ref}} \cdot K_{\text{VCO}}}{\text{Gain}_{\text{BB}} \cdot K_{\text{DCO}}}
\]

\[
\text{Gain}_{\text{BB}} = \frac{2}{\pi} \cdot \frac{D}{\sigma_{\phi_{\text{err}}}}
\]

Linear VCO noise to output phase:

\[
\phi_{\text{out, rms}} = \frac{1}{\sqrt{2}} \cdot \frac{1}{4 \cdot P_{\text{BB}} \cdot K_{\text{DCO}}} \cdot \frac{\left(\sigma_{V_n} \cdot K_{\text{VCO,n}}\right)^2}{\Delta f}
\]

VCO thermal and supply noise (assume it dominates)

Linear PLL Simulation
BBPLL Simulation
BBPLL Analysis

VCO noise reduction
Excess BBPD noise
Linear model unstable
Digital BBPD-PLL

- PFD to DCO direct proportional path for faster phase tracking
Practical Digital PLL

• In IBM Power7 processor, per each core

Tierno, VLSI’10

Tierno, JSSC’08
Next Lecture

• Clock distribution
• Power-supply regulation