EECS251B : Advanced Digital Circuits and Systems

Lecture 25 – Clocks

Borivoje Nikolić

Course Evaluations Time!

…Reviewers note that, in some of Nikolić's courses, the return rate for student evaluations is low. They encourage him to consult the website of the Center for Teaching and Learning (https://teaching.berkeley.edu/how-can-instructors-encourage-students-complete-course-evaluations-and-provide-informative-responses) for suggestions on how to increase response rates…

Victoria C. Plaut
Vice Provost for the Faculty

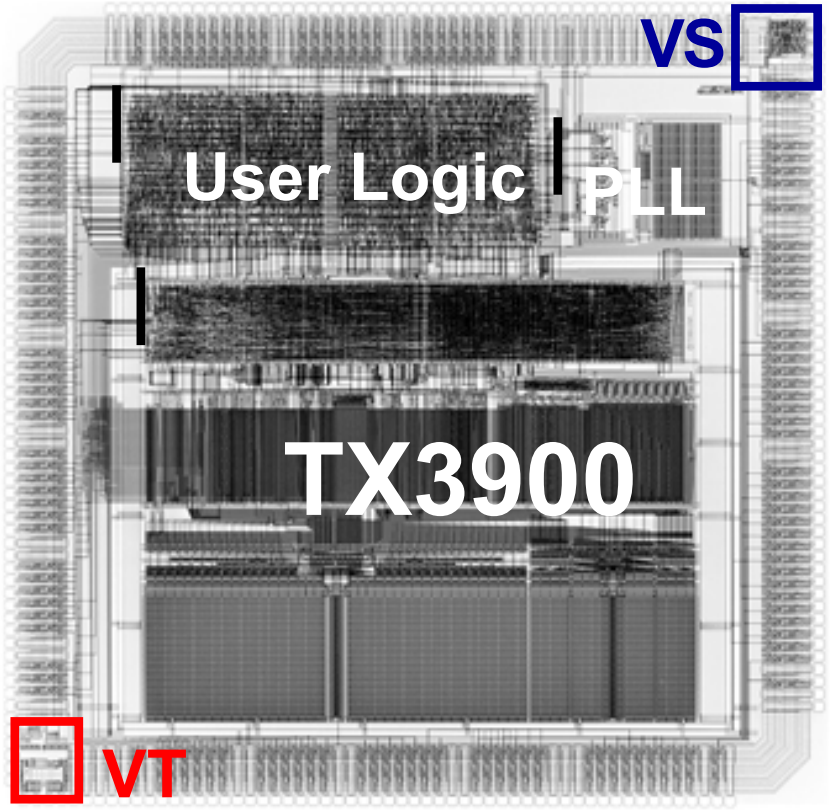
Announcements

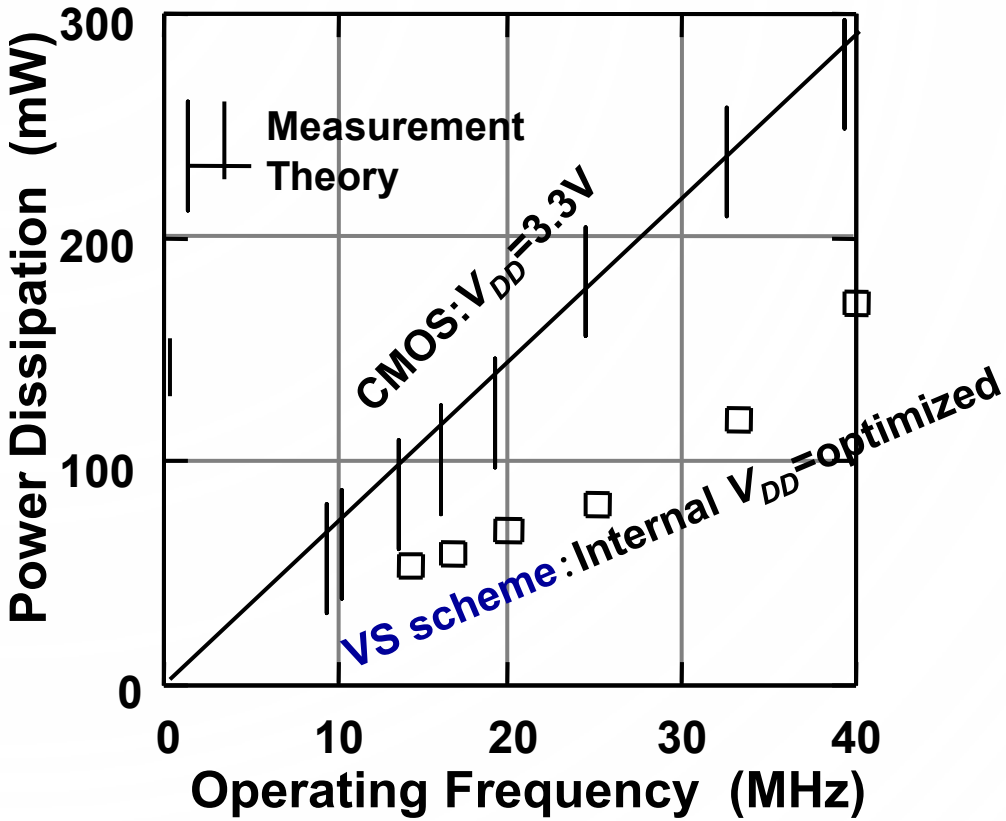
- Homework 5 due next week
  - Quiz 4 today
- Project
  - Pay attention to integration with other teams!
  - Final presentations: May 2, 9am-12pm
- Final exam: April 26, in class

Optimal V_{DD}, V_{Th}

Dynamic Voltage Scaled Microprocessor

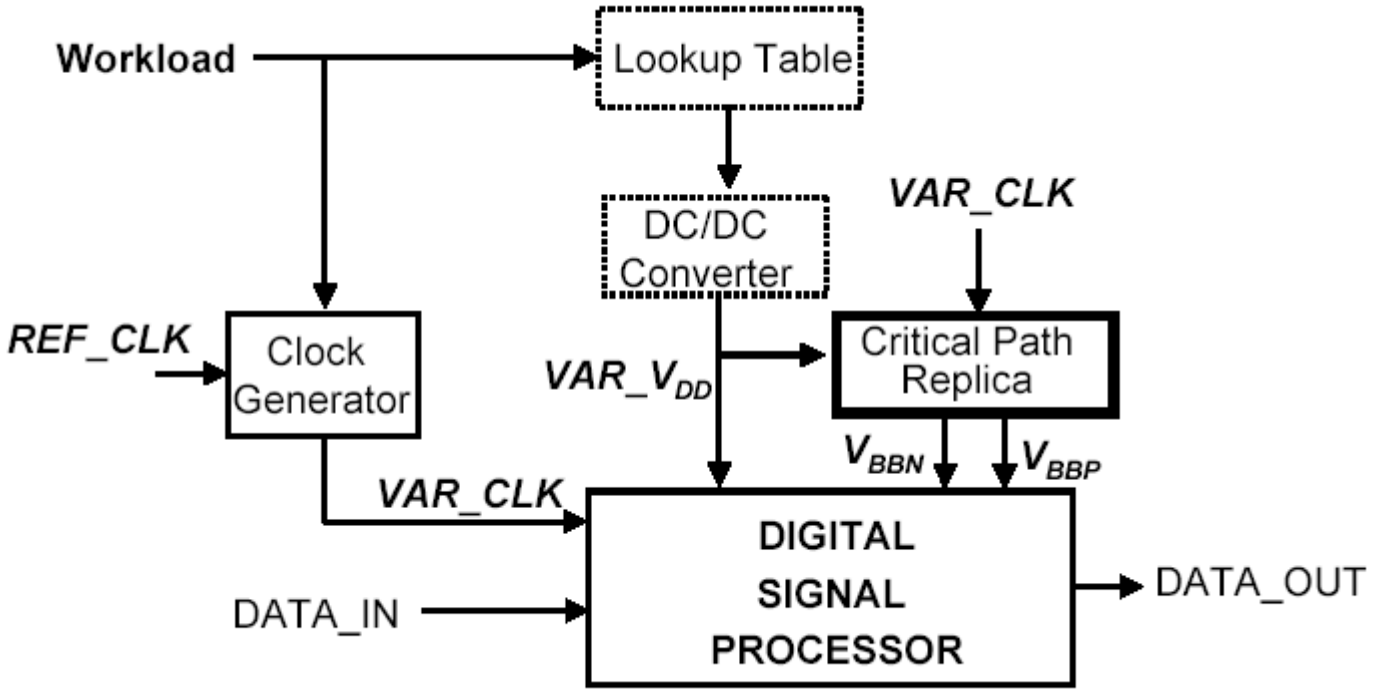
External V_{DD} 3.3V±10%
Internal V_{DDL} 0.8V~2.9V ±5%





Courtesy: Prof. Kuroda

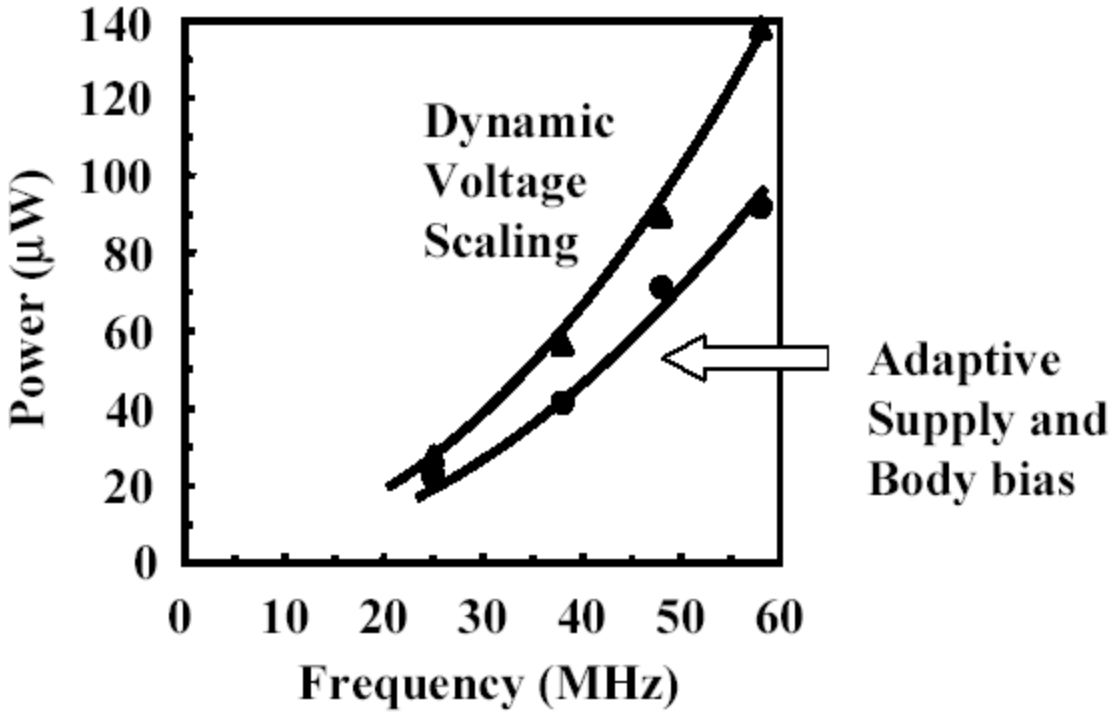
Adapting V_{DD} and V_{TH}



- Adapting both V_{DD} and V_{Th} during runtime
  - V_{Th} is much less sensitive

Miyazaki, ISSCC'02

Adapting V_{DD} and V_{TH}



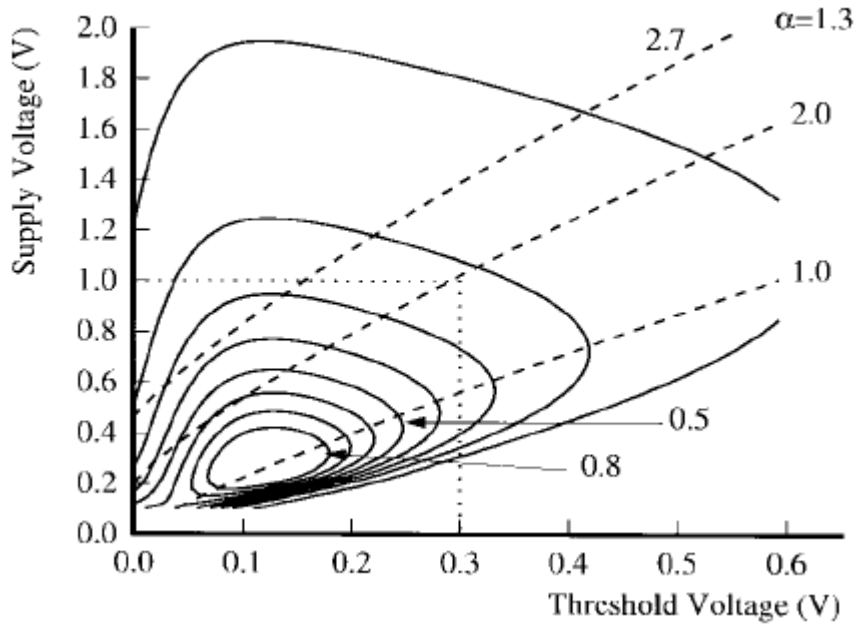
Miyazaki, ISSCC'02

Optimal V_{DD}, V_{Th}

- Adjusting V_{DD}, V_{Th} trades of energy and delay
- We studied energy-limited design
  - And alternate ways for optimizing energy and delay together
  - E.g. energy-delay product (EDP)
  - Or E^nD^m, $n,m > 1$

Optimal EDP Contours

- Plot of EDP curves in V_{DD}, V_{Th} plane



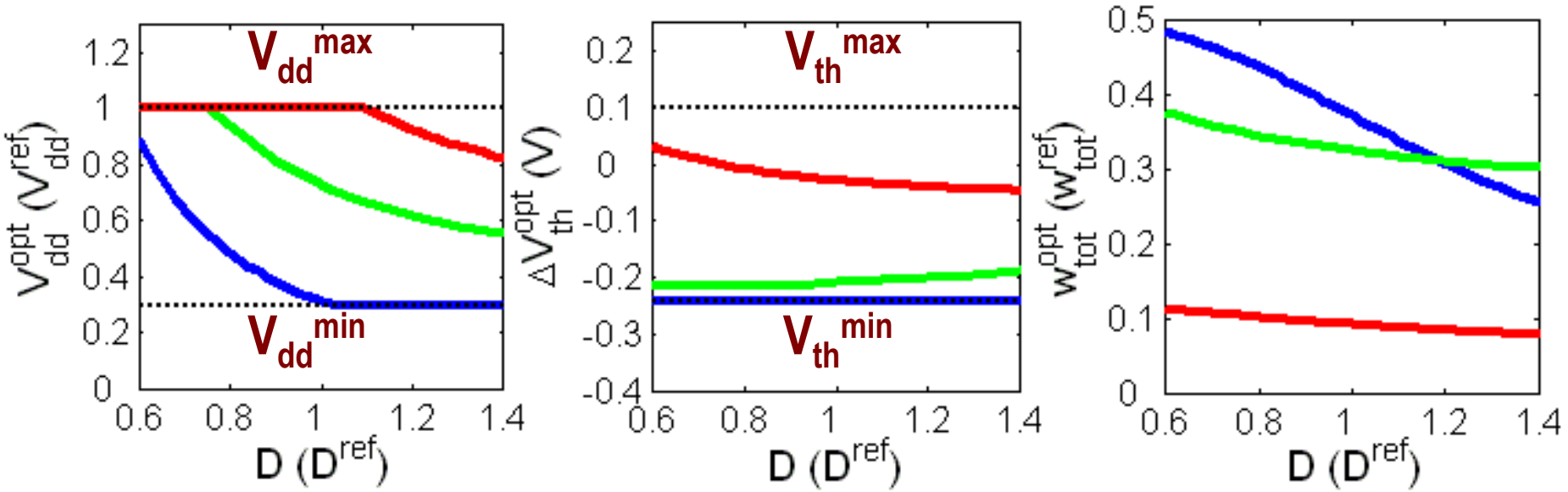
Gonzalez, JSSC 8/97

Sizing, Supply, Threshold Optimization

Reference Design:
D^{ref} (V_{dd}^{max},V_{th}^{ref})

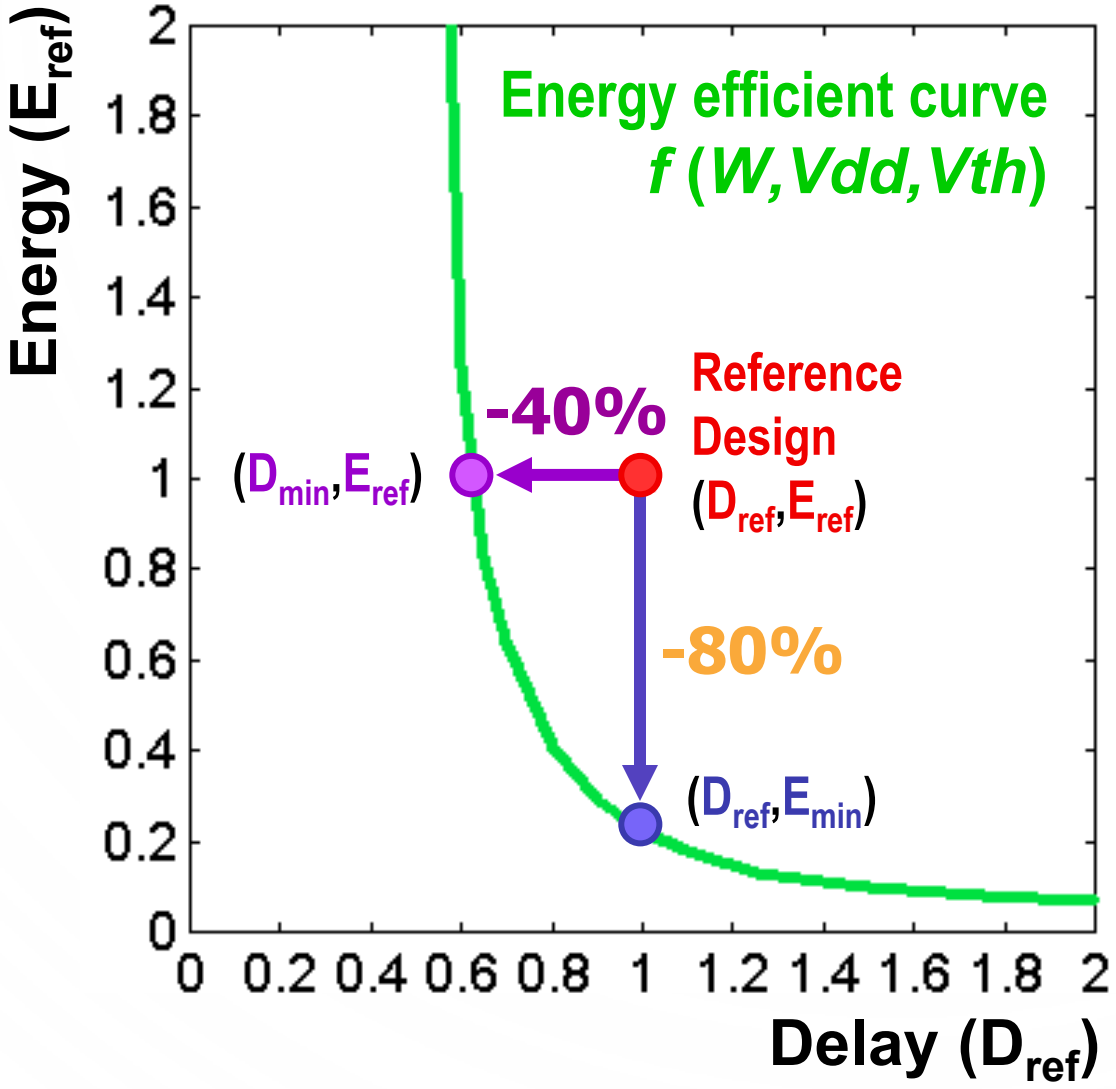
Topology	Inverter	Adder	Decoder
$(E_{Lk}/E_{Sw})^{ref}$	0.1%	1%	10%

Large variation in optimal circuit parameters V_{dd}^{opt}, V_{th}^{opt}, w^{opt}



Technology parameters (V_{dd}^{max}, V_{th}^{ref}) rarely optimal

Result: E-D Tradeoff in an Adder



Sensitivity	W	Vdd	Vth
(D_{ref},E_{ref})	∞	1.5	0.2
(D_{ref},E_{min})	1		
(D_{min},E_{ref})	22	16	22

80% of energy saved without delay penalty

40% delay improvement without energy penalty

Energy-constrained delay

- Active power

$$P_{act} = \alpha f C V_{DD}^{\ 2}$$

$$f = 1/L_D t_p$$

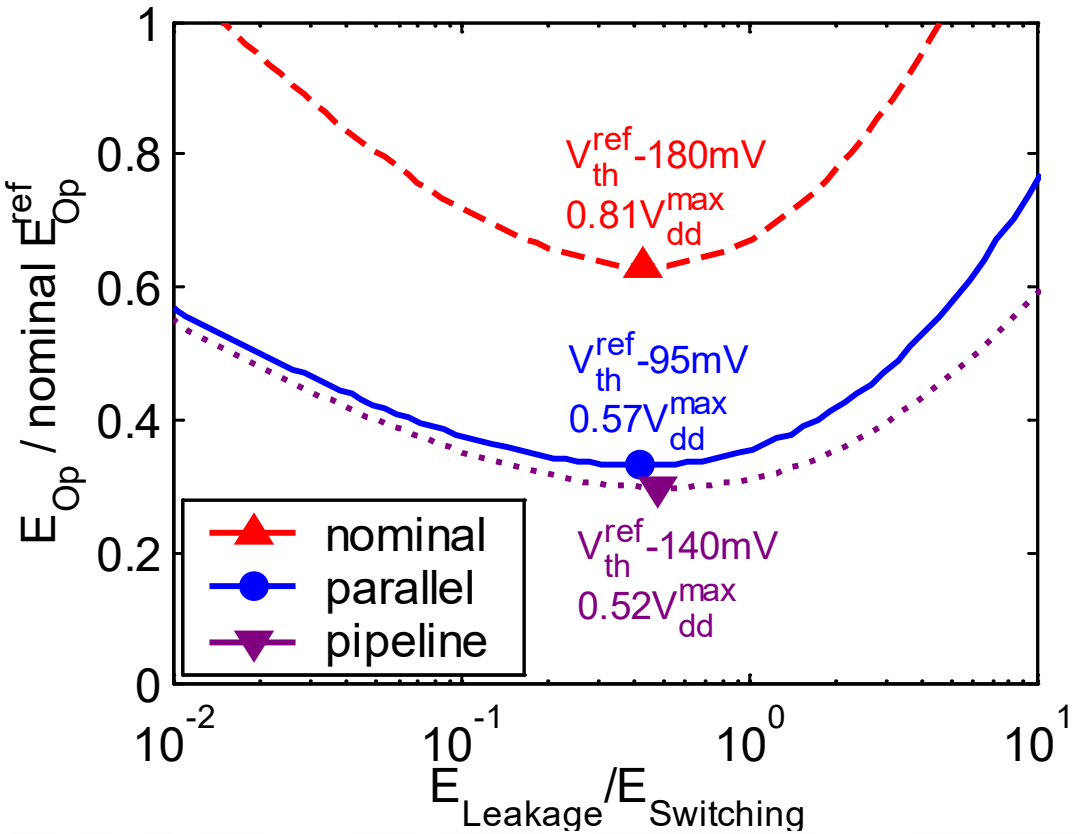
- Leakage power

$$P_{leak} = I_0 e^{\frac{-V_{Th} - \gamma V_{DD}}{S}} V_{DD}$$

- Eliminate one variable(V_{Th}) and find P_{min}(V_{DD})

Nose, ASP-DAC'00

Minimum energy: $E_{Sw} = 2_{ELk}$



- Large $(E_{Lk}/E_{Sw})^{opt}$
- Flat E_{Op} minimum
- Topology dependent

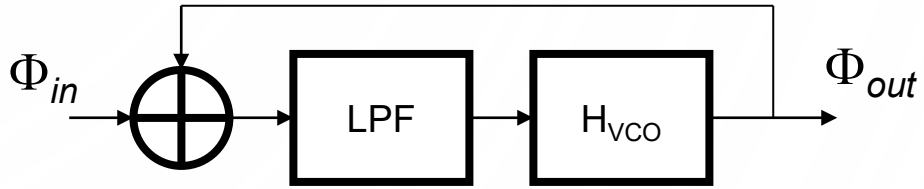
$$\left(E_{Lk}/E_{Sw}\right)_{opt} = \frac{2}{\ln\left(\frac{L_d}{\alpha_{avg}}\right) - K}$$

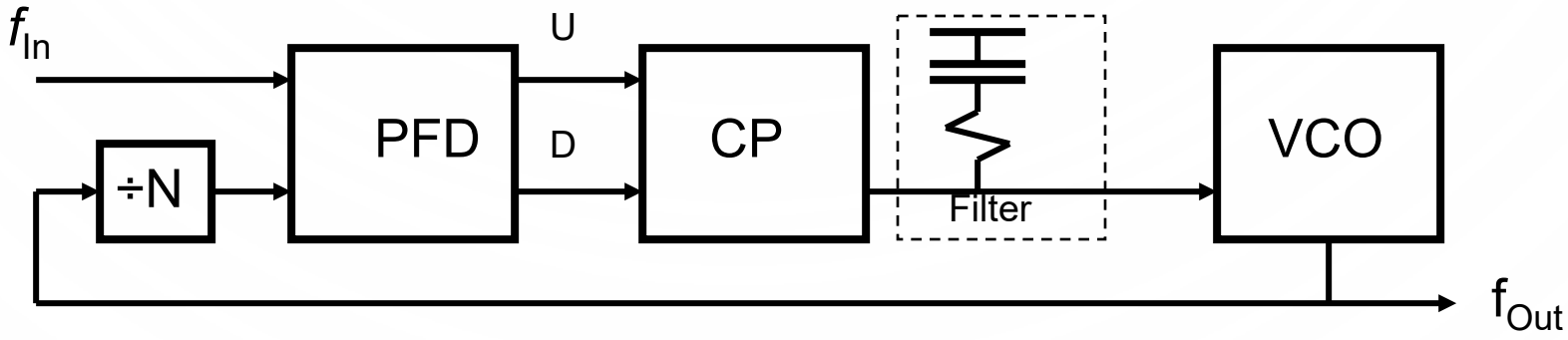
Optimal designs have high leakage ($E_{Lk}/E_{Sw} \approx 0.5$)

Phase Locked Loops

Phase-Locked Loop

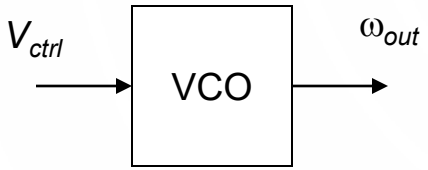
- PLL is locked when the phase difference is zero
- Second/third order loop
- ÷N for frequency synthesis (and x M)
- Filters input jitter
- Accumulates phase error





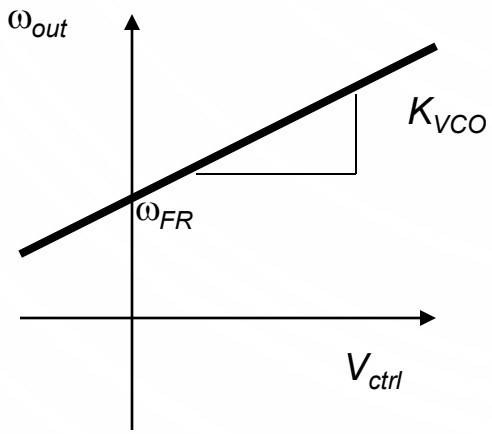
Voltage-Controlled Oscillator

- Oscillation frequency controlled by voltage



$$\omega_{out} = \omega_{FR} + K_{VCO} V_{ctrl}$$

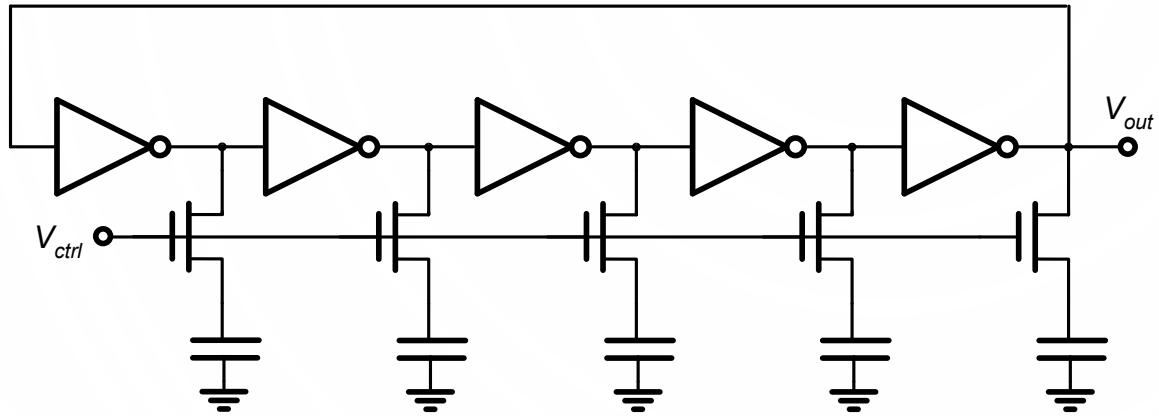
$$y_{out}(t) = A\cos\left(\omega_{FR} t + K_{VCO}\int_{-\infty}^{t} V_{ctrl}\, dt\right)$$



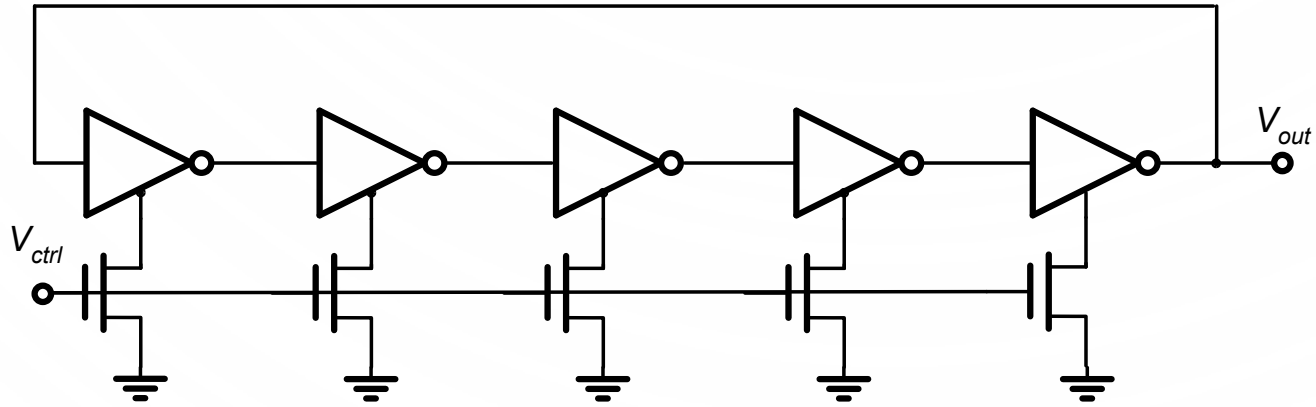
ω_{FR} – free-running frequency

Example VCO

- Ring-oscillator-based VCO: RC loaded

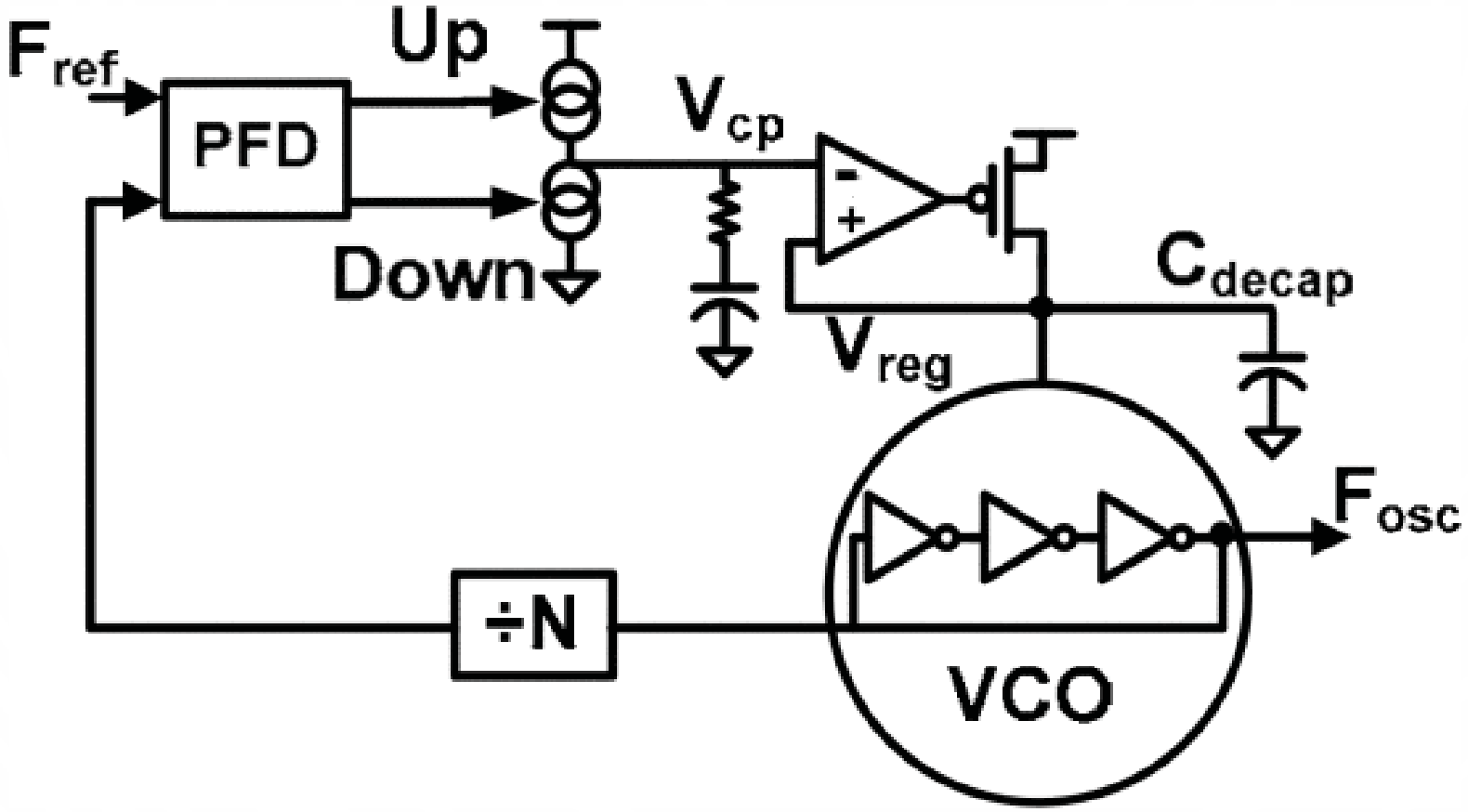


- Ring-oscillator-based VCO: Current-starved



Example VCO

- Ring-oscillator-based VCO: Supply-regulated



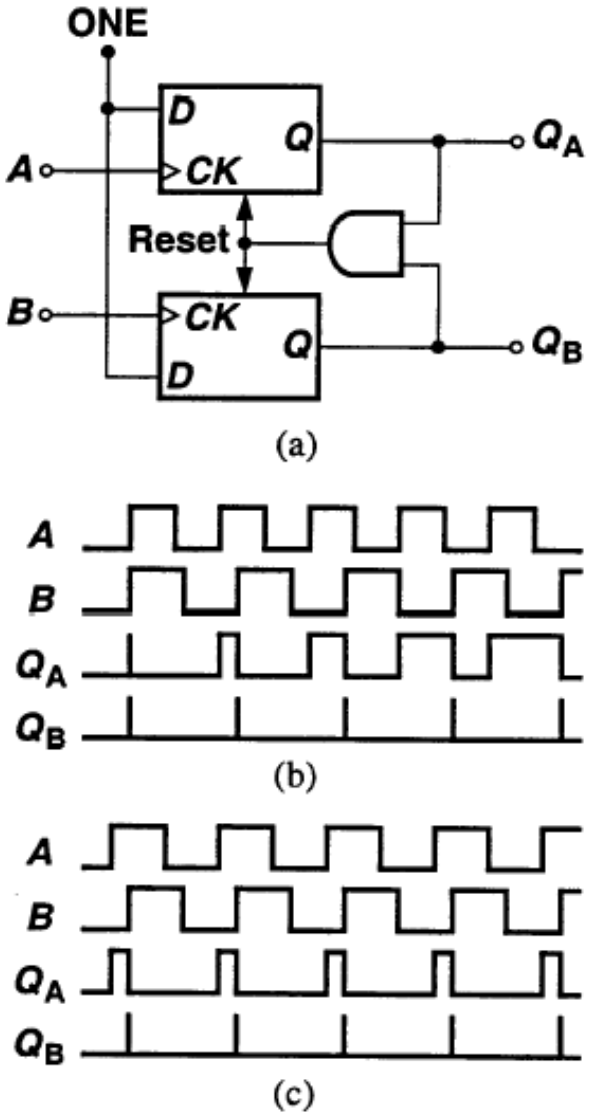
Sidiropoulos VLSI00

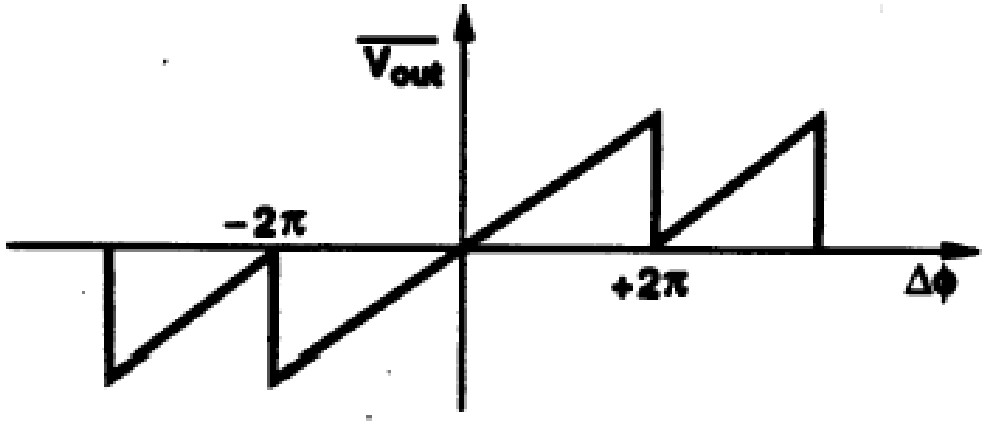
PLL vs. DLL Dynamics

- The key difference is in the VCDL vs. VCO transfer characteristics
- VCO integrates (accumulates) phase

$$H_{VCO}(s) = K_{VCO}/s$$

Linear Phase-Frequency Detector

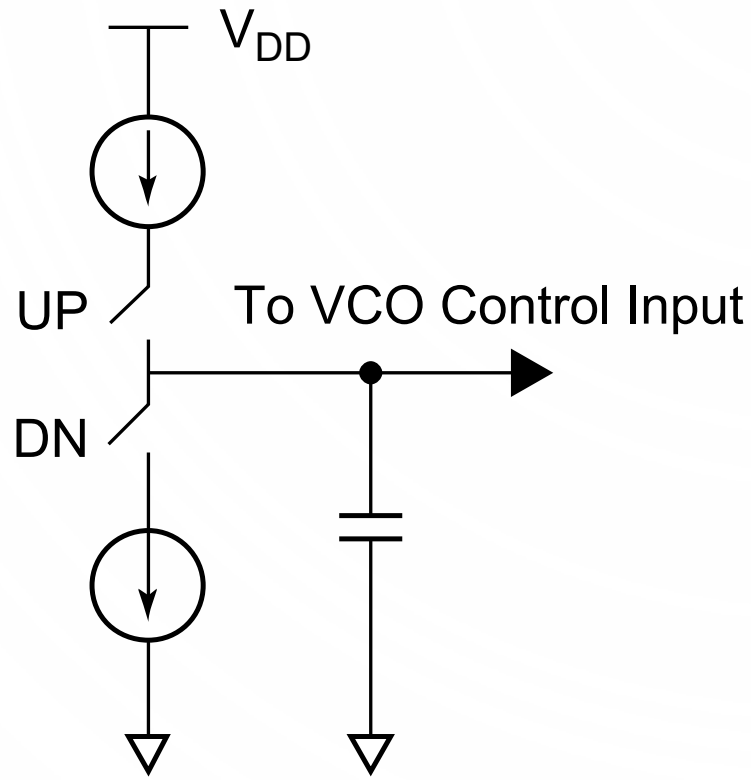


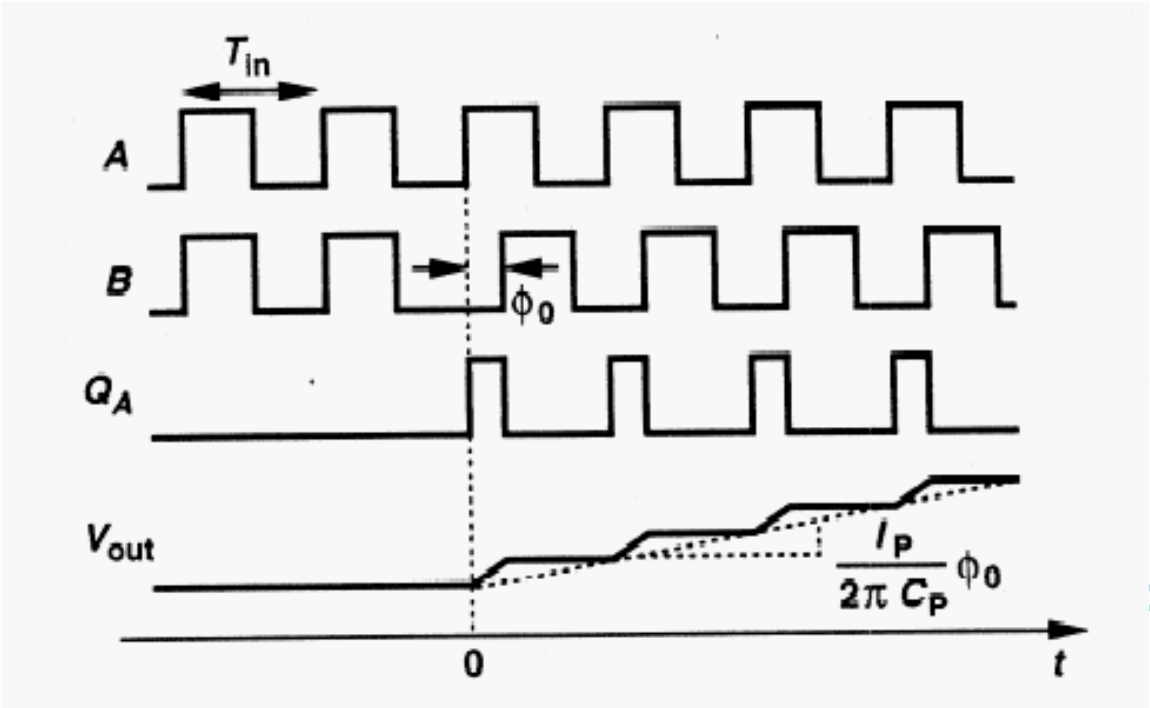


- Razavi'2001

Charge Pump

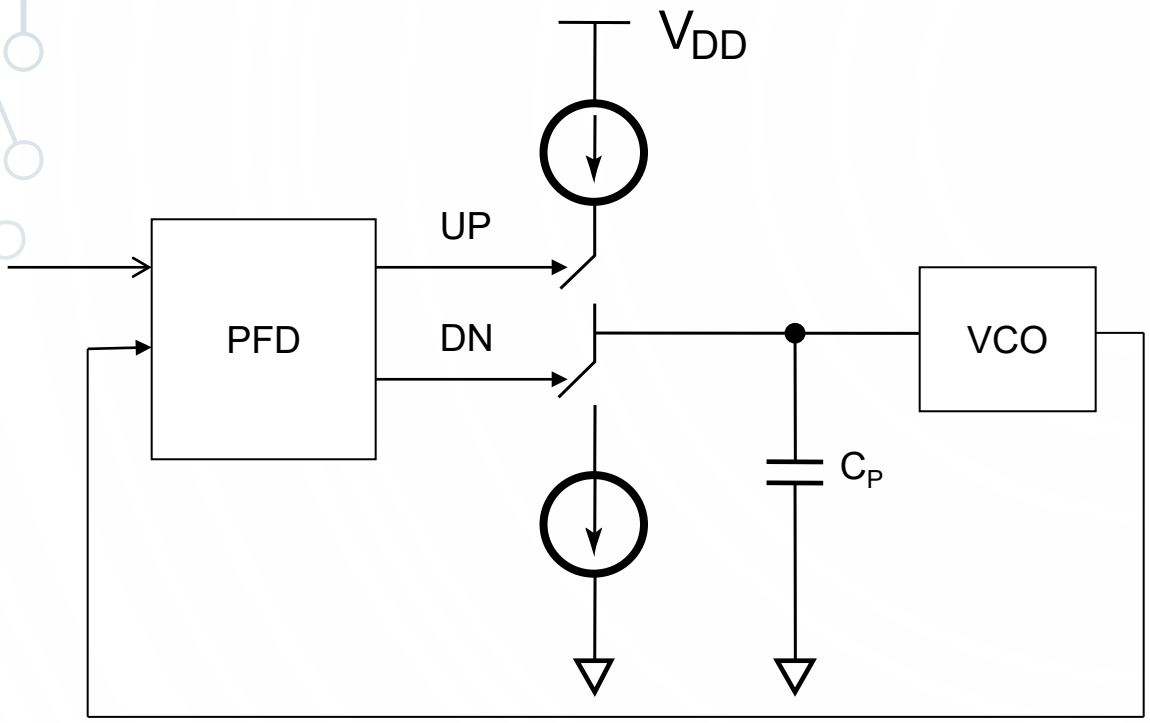
- Push/pull current source operation

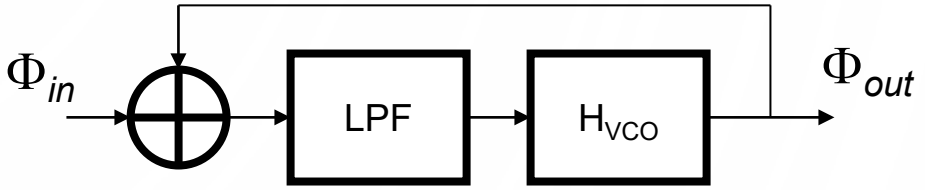




Razavi'2001

Charge-Pump PLL



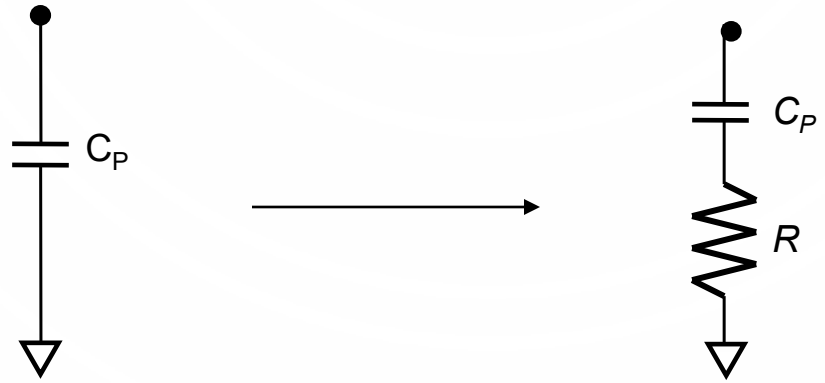


- Phase transfer function

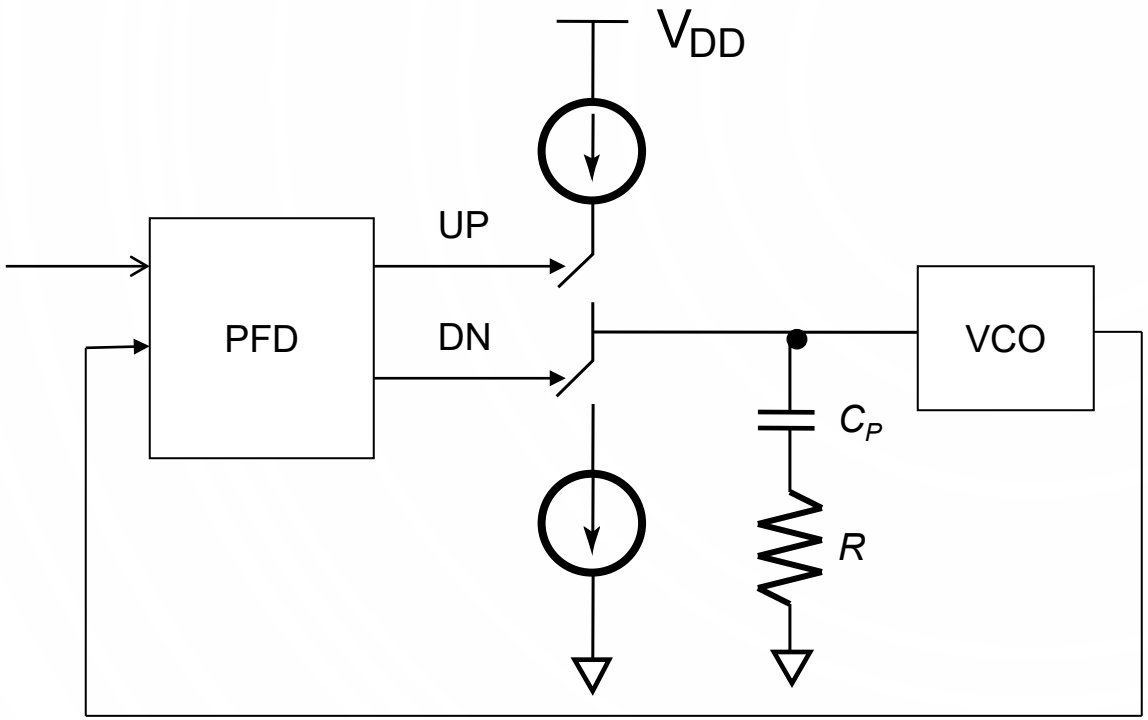
$$H(s) = \frac{\Phi_{out}}{\Phi_{in}} = \frac{\frac{K_{PFD}}{s} \cdot \frac{K_{VCO}}{s}}{1 + \frac{K_{PFD}}{s} \cdot \frac{K_{VCO}}{s}} = \frac{K_{PFD}K_{VCO}}{s^2 + K_{PFD}K_{VCO}}$$

Charge Pump PLL with a Zero

- Charge pump PLL has a stability problem
- Compensation by adding a zero



Charge Pump PLL with a Zero



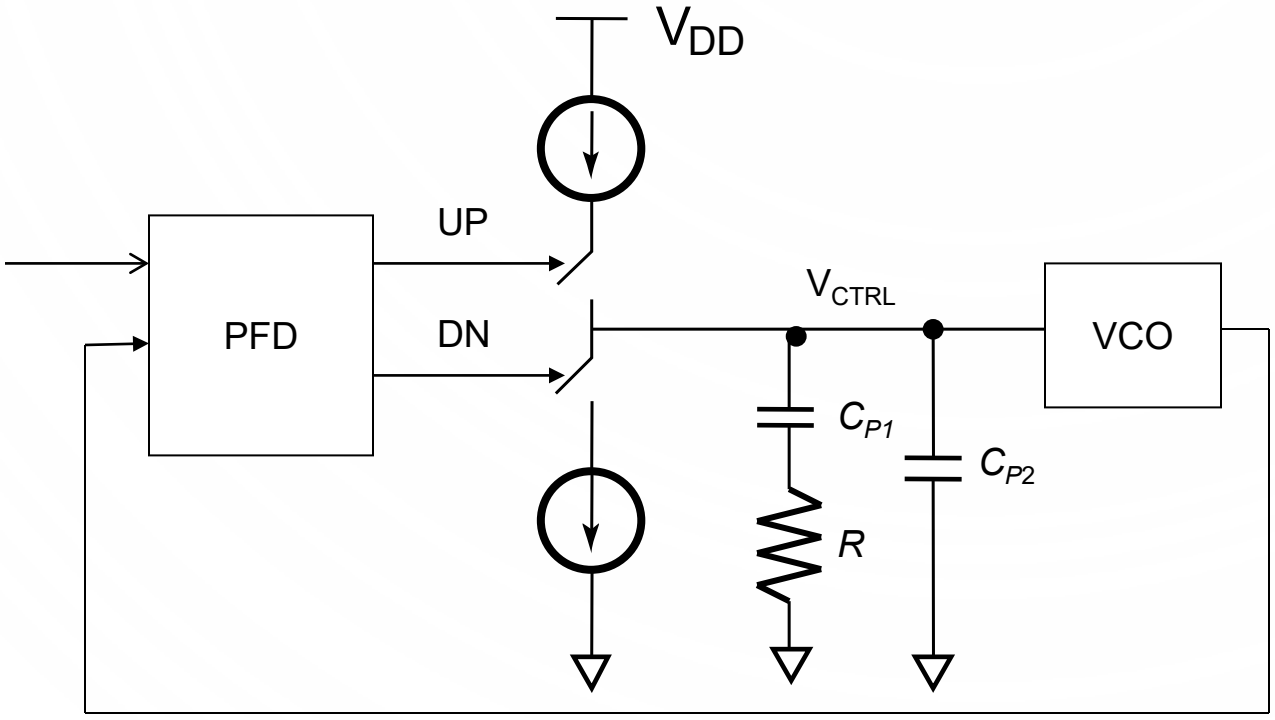
$$\omega_n = \sqrt{\frac{I}{2\pi C_P} K_{VCO}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{IC_P}{2\pi} K_{VCO}}$$

$$H(s) = \frac{\frac{K_{VCO} \cdot I}{2\pi C_P} \cdot (RC_P s + 1)}{s^2 + \frac{I}{2\pi} K_{VCO} R_S + \frac{I}{2\pi C_P} K_{VCO}}$$

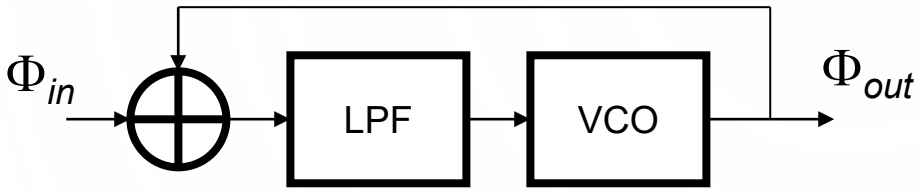
Higher Order Loops

- Another pole naturally exists
  - Filters the control voltage V_{CTRL}
  - Lowers phase margin
  - Reduces the lock range

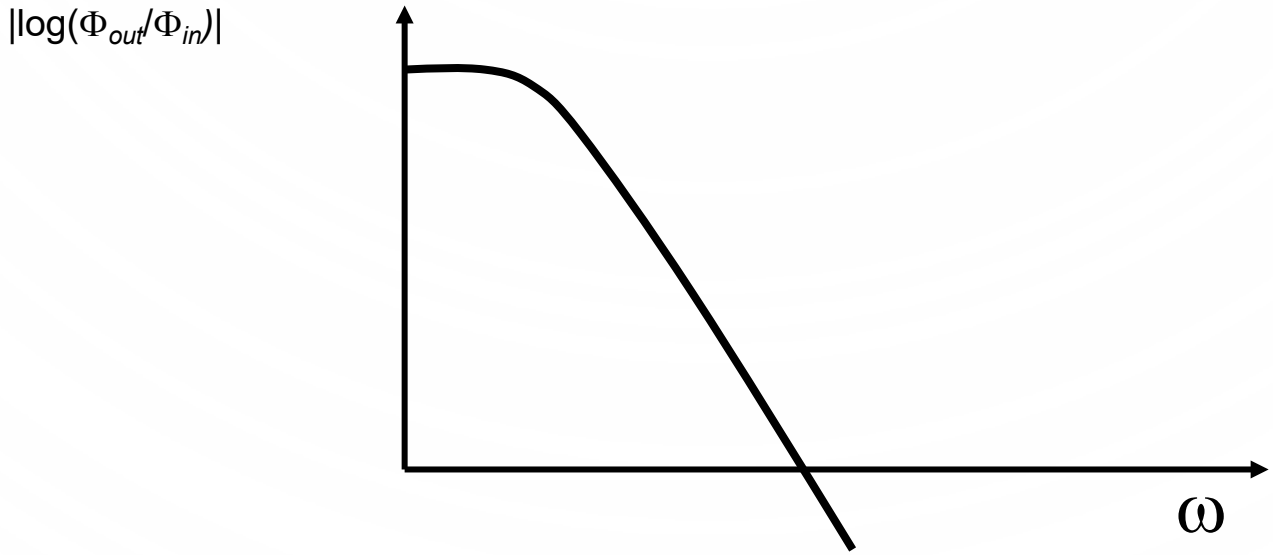


Phase Noise at the PLL Input

- Low-pass characteristic

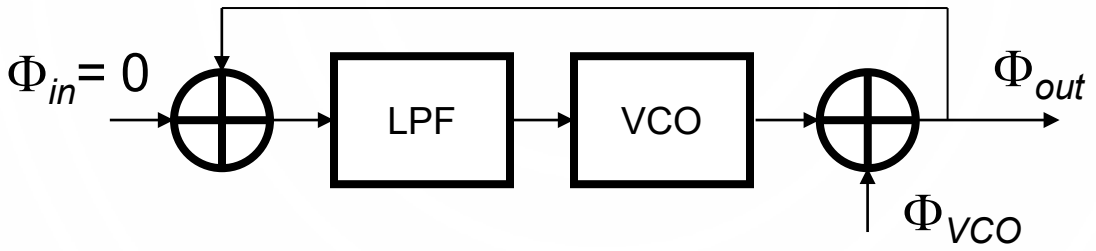


$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

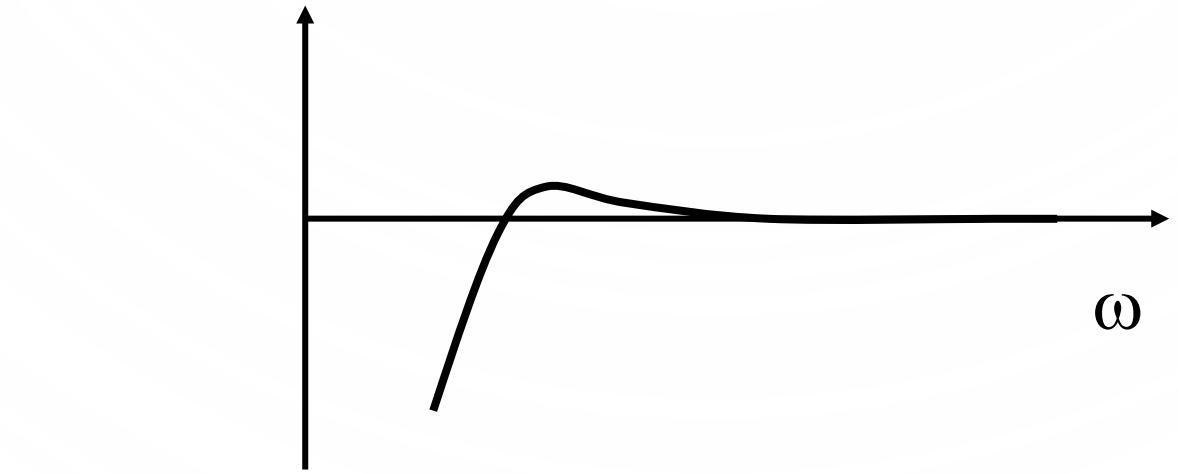


VCO Phase Noise – Noise Transfer Function

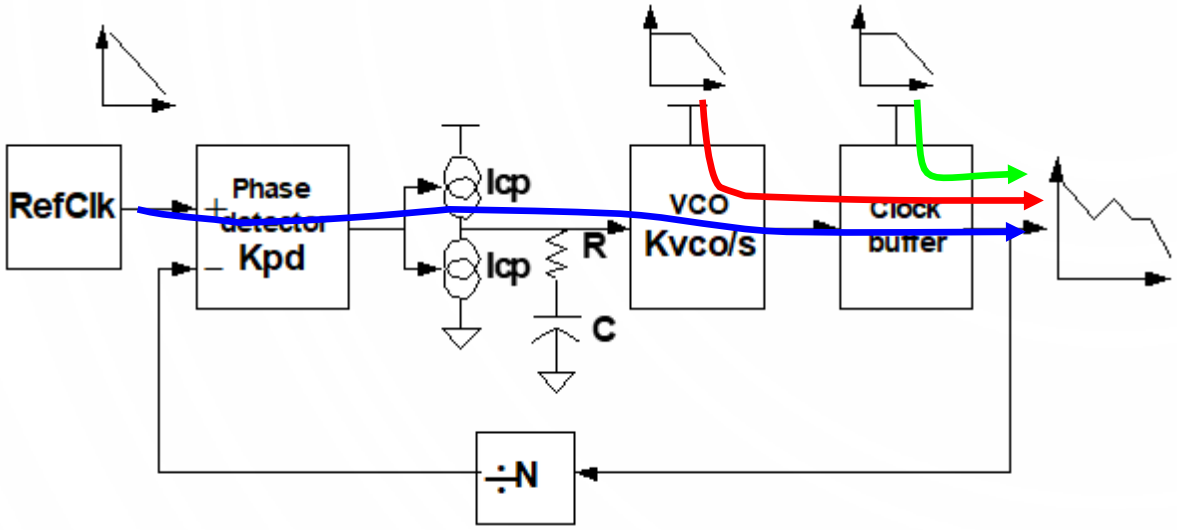
- High-pass characteristic noise transfer function

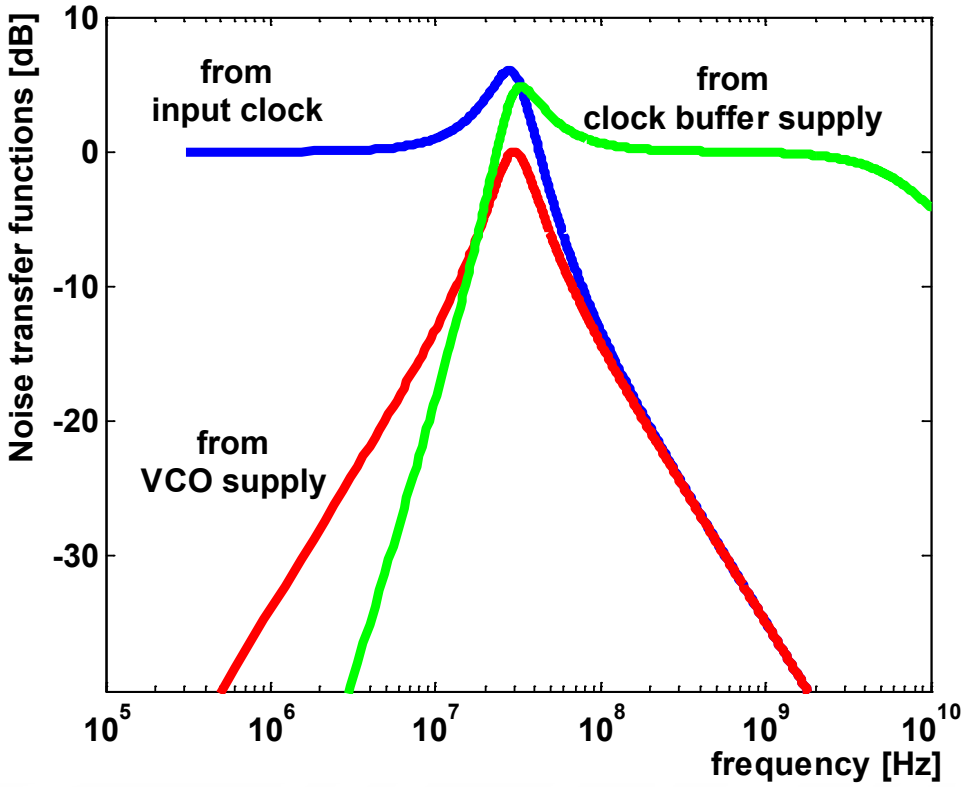


$$\frac{\Phi_{out}(s)}{\Phi_{VCO}(s)} = \frac{s(s+\omega_{LPF})}{s^2 + 2\zeta\omega_n s + \omega_n{}^2}$$



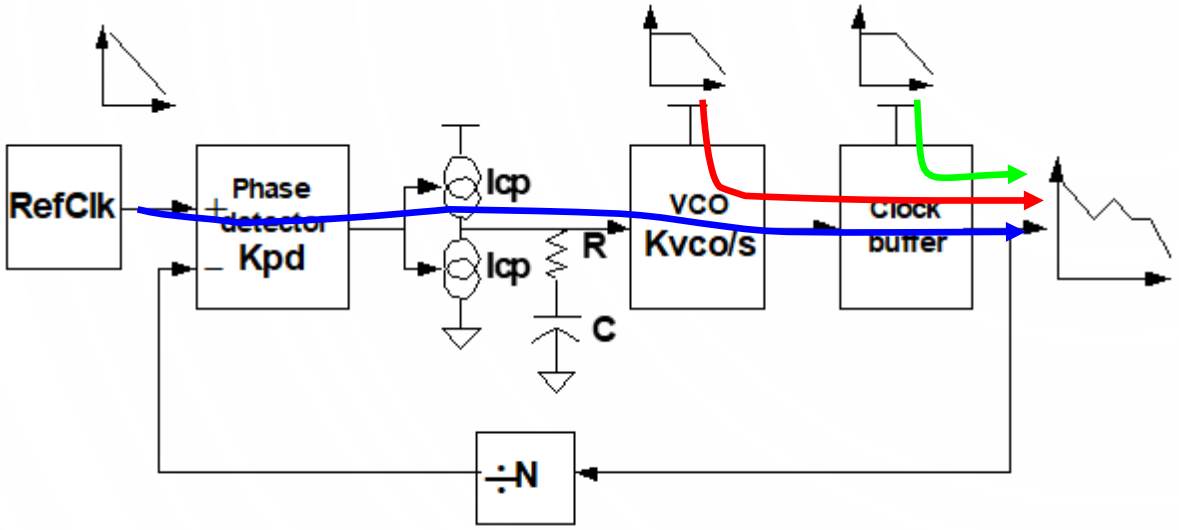
Adding clock buffers – all noise transfer functions

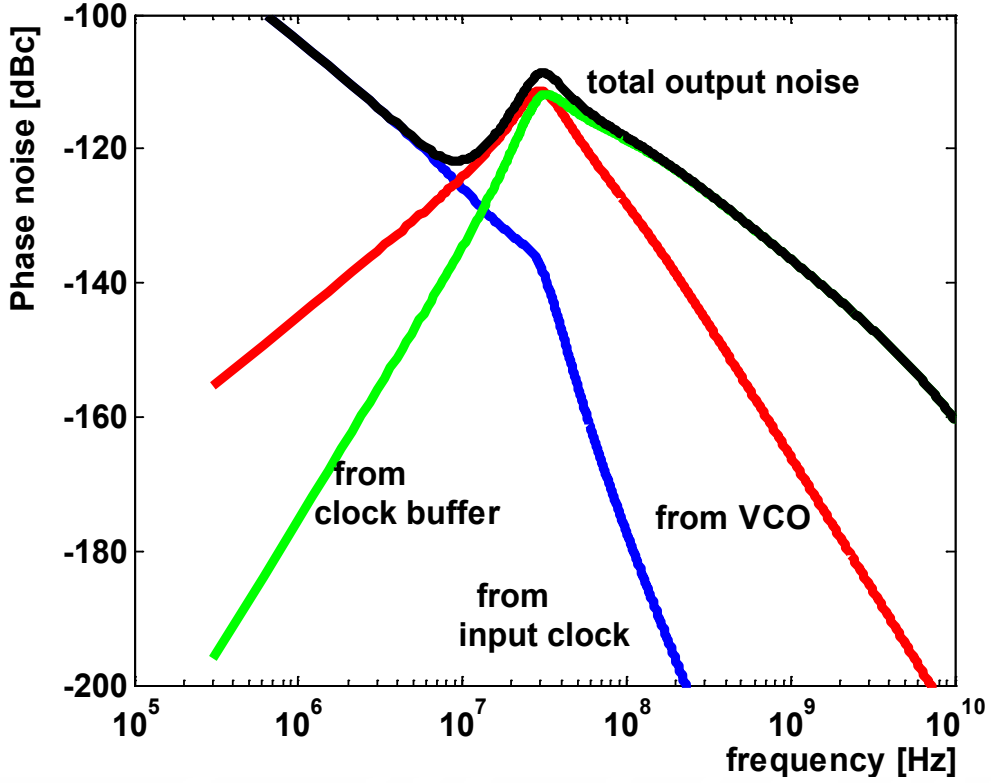




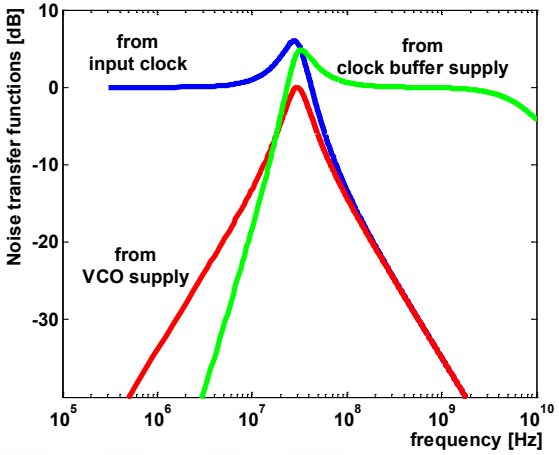
- Noise Transfer Functions (NTFs)
  - Low-pass from refclk
  - Band-pass from VCO supply
  - High-pass from clock buffer supply

Resulting Output Phase noise spectrum





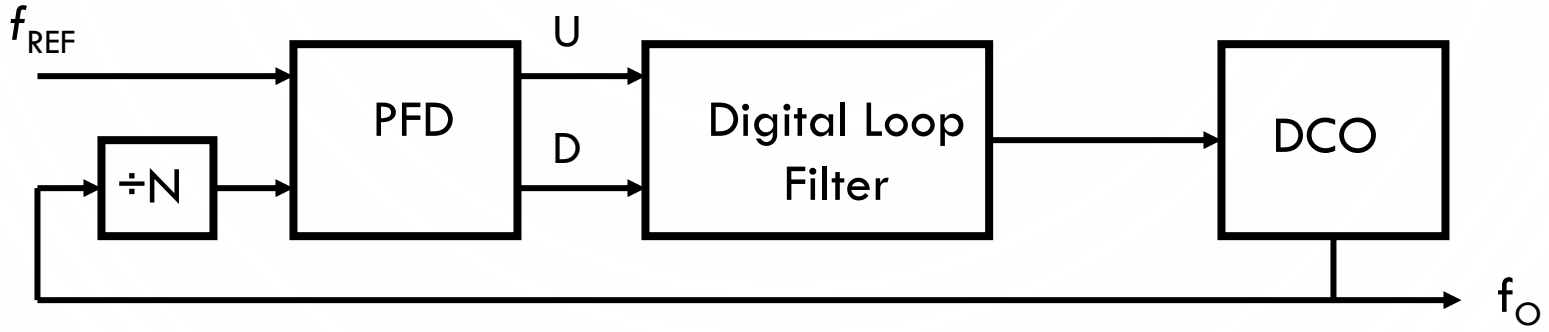
- Set by reference clock f < loop bandwidth
- Set by supply noise f > loop bandwidth



Digital PLLs

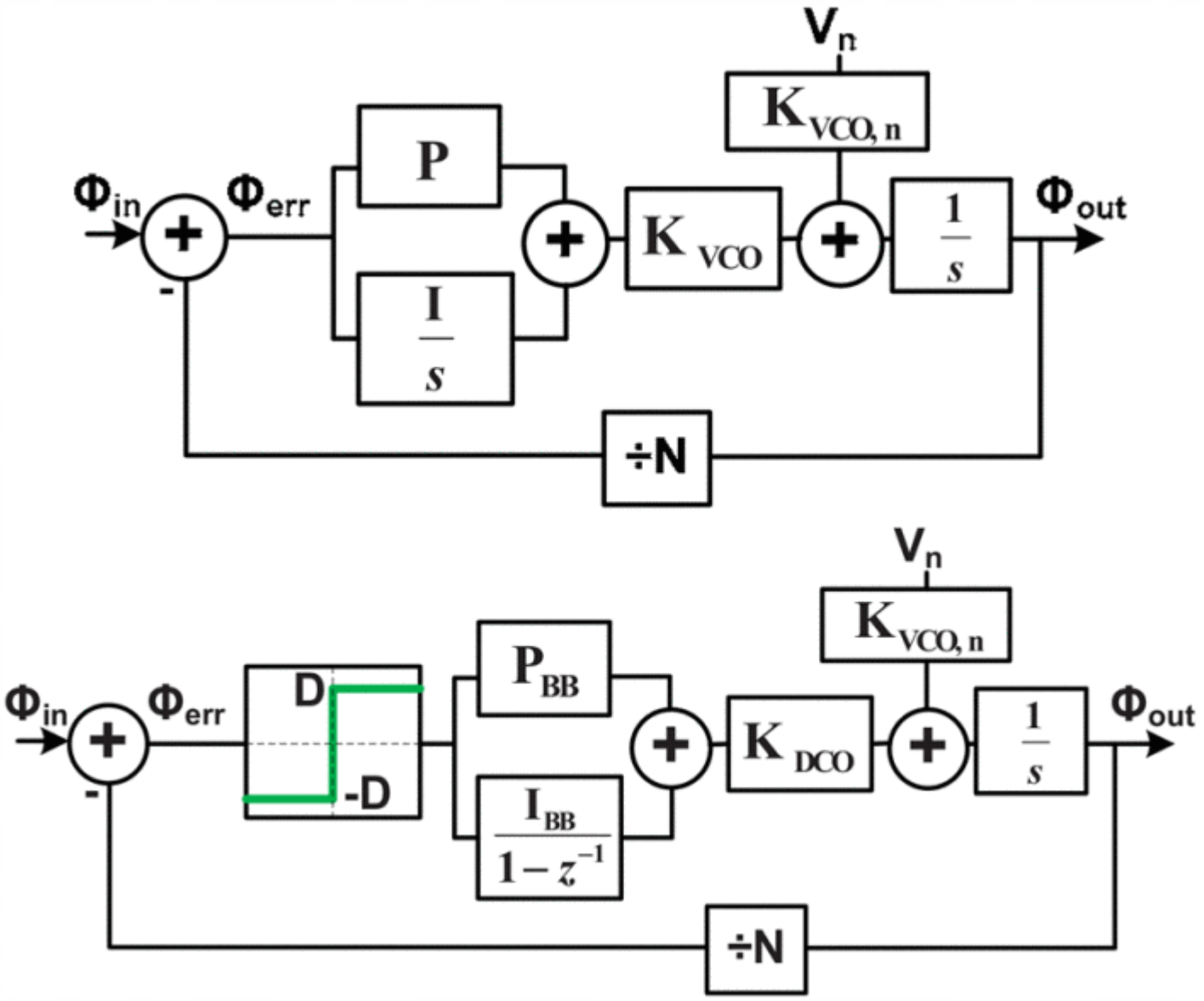
Digital PLL

- Replace analog functions with digital equivalents



- **Digitally-controlled oscillator (DCO)**

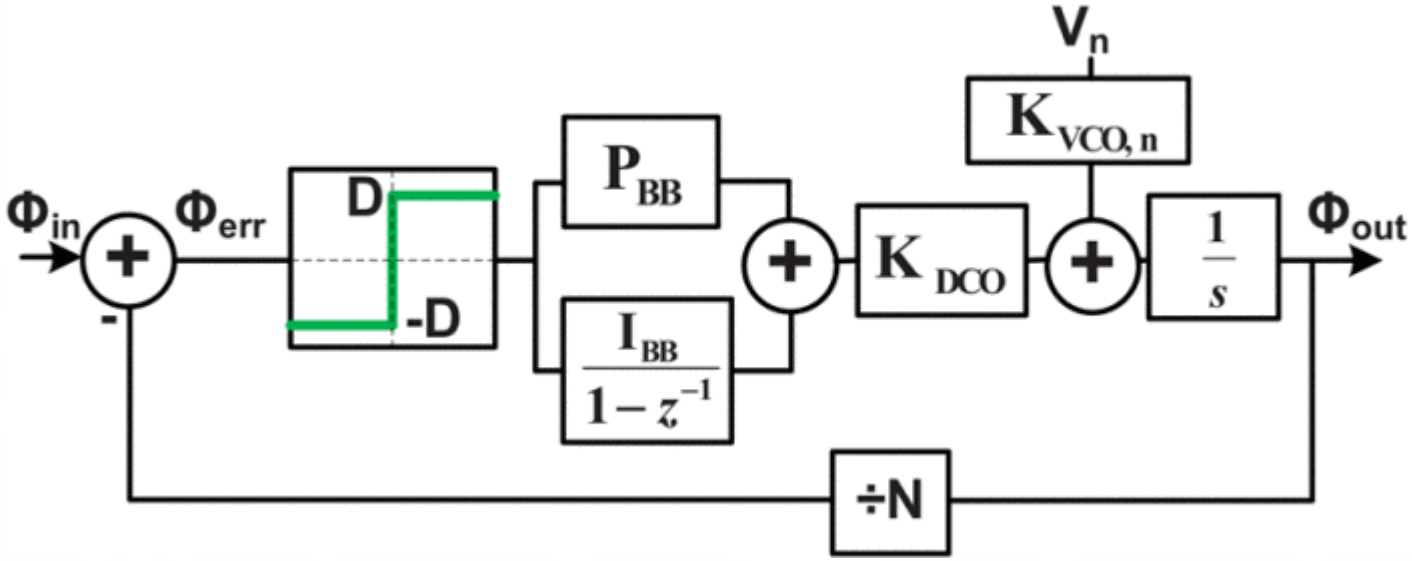
Digital vs Analog PLL



Crossley CICC11

Digital PLL Quantization noise

- Limit cycle phase noise adds to the linearized model phase noise



$$\varphi_{out,lc,p-p} = T_{ref} \cdot K_{DCO} \cdot (2P_{BB} + I_{BB})$$

$$\varphi_{out,lc,rms} = \frac{T_{ref} \cdot K_{DCO}}{\sqrt{3}} \cdot \sqrt{P_{BB}^2 + P_{BB} \cdot I_{BB} + \frac{I_{BB}^2}{2}}$$

Digital PLL Analysis

- Loop parameters can be matched to the analog PLL

$$P_{BB} = \frac{\mathrm{P}\cdot\mathrm{K_{VCO}}}{\mathrm{Gain_{BB}}\cdot\mathrm{K_{DCO}}}$$

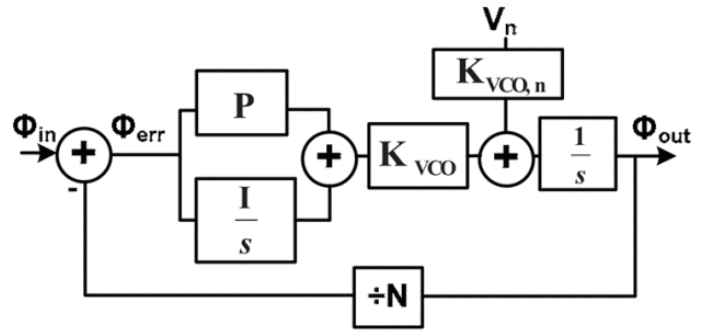
$$I_{BB} = \frac{\mathrm{I}\cdot\mathrm{T_{ref}}\cdot\mathrm{K_{VCO}}}{\mathrm{Gain_{BB}}\cdot\mathrm{K_{DCO}}}$$

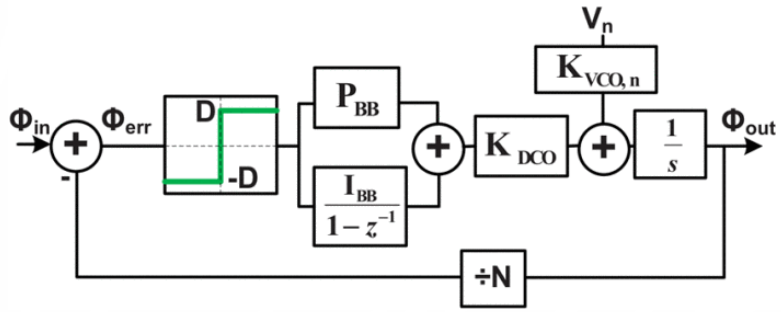
$$Gain_{BB} = \sqrt{\frac{2}{\pi}}\cdot\frac{\mathrm{D}}{\sigma_{\phi_{err}}}$$

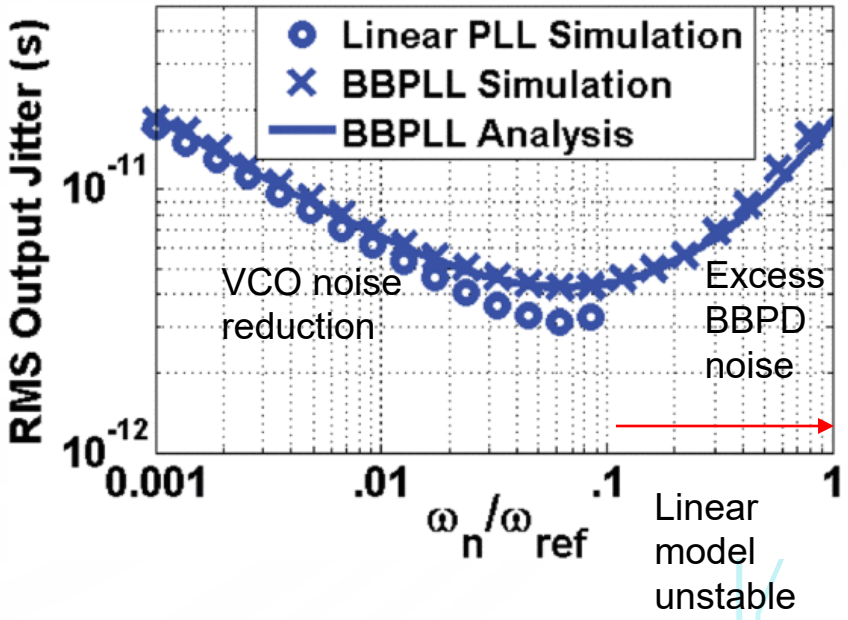
Linear VCO noise to output phase:

$$\varphi_{out,rms} = \sqrt{\frac{\pi}{2}}\cdot\frac{1}{4\cdot \mathrm{P_{BB}}\cdot \mathrm{K_{DCO}}}\cdot\frac{\left(\sigma_{V_n}\cdot \mathrm{K_{VCO,n}}\right)^2}{\Delta f}$$

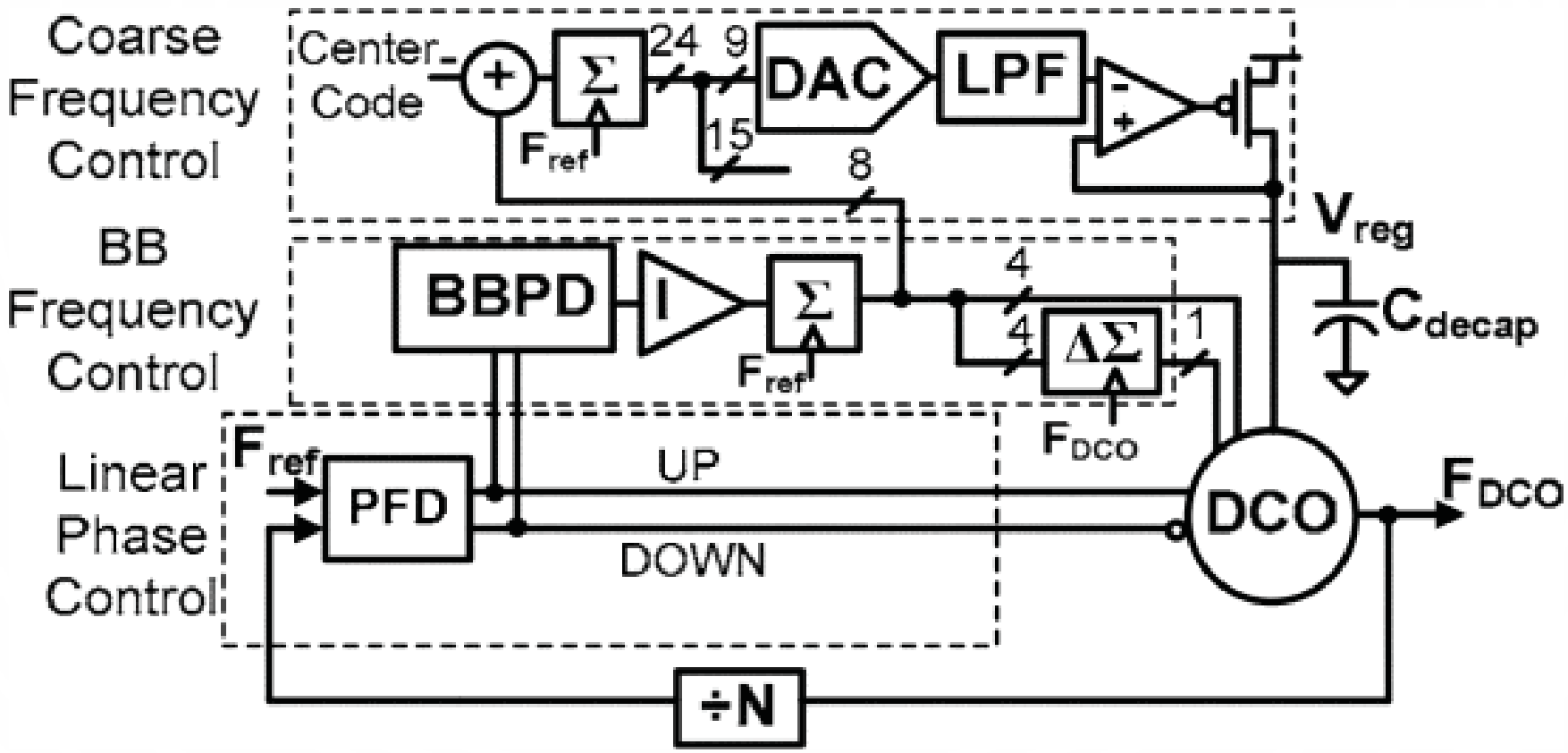
VCO thermal and supply noise (assume it dominates)





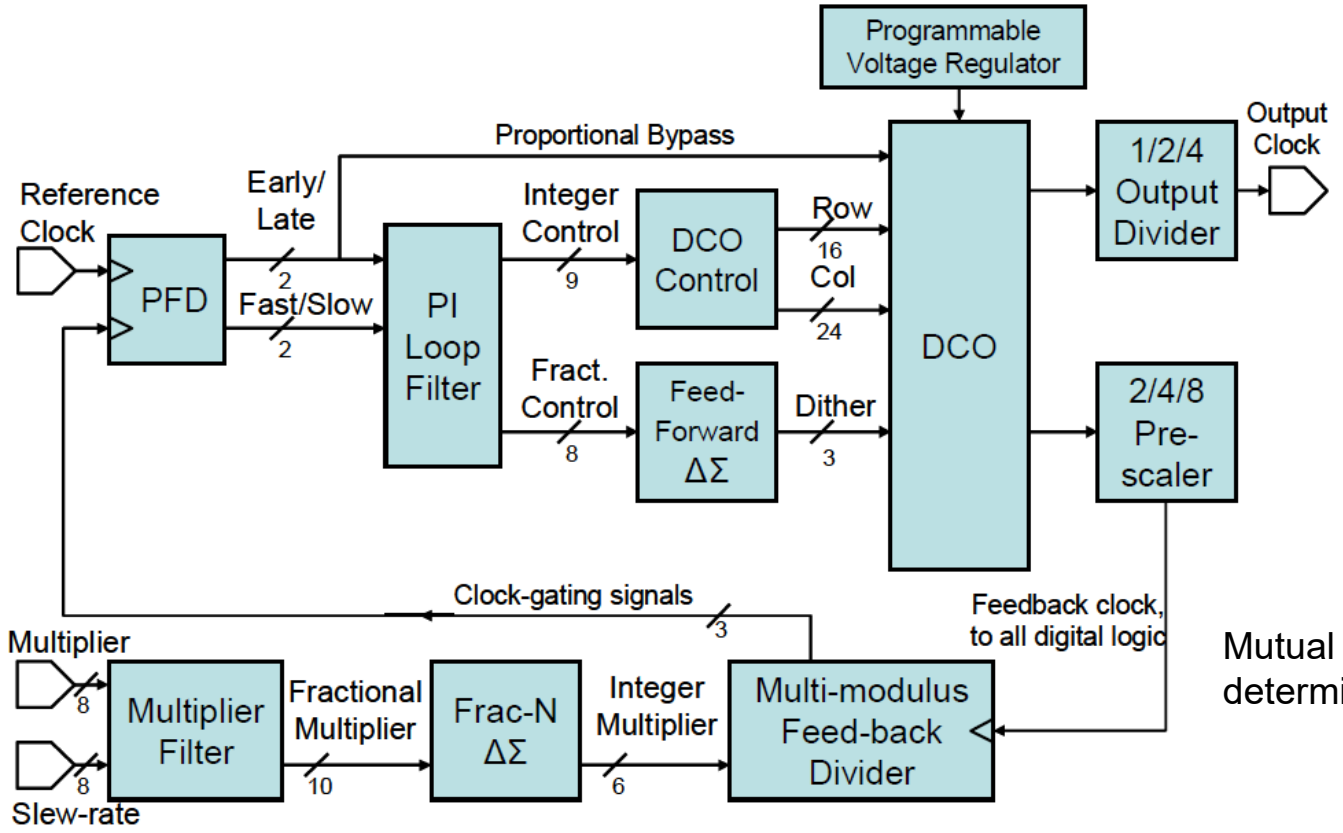


Digital BBPD-PLL

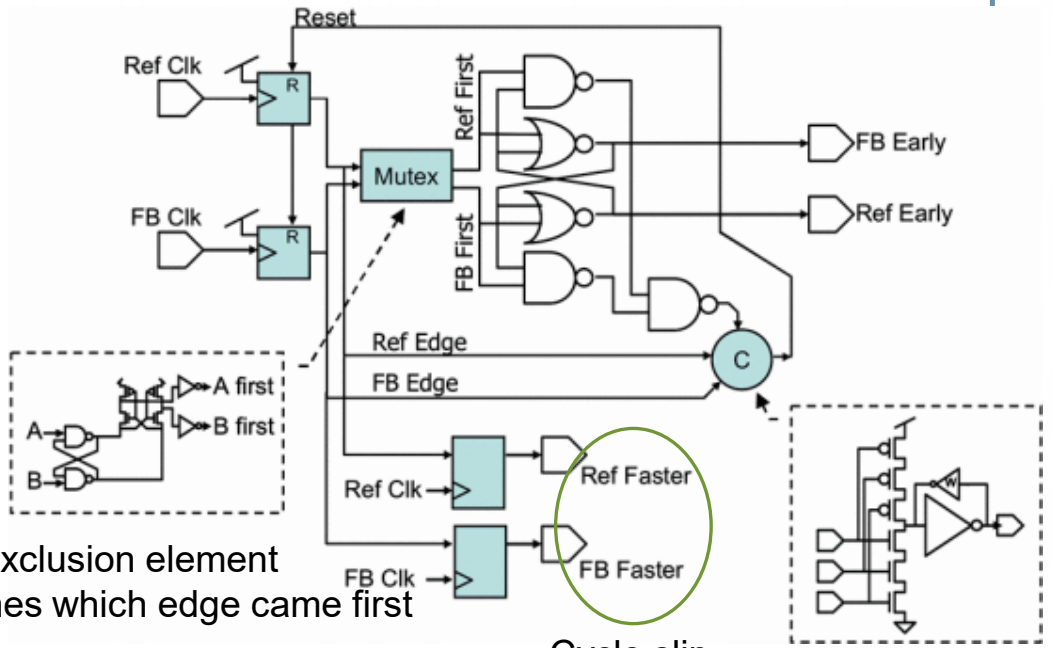


- PFD to DCO direct proportional path for faster phase tracking

Practical Digital PLL



PFD



Mutual exclusion element determines which edge came first

Cycle slip detect

Self-timed reset

- In IBM Power7 processor, per each core

Tierno, JSSC'08

Tierno, VLSI'10

Next Lecture

- Clock distribution
- Power-supply regulation