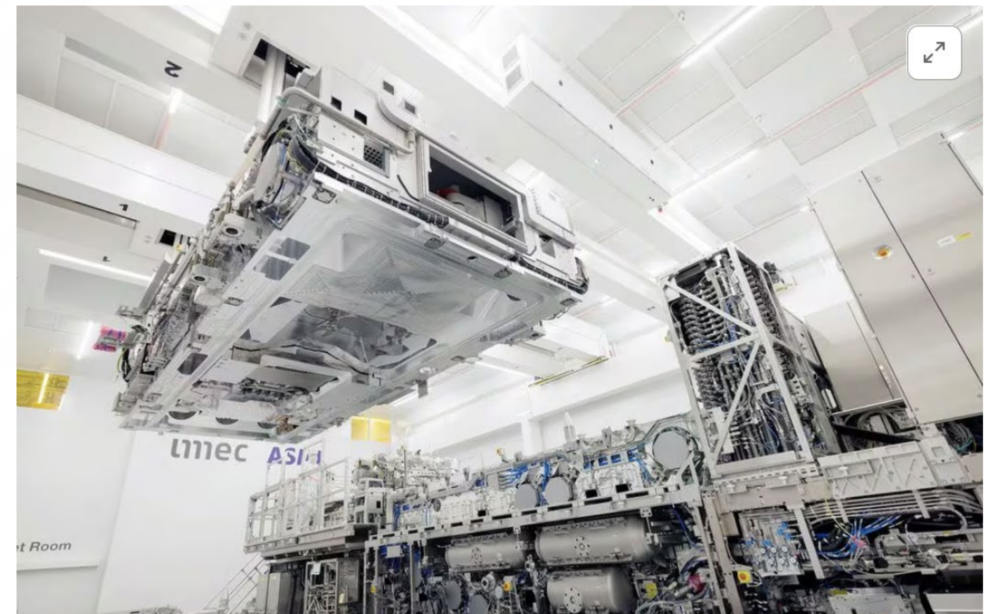
EECS251B : Advanced Digital Circuits and Systems

Lecture 9 – Implications of Lithography

Borivoje Nikolić

February 9, 20249:06 AM PST: ASML's next chip challenge: rollout of its new $350 mln 'High NA EUV' machine.

Chip toolmaking giant ASML (ASML.AS), said on Friday it was gearing up production of its new $350 million "High NA EUV" machine, a device the size of a double decker bus central to its bid to keep its lead in a $125 billion market.



https://www.reuters.com/technology/asmls-next-chip-challenge-rollout-its-new-350-mln-high-na-euv-machine-2024-02-09/

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Announcements

- Lab 4 this week
- Homework 2 will be posted this week
- Project survey follow-up
- No Lecture next Tuesday, February 19 (ISSCC)

A Perspective on Scaling

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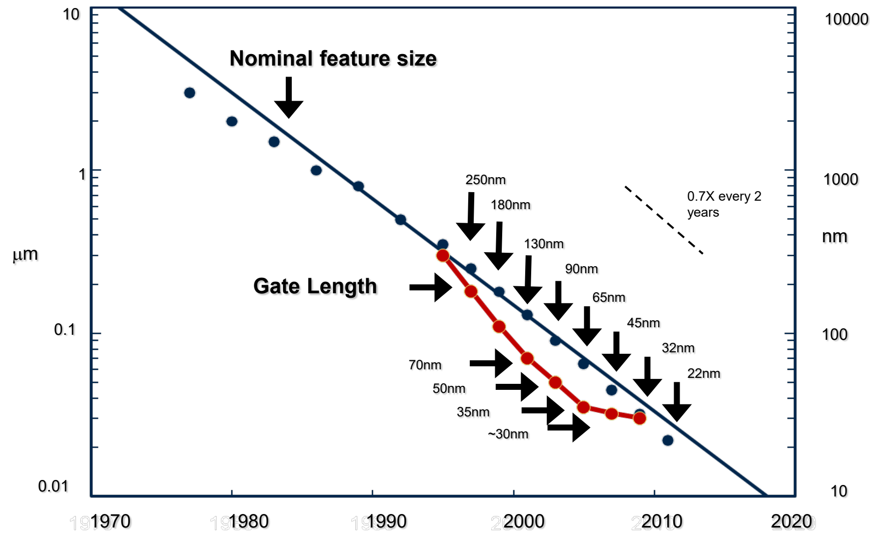
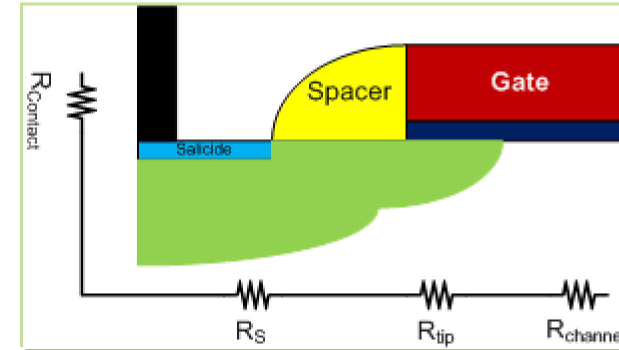
Lg, R, C scaling

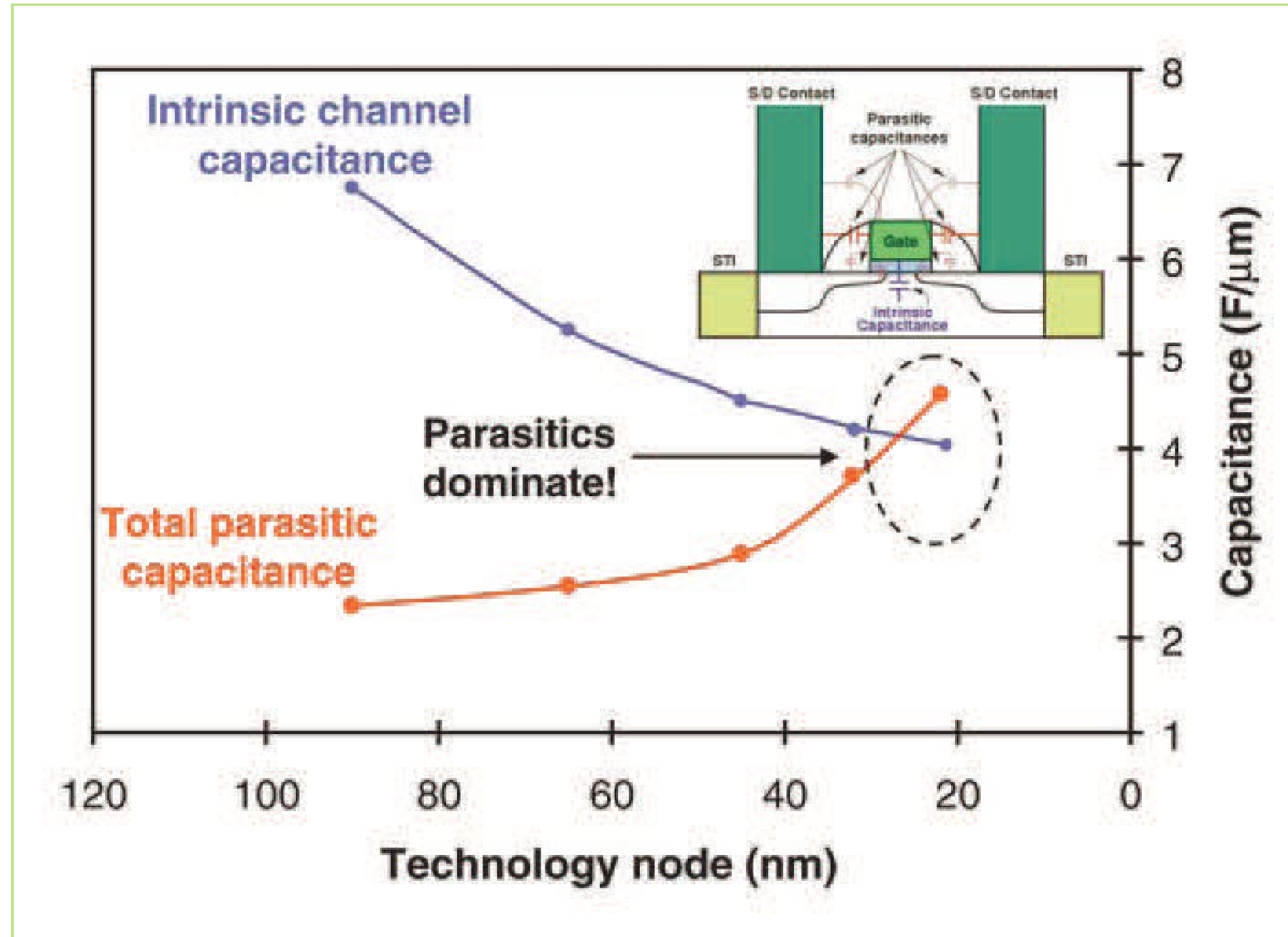




- With scaling L, need to scale up doping - scale junction depth (control leakage) – S/D resistance goes up
- External resistance limits current

$$I_D \approx V_{DS} / \left(R_{channel} + R_{ext} \right)$$

Parasitic Capacitance Scaling



Reality: Overlap + fringe can be 50% of $C_{channel}$ in 32nm

S. Thompson, *Materials Today*, 2006.

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Lithography Implications

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Lithography – Key Points

- Current lithography restricts features in design, affects variability
- This is changing with EUV
  - Long time to come
  - Deployed at 5nm (Samsung, TSMC, Intel) – transistors, contacts
  - Extended deployment at 3nm- and 2nm-class technologies

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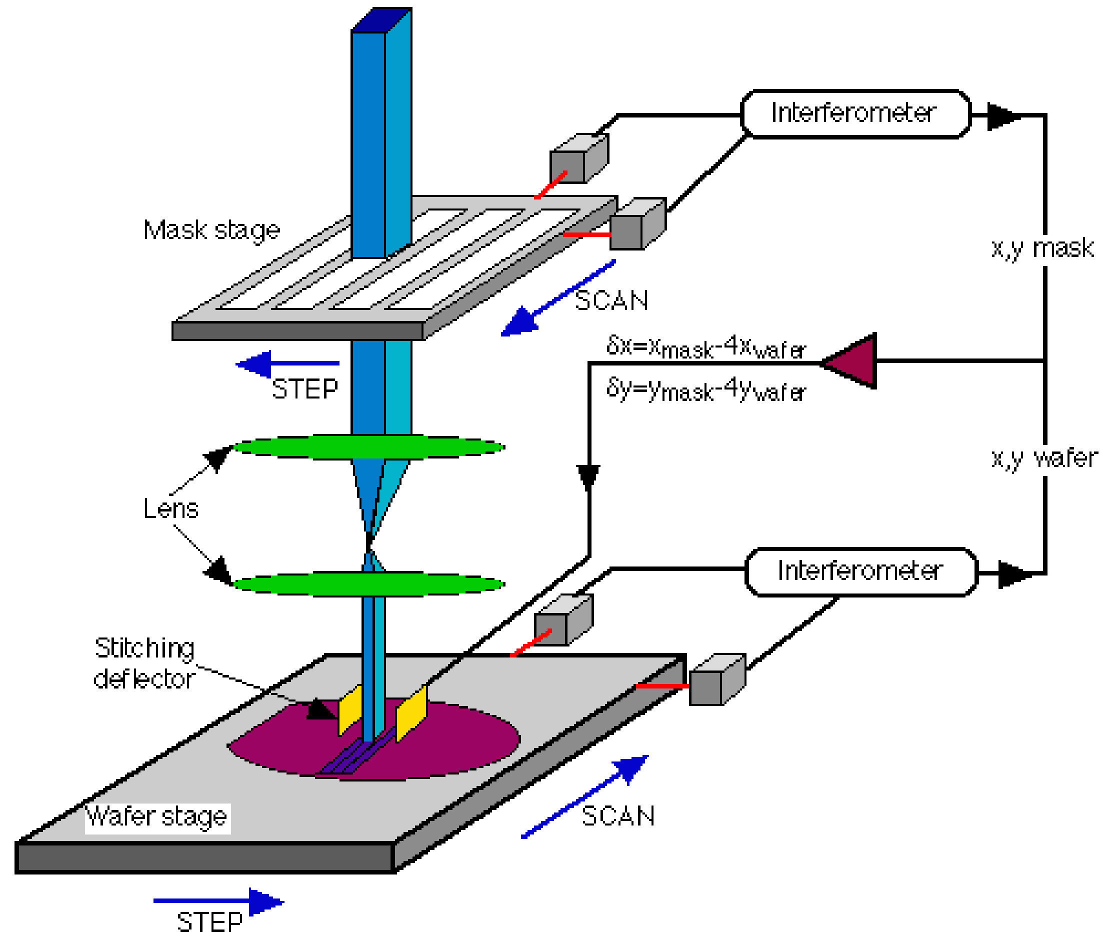
Step-and-Scan Lithography



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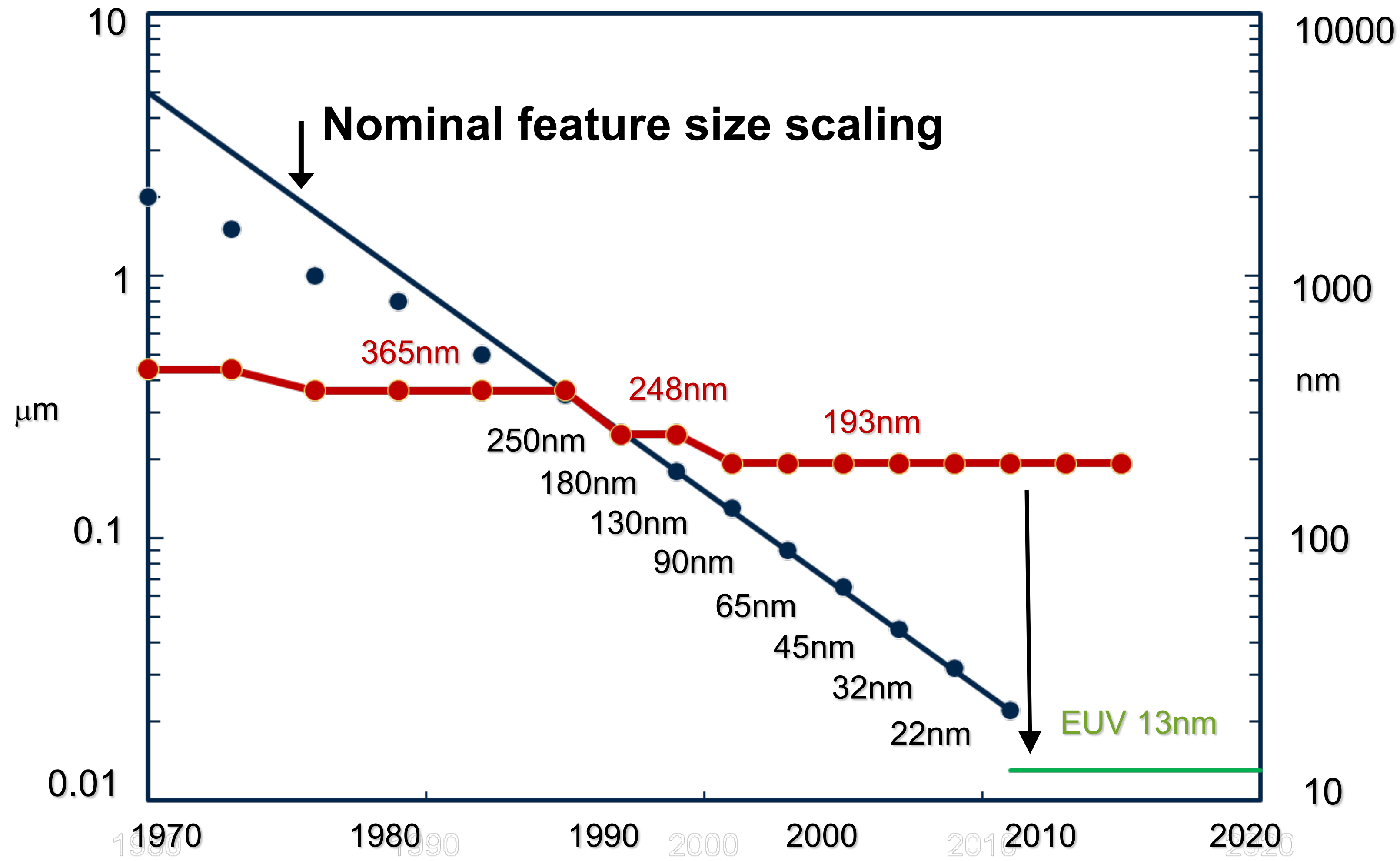
Lithography Scaling



EUV – Technology of the future (forever)?

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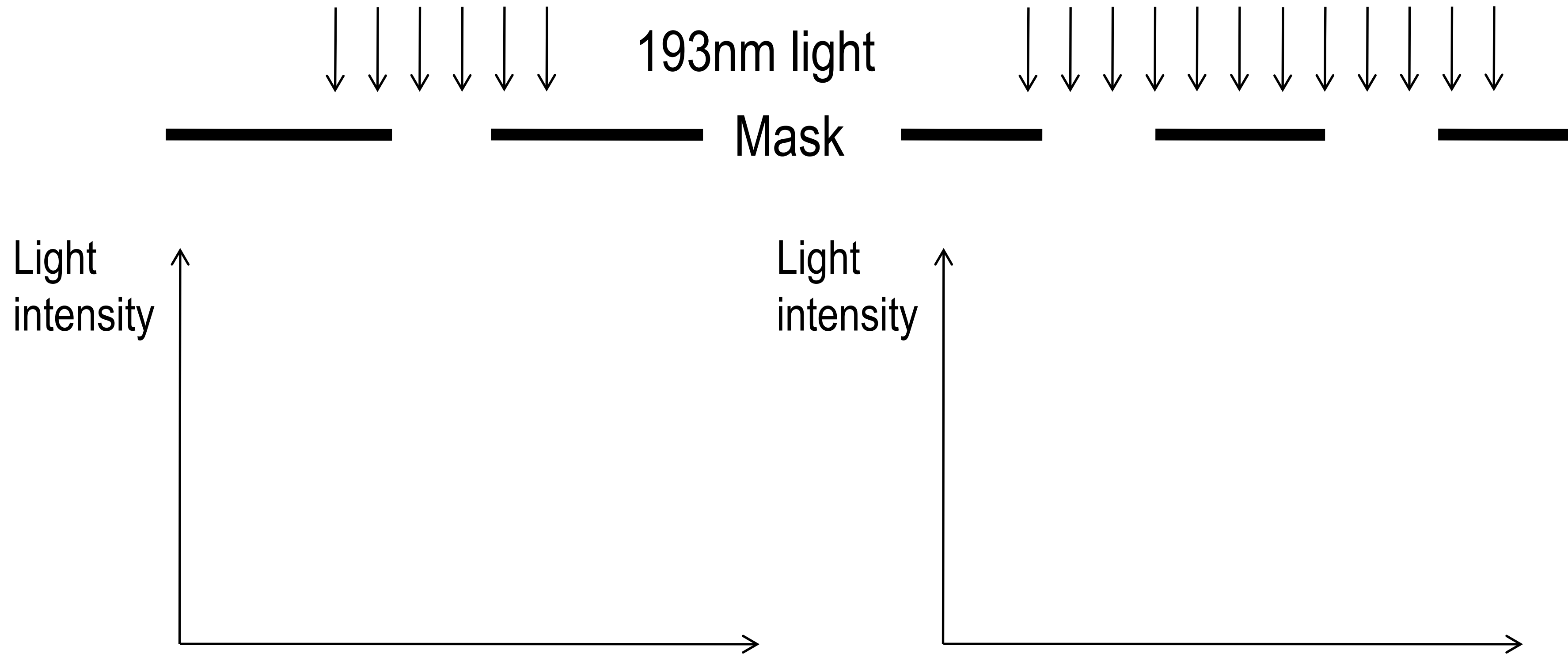
Sub-Wavelength Lithography

- Light projected through a gap



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Sub-Wavelength Lithography

- CD ~ half pitch
- Decrease λ
  - DUV: 193 nm (ArF excimer laser)
  - EUV: 13.5nm
- Increase $NA = n\sin\alpha$
  - Maximum n is 1 in air
  - Presently: ~0.92-1.35
  - Immersion
- Result: Shrinking k1
  - Presently: 0.35 – 0.4
  - Theoretical limit: 0.25

$$CD = k_1 \frac{\lambda}{NA}$$

$$CD_{min} = k_1 \frac{\lambda}{NA} = 0.25 \frac{193nm}{0.92} = 50nm$$

22nm pitches at (or beyond) resolution limit

Intel

Node	CPP	MxP	FP
65nm	230	230	
45nm	160	160	
32nm	112.5	112.5	
22nm	90	80	60
14nm	70	52	42
10nm	54	36	34
7nm	37	32	

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Litho: How to Enhance Resolution?

- Immersion
- Off-axis illumination
- Optical proximity correction
- Phase-shifting masks
- Double/multiple patterning
- EUV

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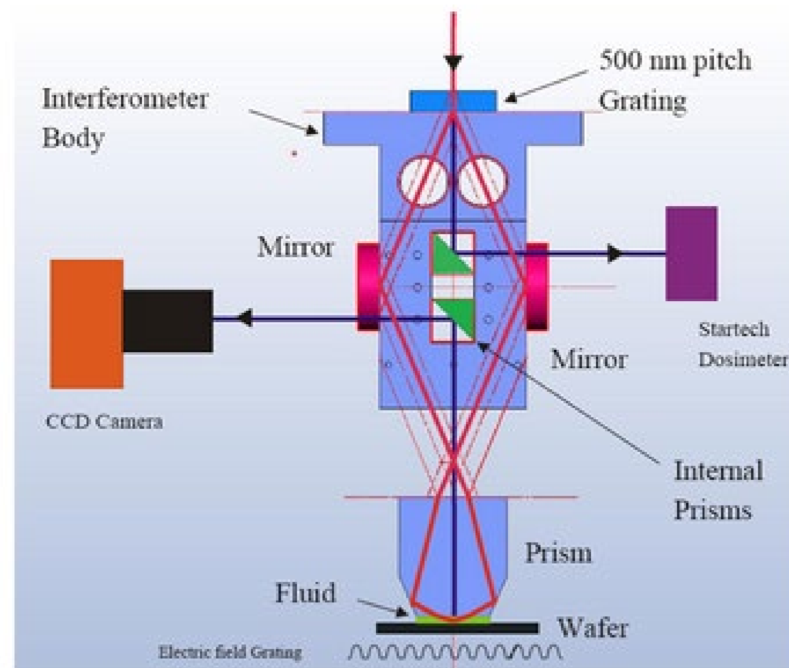
Litho (1): Immersion

- Project through a drop of liquid
- n_{water} = 1.47

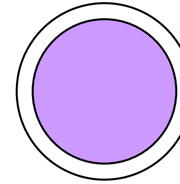
$$CD_{\min} = k_1 \frac{\lambda}{NA} = 0.25 \frac{193nm}{1.35} = 35nm$$



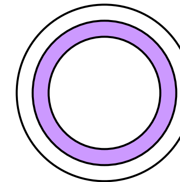
IBM

Litho (2): Illumination

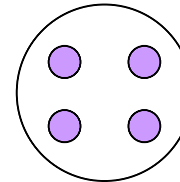
- Amplifies certain pitches/rotations at expense of others
  - Regular Illumination



  - Many off-axis designs (OAI)
    - Annular



    - Quadrupole / Quasar



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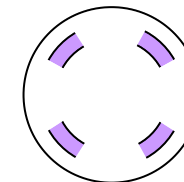
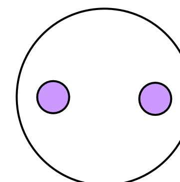


    - Dipole



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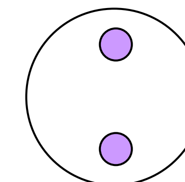
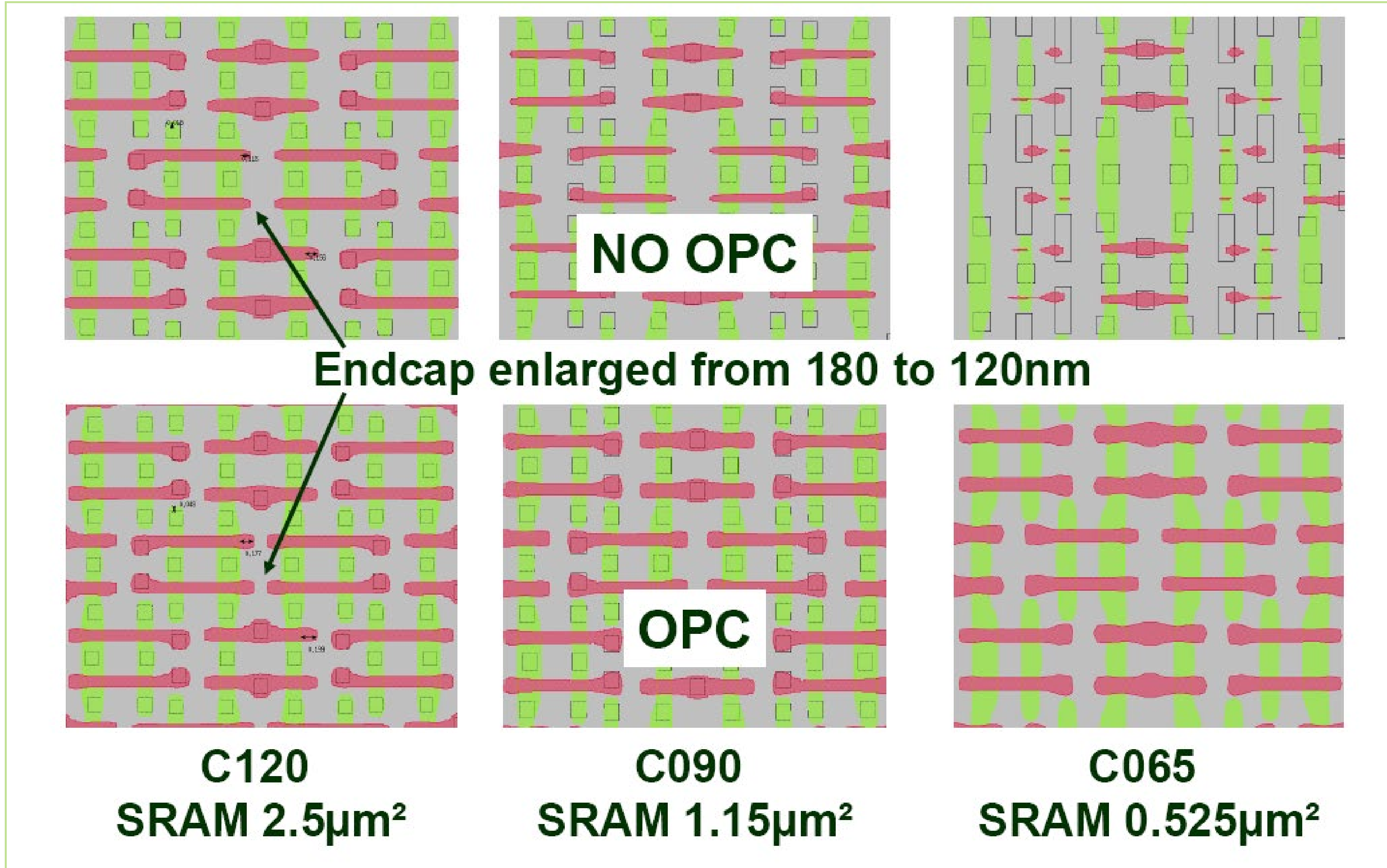


A.Kahng, ICCAD'03

Litho (3): Resolution Enhancement



J.Hartmann, ISSCC'07

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Litho (3): OPC

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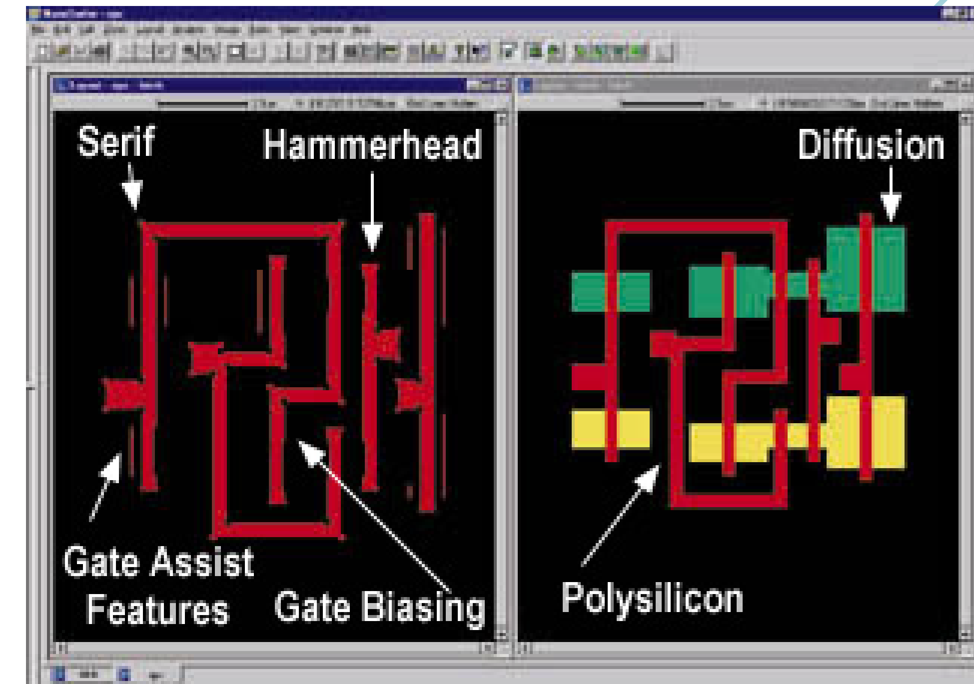
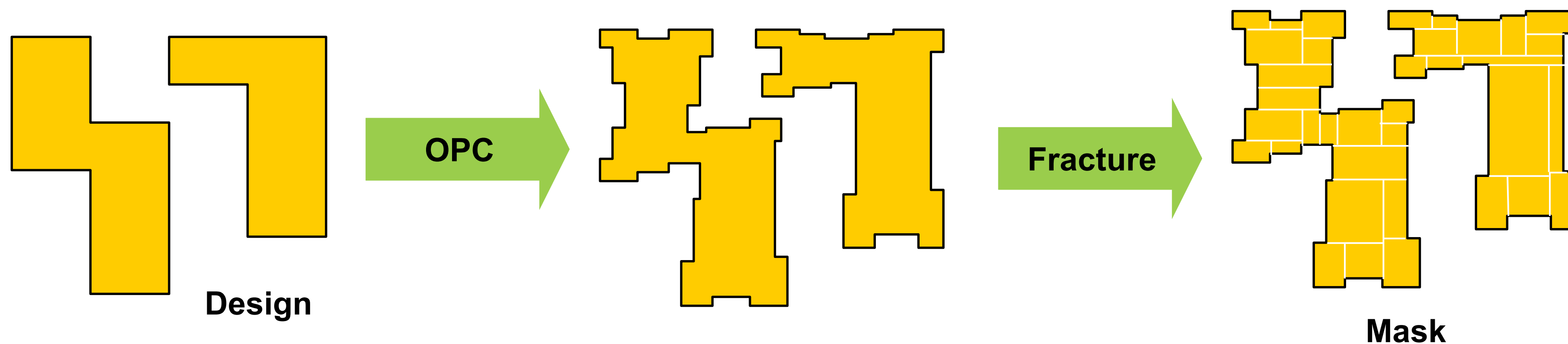
Litho (3): OPC

- Optical Proximity Correction (OPC) modifies layout to compensate for process distortions
  - Add non-electrical structures to layout to control diffraction of light
  - Rule-based (past) or model-based





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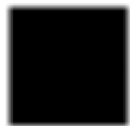
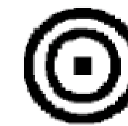
Inverse Lithograpphy Techniques

- OPC vs. ILT

Optical Proximity Correction		Inverse Lithography Technology	
45nm node	28nm node	14nm node	7nm node
without OPC	normal OPC	normal ILT	ideal ILT
			

https://semiengineering.com/what-happened-to-inverse-lithography/

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Extreme Ultraviolet Lithography

- Wavelength λ = 13.5nm
- Lower wafer throughput
- Simpler design rules (single patterning)
- Used on critical layers

- First deployed by Samsung in 7nm node (Exynos 9825 SoC)
  - Also used by Intel in 7nm, TSMC in 5nm [J.C. Liu, IEDM'20]

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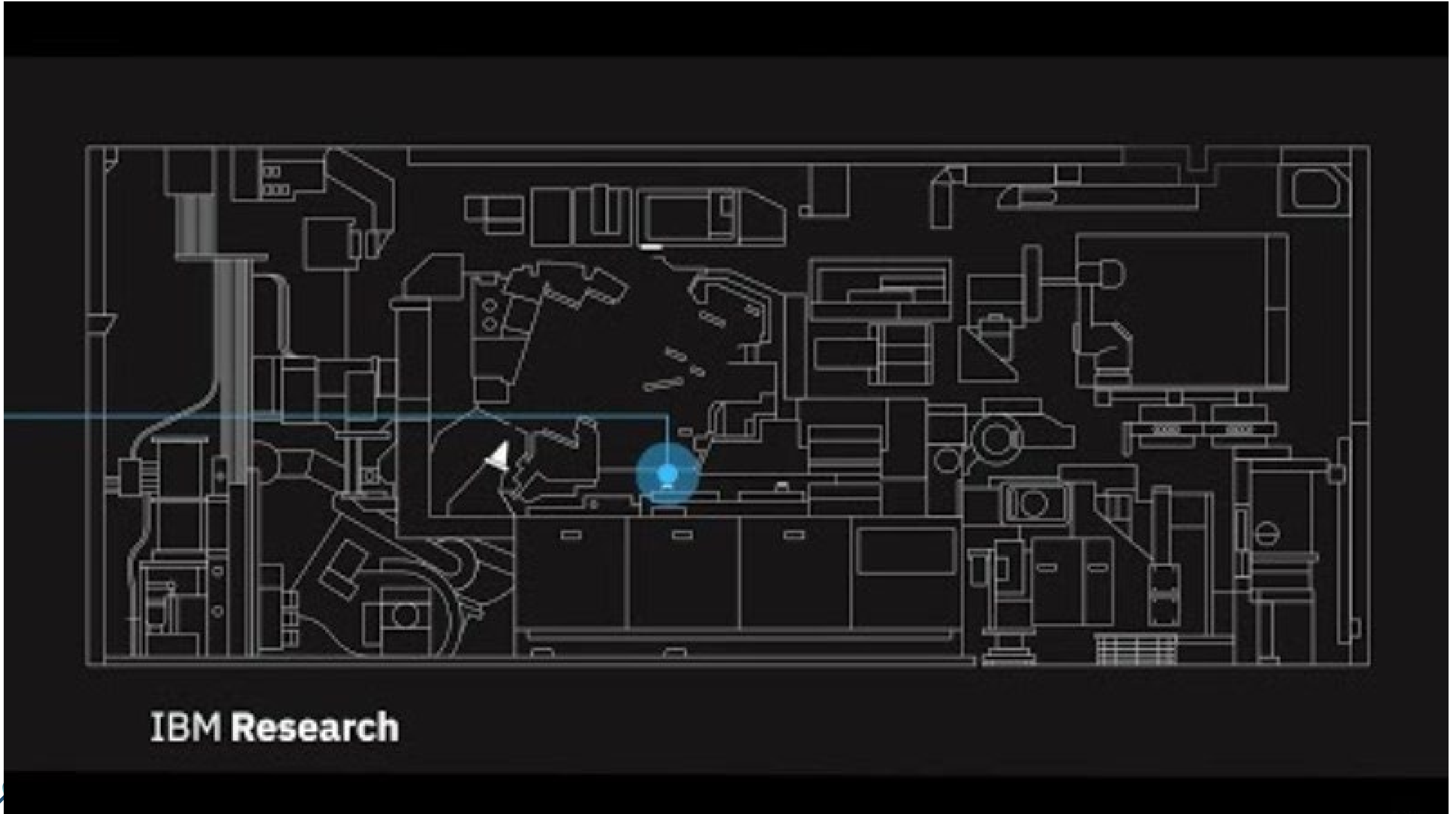
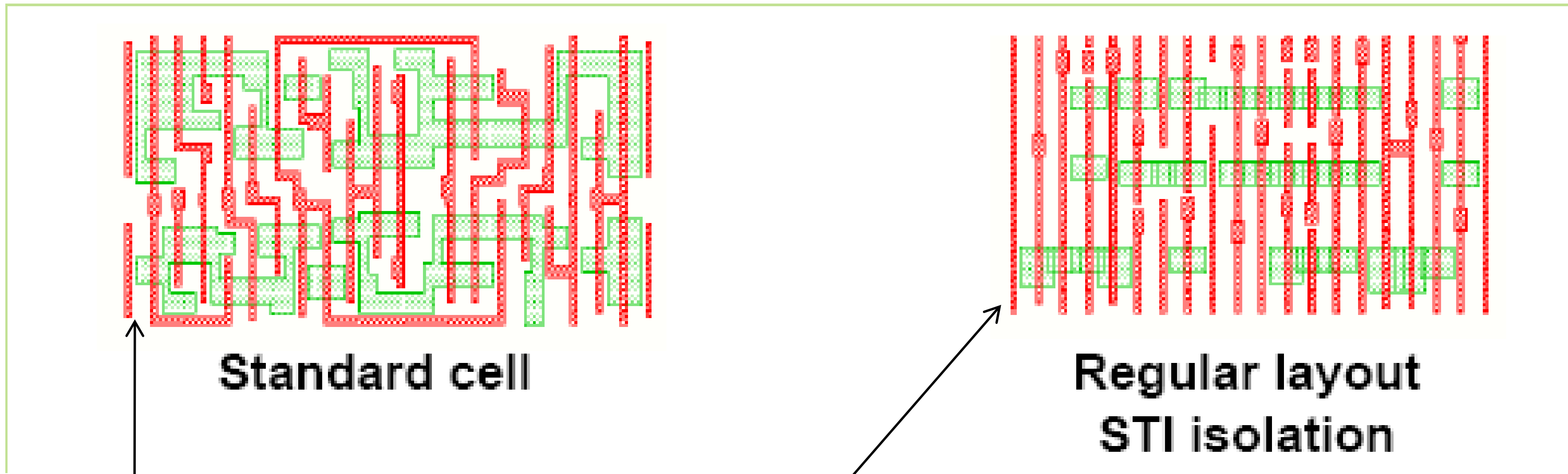
EUV Video



Litho (4): Restricted Design Rules



Also: note poly density rules

J.Hartmann, ISSCC'07

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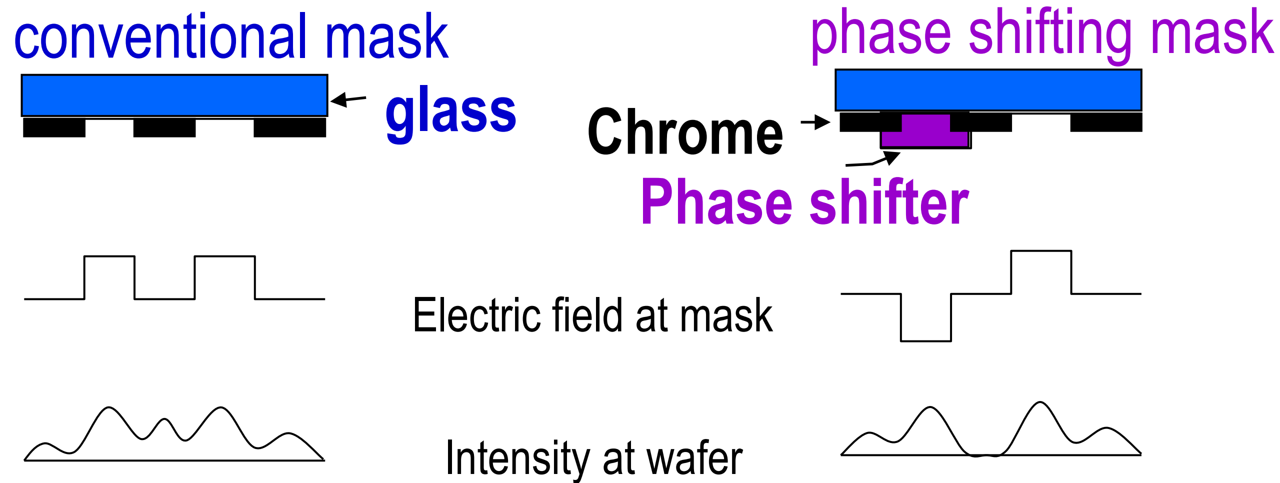
Litho (5): Phase-Shift Masks

- Phase Shifting Masks (PSM)
  - Creates interference fringes on the wafer →Interference effects boost contrast →Phase Masks can make extremely small lines



A.Kahng, ICCAD'03

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Litho (6): Double Patterning

- Double exposure double etch
  - Double exposure double etch
  - Pitch split, litho-etch-litho-etch (LELE)
- Self-aligned methods
  - Self-aligned double patterning
  - Self-aligned quadruple patterning

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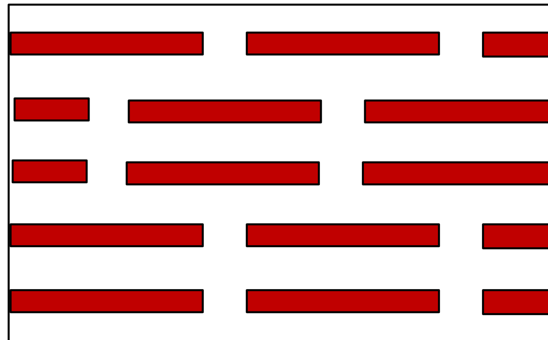
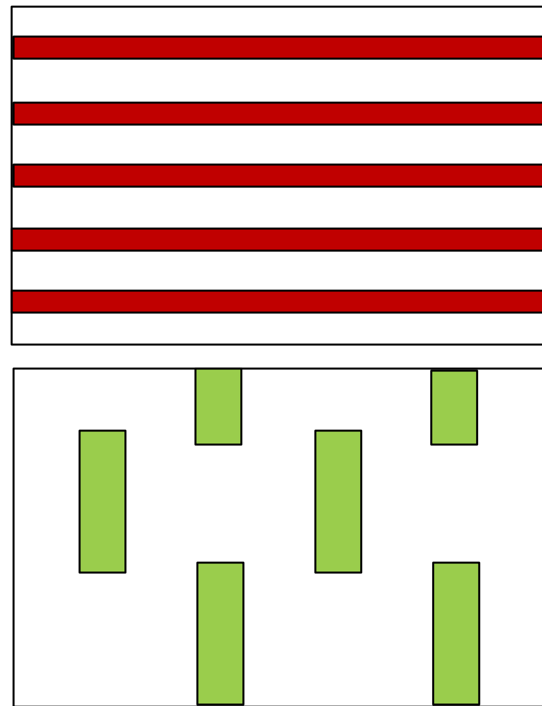
Double-Exposure Double-Etch

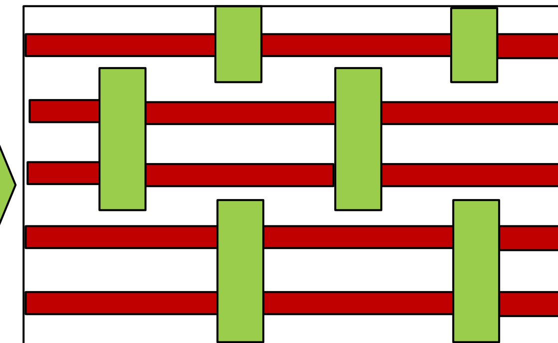
Starting layout



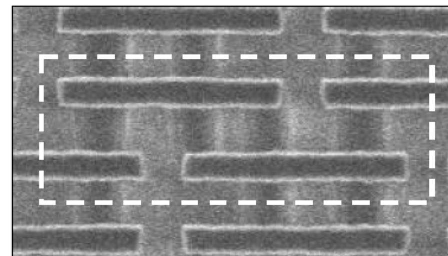
Line + cut split



Cut over line



Result:



SRAM image from K. Mistry, IEDM'07

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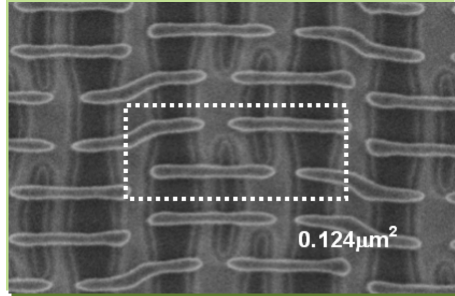
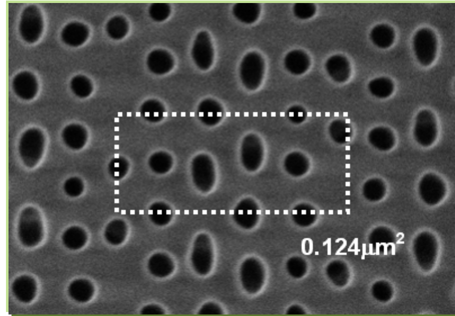
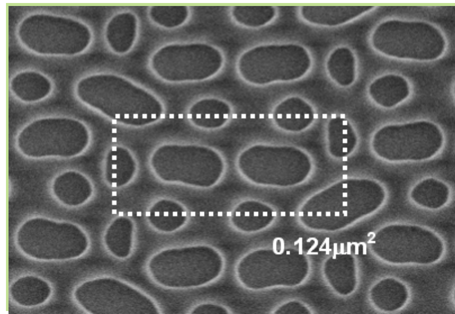
32nm Examples

Single exposure

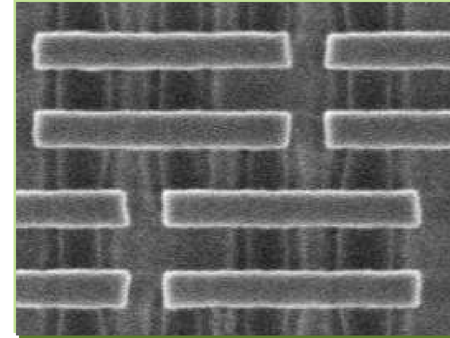






IEDM'08

Double exposure



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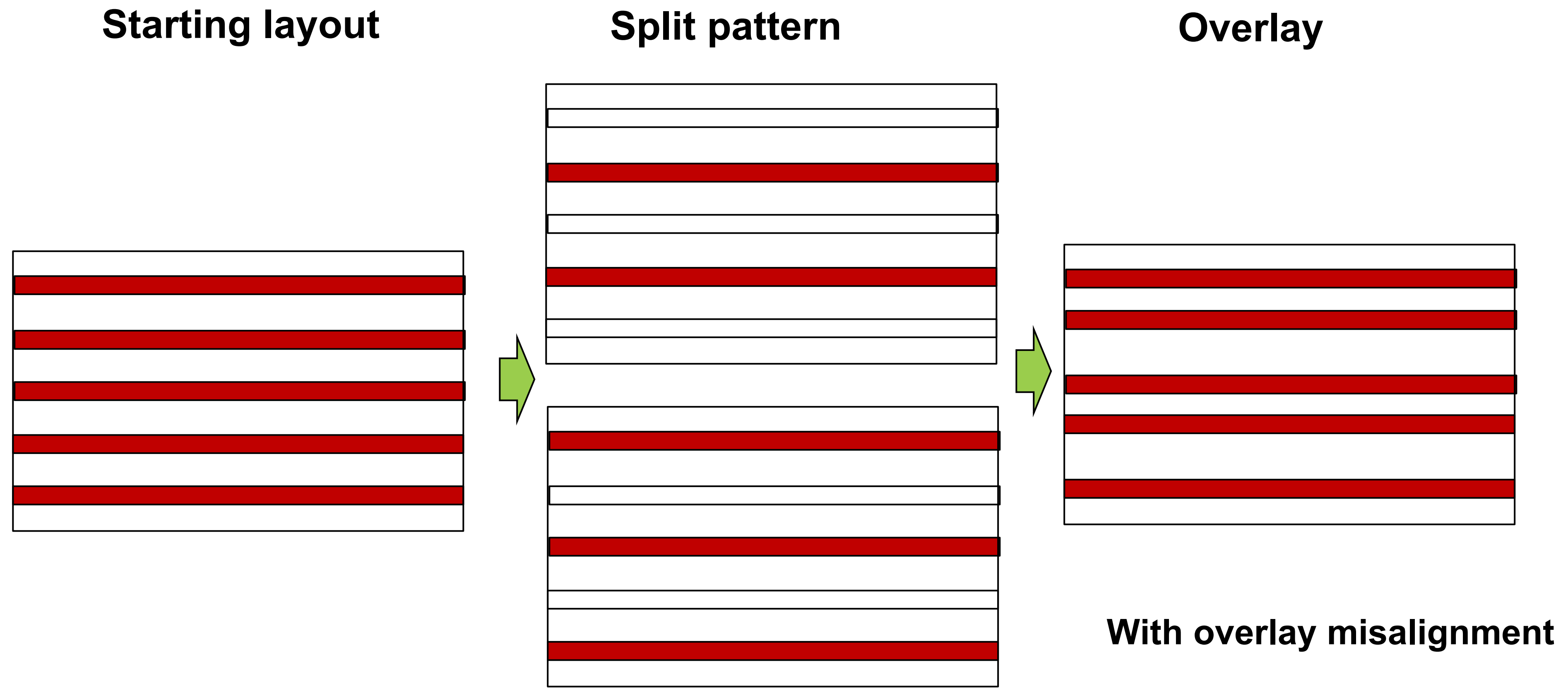
Pitch-Split Double Exposure



Also called litho-etch-litho-etch (LELE)

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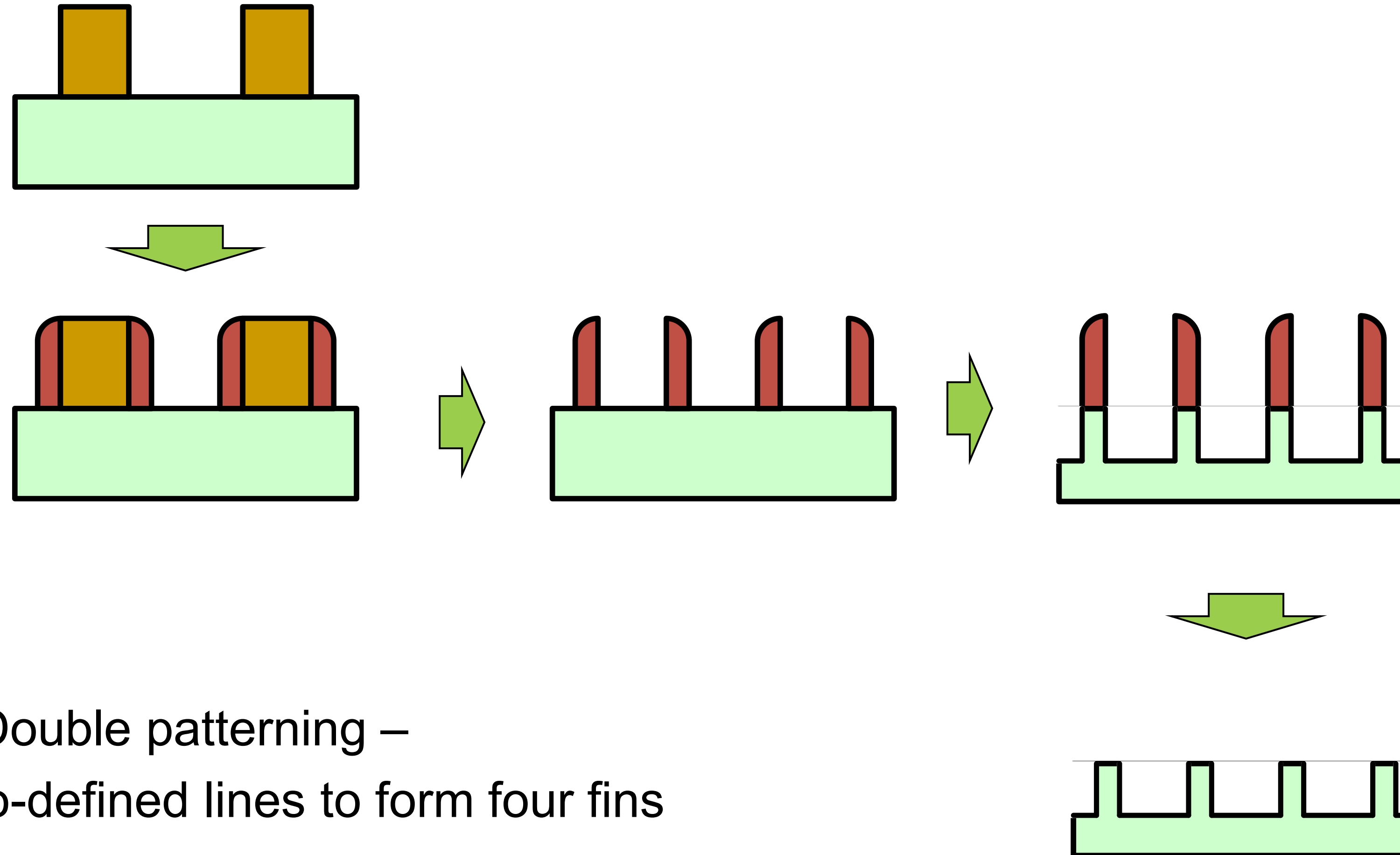
Self-Aligned Double Patterning (SADP)



- SADP: Double patterning –
  Two litho-defined lines to form four fins
- SAQP: Quadruple patterning

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Litho: Design Implications

- Forbidden directions
  - Depends on illumination type
  - Poly lines in other directions can exist but need to be thicker
- Forbidden pitches
  - Nulls in the interference pattern
  - Multiple patterning
- Forbidden shapes in PSM, multiple-patterning
- Assist features
  - If a transistor doesn't have a neighbor, let's add a dummy

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Litho: Current Options (Beyond 10nm)

- Multiple patterning
  - NA ~ 1.2-1.35
- EUV lithography
  - λ = 13.5nm

Normalized wafer cost adder*	
SE	1
LELE	2.5
LELELE	3.5
SADP	2
SAQP	3
EUV SE	4
EUV SADP	6

*TEL™ Internal calculation

Cost adder reduced with increased power/throughput of EUV

A. Raley, SPIE'16

cc BY NC SA

Summary

- Transistors are changing
  - Dennard's scaling ended around 2005
  - Moore's Law is ending
- FinFET and FDSOI processes deployed now
  - Expected to be replaced by nanosheets
- Lithography and manufacturing restrict design rules
  - Need to be aware of implications on design
- More changes coming: forksheets, buried power rails, chiplets – 2.5D and 3D

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Next Lecture

- Features of modern processes
- Projects

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