EE251B Advanced Digital Integrated Circuits and Systems   **Spring 2024.**

Your Name: EE251B

Quiz 1.   **Tuesday, February 26, 2024. in class.**

Please show all your work.
Consider a 2D 4x4 mesh network on a chip with 16 processor cores. Interconnect width is 256 bits and packet sizes are 1024 bits. Please calculate:

a) Maximum number of hops in this network is: 7 hops.
    Longest path is between opposite corners of the mesh. The number of hops (i.e. the number of routers) for this path is 7.

b) Bisection bandwidth of this network is: 2048 bits/cycle.
    4 channels cross the bisection in either direction, yielding a total bisection bandwidth of 2 * 4 * 256 = 2048 bits/cycle.

c) The total throughput of the network is: 4096 bits/cycle.
    The bisection bandwidth is half of the total throughput of the network (half of the data stays on the same side of the network, the other half crosses). The total throughput is therefore twice the bisection bandwidth (4096 bits/cycle).

• Assume that the latency of each channel (core-to-router or router-to-router) is 1 cycle.
• Assume the latency of each router to be 1 cycle.