EECS251B Advanced Digital Integrated Circuits and Systems **Spring 2024.**

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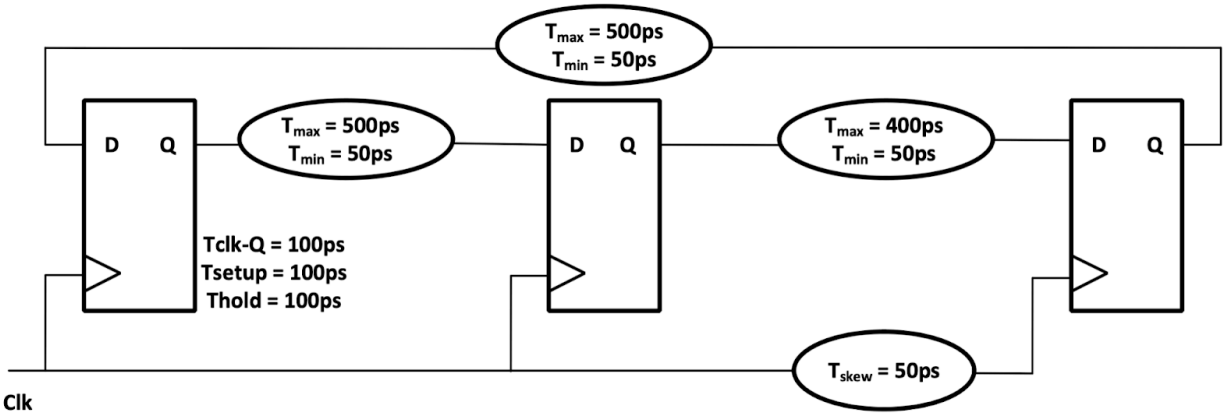
Quiz 3. **Thursday, April 4, 2024. in class.**
Please show all of your work.

A timing path is shown in figure below. Logic bubbles contain static combinational logic with indicated min and max delays. Flip-flop clk-Q delays, setup and hold times are indicated in the figure – and all flip-flops are the same.



What is the highest clock frequency that this circuit can operate at?

The skew indicates that the clock of register 3 arrives 50 ps after the clock of registers 1 and 2. As such, the skew increases the margin for the path from register 2 to 3 but decreases the margin for the path from register 3 to 1.

We can calculate the length of the critical path by calculating the minimum required clock period for each path.

$T_{clk} \geq T_{clk\text{-}Q} + T_{max} + T_{setup} - T_{skew}$

1 -> 2: $T_{clk} \geq 100\text{ ps} + 500\text{ ps} + 100\text{ ps} - 0\text{ ps} = 700\text{ ps}$
2 -> 3: $T_{clk} \geq 100\text{ ps} + 400\text{ ps} + 100\text{ ps} - 50\text{ ps} = 550\text{ ps}$
3 -> 1: $T_{clk} \geq 100\text{ ps} + 500\text{ ps} + 100\text{ ps} - (-50\text{ ps}) = 750\text{ ps}$

The critical path is 3 -> 1, which gives us a clock period of 750 ps and a clock frequency of 1.33 GHz.

f_{max} = 1.33 GHz