EECS251B Advanced Digital Integrated Circuits and Systems **Spring 2024.**

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Quiz 4. **Tuesday, April 16, 2024. in class.**
Please show all of your work.

Consider a conventional 6-T SRAM cell, sized to be stable at nominal operating conditions. The cell is supposed to be operated within a conventional, precharged bitline array. We would like to operate it at a reduced supply voltage so we are considering assist techniques. Let's analyze the effect of peripheral signals on the operation of the cell.

a) How does the increased wordline voltage affect the read stability of the cell?

Fill one: O Improves O Degrades O Doesn't affect

Explain: The access transistors are turned on more strongly, decreasing their effective resistance relative to the pull down transistors. This makes the internal nodes experience higher voltages during reads, increasing the potential for bit flips.

b) How does the increased wordline voltage affect the writeability of the cell?

Fill one: O Improves O Degrades O Doesn't affect

Explain: The access transistors are turned on more strongly, decreasing their effective resistance relative to the pull up transistors. This allows the access transistors to more effectively pull down the internal node voltage during writes.

c) How does the increased wordline voltage affect the read access time of the cell?

Fill one: O Improves O Degrades O Doesn't affect

Explain: The access transistors are turned on more strongly, increasing the current drawn from the bitline. The faster discharge of the bitline allows for shorter read access times.