UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

Last modified on	*Jan Rabaey*	*EECS 141*
October 1, 2007 by	*Homework #3: Delay, Power and Scaling*	
Louis Alarcon	*Due Monday, October 15th, 5pm*	

Problem 1 - Propagation Delay and Energy

a) What is the delay of a minimum sized inverter driving another inverter *f* times its size? For the minimum sized inverter, assume input capacitance equal to C_{unit}, equivalent resistance through the NMOS or PMOS equal to R_{unit}, and intrinsic (self-loading) capacitance on the output also equal to C_{unit}. Assume that the capacitance and resistance values scale linearly with size. Your answer will be in terms of these parameters (no calculations!). Take the limit as *f* goes to 0 and call the result τ_{inv}.

b) From part a), how much energy is consumed by the driving inverter after successive low to high (L→H) and high to low (H→L) transitions, in terms of a supply voltage V_{dd}?

c) In order to drive a large capacitance ($C_L=60C_{unit}$) from a minimum size gate (with input capacitance $C_{in}= C_{unit}$), you decided to introduce a two-stage buffer as shown in Fig. 1. From (a), the propagation delay of a self-loaded minimum size inverter is τ_{inv}. Assume that the capacitance and resistance values scale linearly with size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay. What is the corresponding propagation delay?

d) Given a supply voltage of V_{dd}, and a probability of input going from zero to one $P_{0\rightarrow1}=0.5$, what is the average energy-delay product of the circuit in part (c)?

e) Determine the sizing of the two buffer stages that will minimize the average energy per transition while maintaining the propagation delay within 10% of the minimum value from part (c). For simplicity, assume that sizes are increasing in geometric fashion ($1, f, f^2$). This means that effective fanout of the first two stages (C_{in2}/C_{in} and C_{in3}/C_{in2}) is *f*, while the effective fanout of the last stage is equal to C_L/C_{in3}. What is the new average energy-delay product?

f) Find the optimum number of inverters and sizing ratio for the output load specified in Part (c). Express the optimum delay in terms of τ_{inv}. Considering your result for Part (b), do you think this inverter chain will consume more or less energy than a single inverter driving the output load?

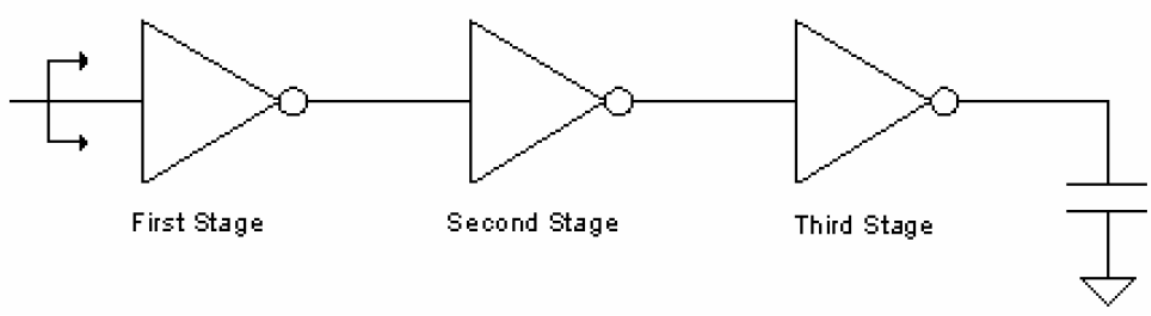
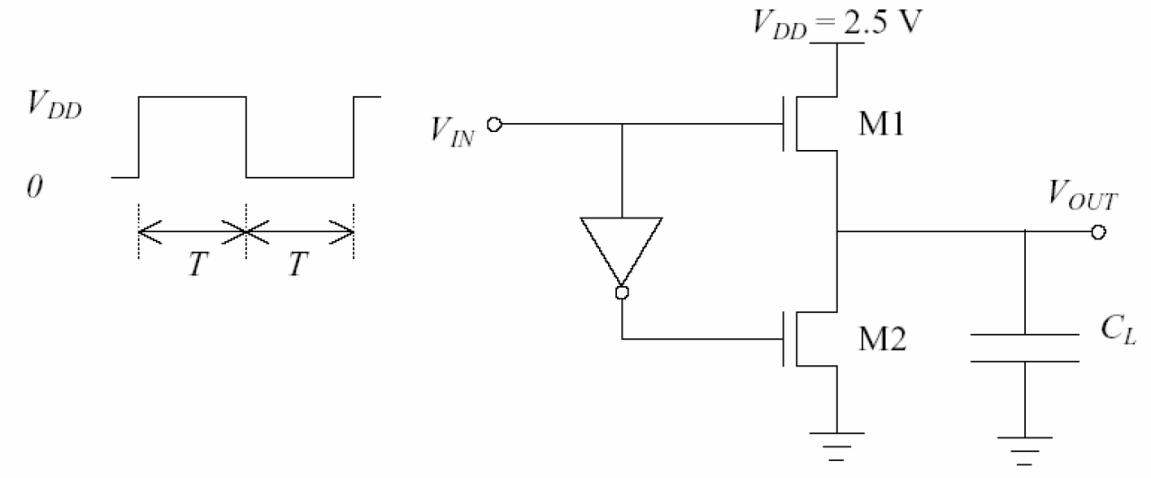


Figure 1. Buffer chain.

Problem 2 - Power Dissipation



Consider the "source follower" circuit used to drive a load C_L=50fF shown above. M_1 and M_2 are both NMOS transistors parameterized by Table 3-2 on page 103 of the text, and $2\Phi_f$= -0.6V. The inverter is a standard CMOS inverter. Assume that the input square wave edges and the inverter are fast compared to the rest of the circuit

a) Assuming that T is relatively long compared to t_{pLH} and t_{pHL}, sketch the transient waveforms of V_{IN} and V_{OUT} over a couple of cycles.

b) What is the power consumption if T=50ns? Neglect the standard inverter and assume that C_L dominates the device capacitance of M_1 and M_2.

c) Consider what happens if V_{IN} is not a square wave, but a data stream consisting of a random sequence of bits. If the bit period is 50ns and each bit has an equal chance of being 0 or 1, what is the average power consumption of the circuit?

Problem 3 - Process Scaling

A not very state-of-the-art embedded microprocessor from a company outside the valley consumes 1mW/MHz when fabricated using a 0.13 μm process. With typical standard cells (gates), the area of the processor is 2 mm^2. Assume a 1GHz clock frequency, and 1.2V power supply. Assume short channel devices, but ignore second order effects like mobility degradation, series resistance, etc. Also, ignore the leakage power (although it might be significant in real life).

a) If the supply voltage in the scaled 0.13μm processor is then reduced to 1.0V, what will the power consumption and power density be?

b) Using full scaling, what will be the area, power consumption, and power density of the original processor be if scaled to 90nm technology? Assume that the clock frequency stays at 1GHz.

c) Assuming that the processor clock speed is not limited by technology performance, but only by power consumption, how fast can the new processor powered at 1.0V be clocked without exceeding the power consumption of the original processor?