UNIVERSITY OF CALIFORNIA
College of Engineering
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Homework #5: CMOS Logic
Due Monday, November 26th, 5pm

EECS 141

Problem 1 – CMOS Gate Design and Implementation

a) Design $F = BC + AC + AB$ in combinational CMOS logic using the least number of devices. Draw the schematics and size the transistors with respect to unit width NMOS and PMOS devices so that worst case equivalent resistances are equal to those of a unit sized inverter (R_{unit}). Assuming $2k'_p = k'_n$. Which input pattern(s) would give you the worst and best equivalent pull- up or pull-down resistance (identify 4 input patterns here).

b) Draw the Logic Graphs corresponding to the circuit and identify the Euler paths.

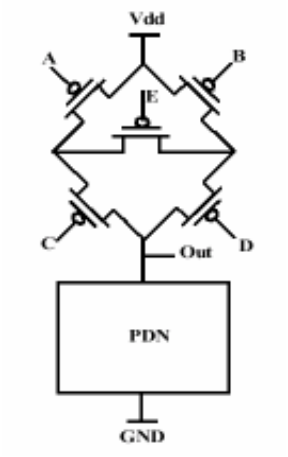
c) Using the Euler paths you found draw the stick diagram for the implementation. You don't need to distinguish different widths in the stick diagram.

Problem 2 – CMOS Logic and Euler Paths

For this problem we will use the following function: $F = (AB) \oplus [C\,(D + E)]$. (Note: $\oplus$ stands for an XOR operation). All signals and their complements are available as inputs.

a) Find a PDN configuration, which implements the function $Y = A \oplus B$ with four transistors.
b) Using the result from a), draw the CMOS logic circuit that implements the function *F*. Size it such that it has the same pull-up/pull-down strength as a minimum sized 2/1 inverter.
c) Determine the order of the input signals, which allows the largest number of diffusions to be shared. Show the signal graphs used to arrive at your solution.

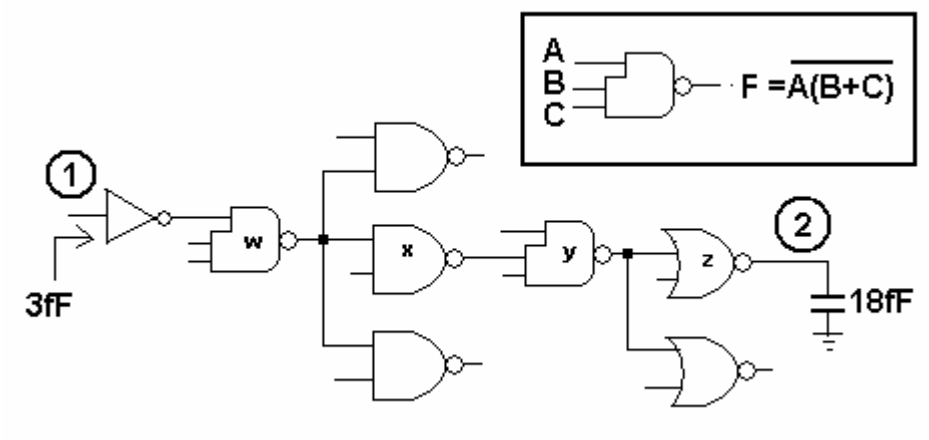
Problem 3 – CMOS Logic



Consider the CMOS logic gate given above.

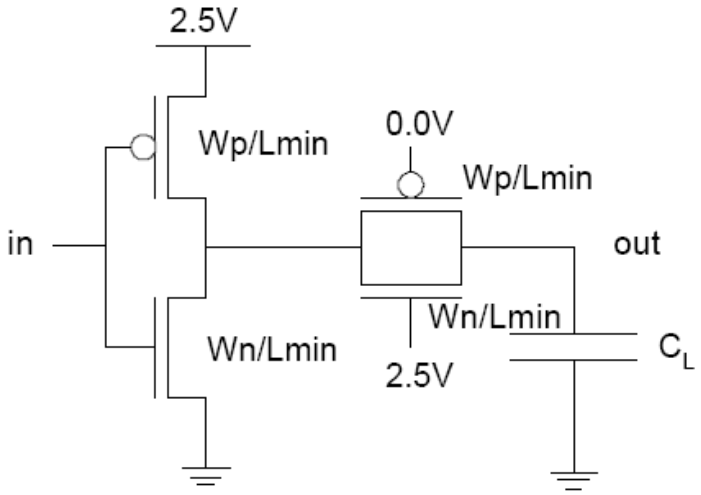
a) Determine the logic function of the gate.
b) Draw the pull-down network (ensure that you use a minimum number of transistors).

Problem 4 – Logic and Logical Effort



a) A three-input XNORT gate (see insert above) behaves like a two-input NOR as long as input A is high; otherwise, the output is stuck high. Implement the XNORT gate in complementary CMOS, and size all transistors such that the worst-case delay is equal to that of a minimum sized 2/1 inverter. Find the logical effort associated with each input.
b) Assuming all input combinations are equally likely, what is the transition activity (probability) of a XNORT gate? Averaged over many cycles, will an XNORT gate typically consume more or less power than a two-input NOR gate, if they both drive equally large output loads? What about a two-input XOR?
c) For the logic path from node (1) to node (2) shown in the figure above, find the path branching effort, path electrical effort, path logical effort, and total path effort. What is the optimum effort per stage for minimizing delay?
d) Find the input capacitances {w, x, y, z} necessary for each of the gates in the path in order to achieve the optimum effort per stage.

Problem 5 – Logical Effort of Transmission Gates



Calculate the logical effort of the circuit shown above given that $W_p = 2W_n = 2W_{min}$.