UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

	Term Project	**EECS 240**
NIKNEJAD	**Due Friday May 16, 2008**	**SPRING 2008**

Objective

You are to design a fully differential amplifier with the following specifications:

Supply, V_{DD}	1.8 V
Closed-loop gain, c	2
Dynamic range at output, DR	≥ 90 dB
Static settling error	≤ $0.5*10^{-3}$
Dynamic settling error	≤ $0.5*10^{-3}$
Settling time, t_s	≤ 50 ns
Power dissipation	Minimum
Process	EE240 0.18μm
Process corner	Nominal
Temperature	25°C

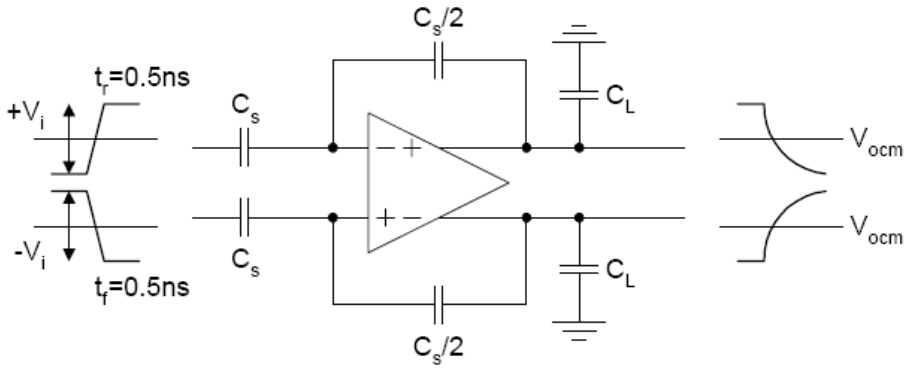

Figure 1 Conceptual diagram of amplifier configured as gain stage

The dynamic range, DR, is defined as

$$DR = 10\log\frac{P_{peak,signal}}{P_{noise}}$$

and measured at the output of the amplifier. The peak signal power, $P_{peak\text{-}signal}$, is the power of the maximum sinusoidal signal at the output that does not overload the amplifier. Note that since the feedback network attenuates the signal, this maximum cannot be achieved in a single clock cycle. The noise, P_{noise}, is the total noise at the amplifier output integrated from 10^{-6}Hz to "infinity". The justification for the upper integration limit is the presence of switches in the real circuit, which cause all noise to alias into the signal band. You

are free to choose an optimal tradeoff between signal-range and capacitor size to meet the dynamic range specification.
You must design the entire circuit including common-mode feedback circuit (but omit the switches) and biasing network with the exception of one supply independent reference current source with one terminal tied to either ground or V_{DD}. This is to keep things simple—in practice you would have to design this circuit as well. If you use a dynamic common-mode feedback circuit, you may assume it has been initialized properly prior to applying the input step to the amplifier.

Report

Document your results in a written report. It should be *concise* summary of your work and should highlight the most important features of the design. Explain clearly why you chose a particular solution over an alternative and explain how you chose key design parameters, such as device currents. *Demonstrate convincingly* how your design meets all requirements. Comment on potential weaknesses or practical problems and how you mitigate them in your design.

The following are crucial parts of the report. Do not exceed the maximum length specified in parentheses.

- (1 page) outline of your design, justifications of key design decisions, comparison with alternatives
- (1 page) schematic and table with all device sizes, g_m, I_D, V* of your final design.
- (3 pages): calculation of key design parameters including relevant transconductances, bias currents, capacitor values, signal ranges, gains to meet specifications. **This section is very important!**
- Verification. Include at least simulations suggested below. Clearly mark each page with a descriptive title, e.g. the ones used below. Perform each simulation with nominal parameters only.

    1. Openloop gain $A_{v0}=V_{od}/V_{id}$ versus V_{od}.
       Mark: A_{v0} (actual value and spec), F A_{v0} and +/- $\Delta V_{o,max}$.

    2. Stability: Bode plot of T(s) for $V_{od} = 0$ and $V_{od}= \Delta V_{o,max}$
       Mark: phase and gain margin and approximate location of doublets (if any).

    3. Step resoponse: V_{od} from 0V to $\Delta V_{o,max}$ and back to 0V.
       Mark: settling accuracy (actual and specification) at t_s=50ns.

    4. Power dissipation: use the same stimulus and initialization as above but plot the power dissipation $P=I_{DD}V_{DD}$ in µW for the amplifier and biasing network separately.
       Mark: average power dissipation of the amplifier.

    5. Noise: Integrated total noise at V_{od} for $V_{od} = 0$ and $V_{od}= \Delta V_{o,max}$ in µV (not V^2).
       Mark: total noise (actual and specification based on $\Delta V_{o,max}$).

- (1 page): Comments and conclusions

Discussion with others is encouraged (including the other engineers in the course as well as your colleagues at work), but submit a genuine design. No exchange of SPICE decks and schematics.

In an industrial design, a number of additional considerations would be important. Simulation over process, temperature, and mismatch would be required as well as a complete and careful layout. For simplicity, these steps have been omitted from the course project.