**UNIVERSITY OF CALIFORNIA**
**College of Engineering**
**Department of Electrical Engineering and Computer Sciences**

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**Spring 2007**

*Note: This is an individual assignment. For problem 1 and 2, please attach the appropriate plots from your SPICE simulations, as well as the SPICE input files.*
**Due: January 25 (Thursday) via email or post.**

## 1. SPICE models (and also to make sure your SPICE setup works)

Use the given model to characterize a 65nm CMOS process; parameter files are on the class home page.

a) Determine the threshold voltage $V_{TH}$, for the NMOS and PMOS devices (for $V_{BS} = 0$, $L = 65$nm and $W = 1\mu$m), by extrapolating from the $I_D$-$V_{GS}$ curve at low $V_{DS}$. Explain your circuit setup. How does this result compare to values reported in the model file? Also, determine the body-effect parameter.
b) Determine the subthreshold slope factor $S$ for the NMOS and PMOS devices (at $V_{DS} =$ 1.1V, room temperature). Determine the leakage currents at $V_{GS} = 0$ V. Repeat it at a lower temperature $T = 77$K. Explain your measurement setup.
c) Determine the effects of channel length $L$ on the threshold voltage $V_{TH}$ between 65nm to 1.0μm. Draw $V_{TH}$ of the NMOS and PMOS as a function of $L$ (for $V_{DS} = 1.1$ and 0.8V). Explain your measurement setup.
d) Determine the effects of drain-source voltage $V_{DS}$, on the threshold voltage $V_{TH}$ between 0 and 1.1V. Draw $V_{TH}$ as a function of $V_{DS}$ (for $L = 65$nm). Explain your measurement setup. What is the measured DIBL factor?

## 2. Technology scaling (and more SPICE review)

Explore the model for scaling a design from 130nm CMOS technology (supply 1.3V) to 90nm technology (supply 1.2V), using the two models on the class website. Starting from the 130nm technology, find out the input capacitance, intrinsic propagation delay, and active energy consumption of an inverter ($W_n = 2L_{min}$, $W_p = 2W_n$) using SPICE (<u>explain your methodology in detail</u>) and then use the generalized scaling theory to predict these parameters in the 90nm technology. Compare and comment on the results between your prediction and simulations in the 90nm technology.

## 3. CMOS scaling

Read the paper "The End of CMOS Scaling" by T. Skotnicki, et. al. Answer the following questions:

a) What is the motivation of exploring non-classical CMOS structures?
b) Write one or several sentences for each non-classical CMOS structure on its difference from the classical CMOS, its advantages and weaknesses.