

NTU 6342 / EECS 241 Homework #1 Solutions

Problem #1:

Part a: NMOS Data

The $I_D - V_{GS}$ curve was obtained by varying V_{GS} from 0 - 2 volts while holding V_{DS} constant at 0.4 volts. The results from HSPICE are then exported into MathCad and plotted below. To determine the body effect parameter, another simulation was done for a source-to-bulk voltage of 0.1 volts.

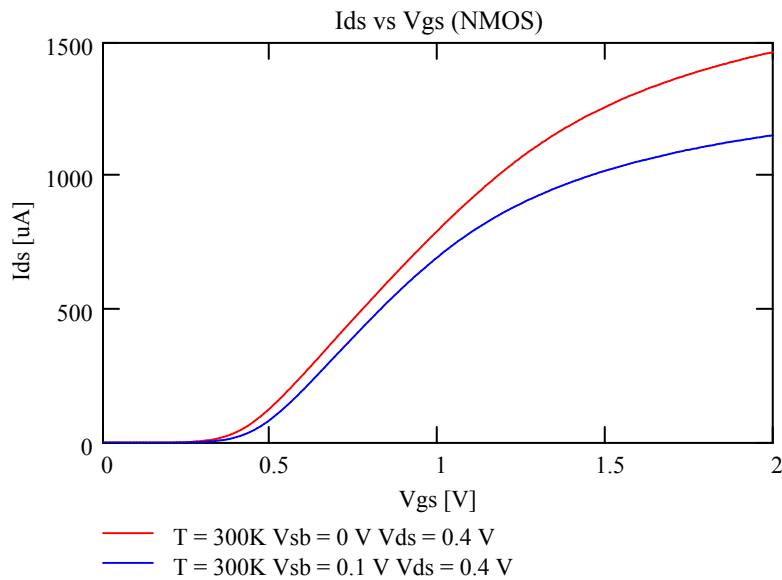
```
Parta_Data300K := READPRN("vgs_id_l=0.065u_T=300k_vds=0.4v.txt" )
```

```
Vgs_array := Parta_Data300K<0>
```

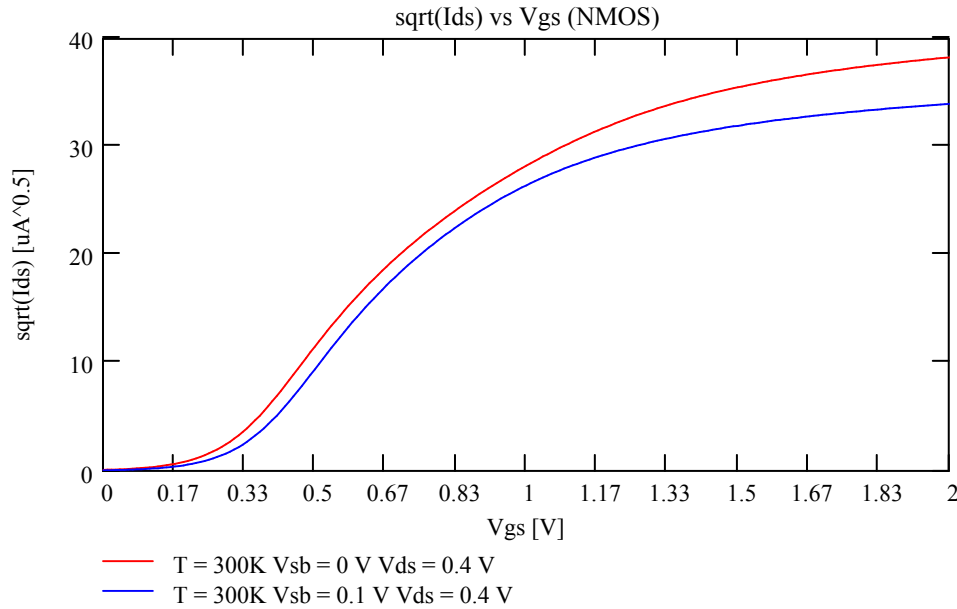
```
Ids_300 := Parta_Data300K<1>      Ids_300_body := Parta_Data300K<2>
```

```
Parta_Data77K := READPRN("vgs_id_l=0.065u_T=77k_vds=0.4v.txt" )
```

```
Ids_77 := Parta_Data77K<1>      Ids_77_body := Parta_Data77K<2>
```



To determine the threshold voltage from the simulation data, we assume that at small V_{GS} values, the current varies as $(V_{GS} - V_{th})^2$. Thus taking the square root of the data and finding the x-intercept best fit line through the linear part of this curve gives us an approximate of the device's threshold voltage.



From the graph, we use the data $500\text{mV} < V_{GS} < 600\text{mV}$. Finding the best-fit line and its x-intercept gives:

$$I_{ds_300_int} := \text{submatrix}(I_{ds_300}, 50, 60, 0, 0) \quad V_{gs_300_int} := \text{submatrix}(V_{gs_array}, 50, 60, 0, 0)$$

$$\begin{pmatrix} V_{th_300} \\ a_{300} \end{pmatrix} := \text{line}(\sqrt{I_{ds_300_int}}, V_{gs_300_int}) \quad V_{th_300} := V_{th_300} \cdot V \quad V_{th_300} = 253.221 \text{ mV}$$

From the graph, we use the data $500\text{mV} < V_{GS} < 600\text{mV}$ to find the threshold voltage of the device with a 100 mV source-to-bulk voltage.

$$I_{ds_300_body_int} := \text{submatrix}(I_{ds_300_body}, 50, 60, 0, 0) \quad V_{gs_300_body_int} := \text{submatrix}(V_{gs_array}, 50, 60, 0, 0)$$

$$\begin{pmatrix} V_{th_300_body} \\ a_{300_body} \end{pmatrix} := \text{line}(\sqrt{I_{ds_300_body_int}}, V_{gs_300_body_int})$$

$$V_{th_300_body} := V_{th_300_body} \cdot V \quad V_{th_300_body} = 306.097 \text{ mV}$$

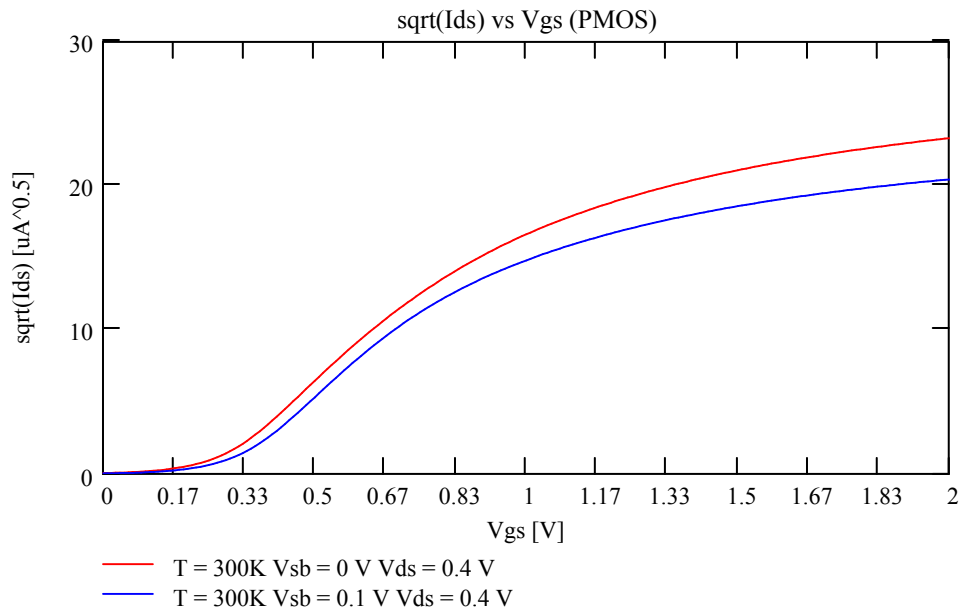
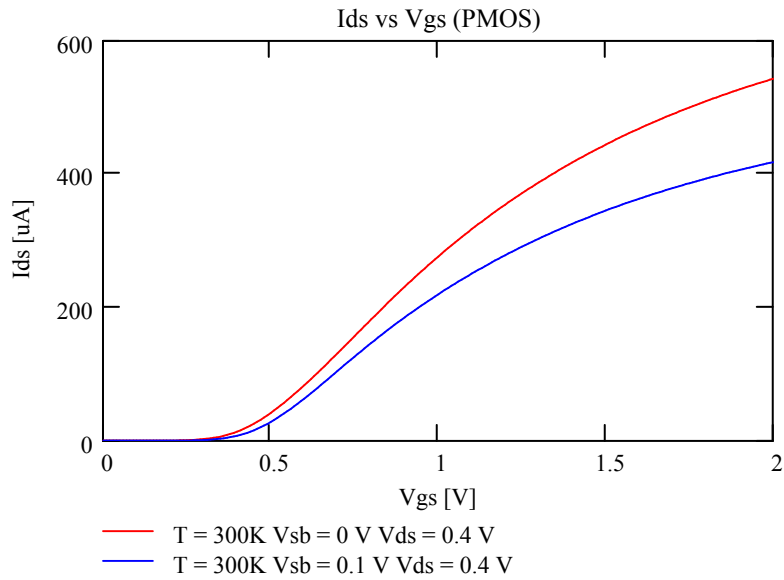
$$\phi_f := 0.3\text{V} \quad V_{sb} := 0.1\text{V}$$

$$\gamma_{300} := \frac{V_{th_300_body} - V_{th_300}}{\sqrt{|2\phi_f| + V_{sb}} - \sqrt{|2\phi_f|}} \quad \gamma_{300} = 0.852 \text{ V}^{0.5} \quad V_{th0_model} := 429\text{mV}$$

Part a: Repeating the procedure for PMOS Transistors:

$$I_{dsp_300} := \overrightarrow{\text{Parta_Data300K}^{(3)}} \quad I_{dsp_300_body} := \overrightarrow{\text{Parta_Data300K}^{(4)}}$$

$$I_{dsp_77} := \overrightarrow{\text{Parta_Data77K}^{(3)}} \quad I_{dsp_77_body} := \overrightarrow{\text{Parta_Data77K}^{(4)}}$$



From the graph, we use the data $500\text{mV} < V_{GS} < 600\text{mV}$. Finding the best-fit line and its x-intercept gives:

$$I_{dsp_300_int} := \text{submatrix}(I_{dsp_300}, 50, 60, 0, 0) \quad V_{gsp_300_int} := \text{submatrix}(V_{gs_array}, 50, 60, 0, 0)$$

$$\begin{pmatrix} V_{thp_300} \\ ap_{300} \end{pmatrix} := \text{line}(\sqrt{I_{dsp_300_int}}, V_{gsp_300_int}) \quad V_{thp_300} := V_{thp_300} \cdot V \quad V_{thp_300} = 257.315 \text{ mV}$$

From the graph, we use the data $500\text{mV} < V_{GS} < 600\text{mV}$. Finding the best-fit line and its x-intercept gives:

$$I_{dsp_300_body_int} := \text{submatrix}(I_{dsp_300_body}, 50, 60, 0, 0)$$

$$V_{gsp_300_body_int} := \text{submatrix}(V_{gs_array}, 50, 60, 0, 0)$$

$$\begin{pmatrix} V_{thp_300_body} \\ ap_{300_body} \end{pmatrix} := \text{line}(\sqrt{I_{dsp_300_body_int}}, V_{gsp_300_body_int})$$

$$V_{thp_300_body} := V_{thp_300_body} \cdot V \quad V_{thp_300_body} = 298.545 \text{ mV}$$

$$\phi_f := 0.3\text{V} \quad V_{sb} := 0.1\text{V}$$

$$\gamma_{p300} := \frac{V_{thp_300_body} - V_{thp_300}}{\sqrt{|2\phi_f| + V_{sb}} - \sqrt{|2\phi_f|}} \quad \gamma_{p300} = 0.664 \text{ V}^{0.5} \quad V_{th0_model} := 378\text{mV}$$

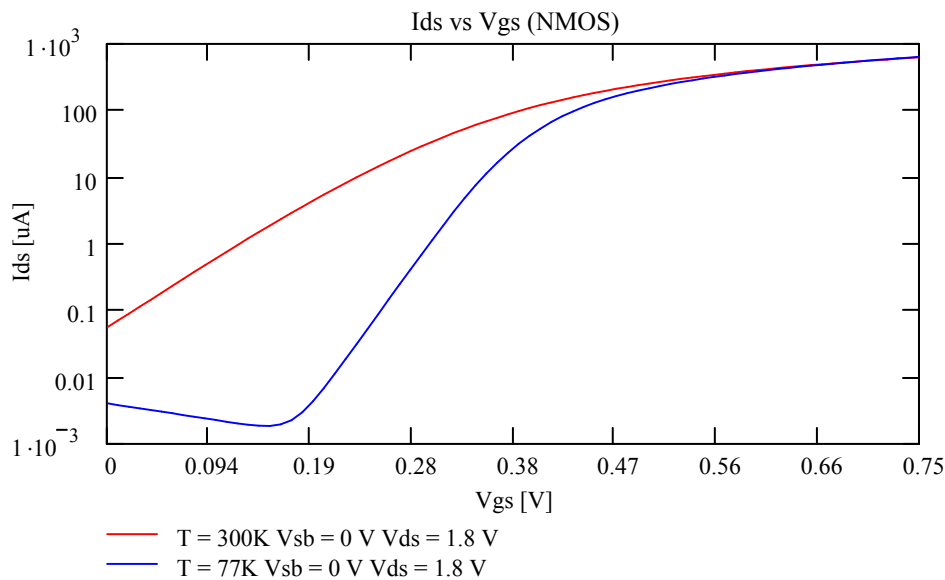
Part b: NMOS Data

To determine the subthreshold slope, we repeat the simulation in Part a, but with a V_{DS} of 1.1 volts and at two temperatures, 300K and 77K. The data is then plotted on a log scale, and shown here for $0 < V_{GS} < 0.75V$. The slope of these curves are then determined.

```
Partb_Data300K := READPRN("vgs_id_l=0.065u_T=300k_vds=1.1v.txt")
```

```
Vgs_array := Partb_Data300K<0> Ids1 := Partb_Data300K<1>
```

```
Partb_Data77K := READPRN("vgs_id_l=0.065u_T=77k_vds=1.1v.txt") Ids2 := Partb_Data77K<1>
```



From the graph, we use the data $100\text{mV} < V_{GS} < 300\text{mV}$ for $T = 300\text{K}$.

```
Ids1_int := submatrix(Ids1, 10, 30, 0, 0)
```

```
Vgs1_int := submatrix(Vgs_array, 10, 30, 0, 0)
```

$$\begin{pmatrix} a_1 \\ b_1 \\ c_1 \end{pmatrix} := \text{expfit}(V_{gs1_int}, I_{ds1_int}) \quad T_1 := 300\text{K} \quad q := 1.602 \cdot 10^{-19}\text{C} \quad k := 1.38 \cdot 10^{-23} \frac{\text{J}}{\text{K}}$$

$$V_{T1} := \frac{k \cdot T_1}{q} \quad V_{T1} = 25.843 \text{ mV} \quad b_1 := \frac{b_1}{V} \quad a_1 := a_1 \cdot A \quad c_1 := c_1 \cdot A$$

$$S_{300} := \frac{\ln(10)}{b_1} \quad S_{300} = 137.157 \frac{\text{mV}}{\text{decade}}$$

The drain current at zero gate-to-source voltage is:

$$I_{ds1} := I_{ds1} \cdot A \quad I_{ds1_0} = 56.38 \text{ nA}$$

For $T = 77\text{K}$, we use the data from $200\text{mV} < V_{\text{GS}} < 300\text{mV}$.

$$I_{\text{ds2_int}} := \text{submatrix}(I_{\text{ds2}}, 20, 30, 0, 0)$$

$$V_{\text{gs2_int}} := \text{submatrix}(V_{\text{gs_array}}, 20, 30, 0, 0)$$

$$\begin{pmatrix} a_2 \\ b_2 \\ c_2 \end{pmatrix} := \text{expfit}(V_{\text{gs2_int}}, I_{\text{ds2_int}}) \quad T_2 := 77\text{K}$$

$$V_{\text{T2}} := \frac{k \cdot T_2}{q}$$

$$V_{\text{T2}} = 6.633 \text{ mV}$$

$$b_2 := \frac{b_2}{\text{V}}$$

$$S_{77} := \frac{\ln(10)}{b_2}$$

$$S_{77} = 45.346 \frac{\text{mV}}{\text{decade}}$$

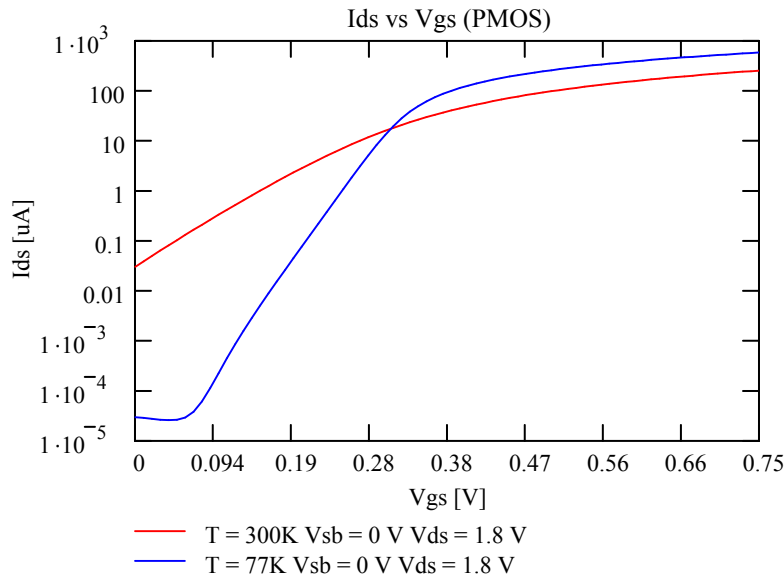
The drain current at zero gate-to-source voltage is:

$$I_{\text{ds2}} := I_{\text{ds2}} \cdot \text{A}$$

$$I_{\text{ds2}_0} = 4.029 \text{ nA}$$

Part b: Repeating the procedure for PMOS Transistors:

$$I_{dsp1} := \overrightarrow{\text{Partb_Data300K}^{(3)}} \quad I_{dsp2} := \overrightarrow{\text{Partb_Data77K}^{(3)}}$$



From the graph, we use the data $100\text{mV} < V_{GS} < 300\text{mV}$ for $T = 300\text{K}$.

$$I_{dsp1_int} := \text{submatrix}(I_{dsp1}, 10, 30, 0, 0) \quad V_{gsp1_int} := \text{submatrix}(V_{gs_array}, 10, 30, 0, 0)$$

$$\begin{pmatrix} a_{p1} \\ b_{p1} \\ c_{p1} \end{pmatrix} := \text{expfit}(V_{gsp1_int}, I_{dsp1_int}) \quad b_{p1} := \frac{b_{p1}}{V}$$

The slope factor and the zero-gate-to-source current is found as:

$$S_{p300} := \frac{\ln(10)}{b_{p1}} \quad S_{p300} = 149.37 \frac{\text{mV}}{\text{decade}} \quad I_{dsp1} := I_{dsp1} \cdot A \quad I_{dsp1_0} = 30.3 \text{ nA}$$

For $T = 77\text{K}$, we use the data from $100\text{mV} < V_{GS} < 200\text{mV}$.

$$I_{dsp2_int} := \text{submatrix}(I_{dsp2}, 10, 20, 0, 0) \quad V_{gsp2_int} := \text{submatrix}(V_{gs_array}, 10, 20, 0, 0)$$

$$\begin{pmatrix} a_{p2} \\ b_{p2} \\ c_{p2} \end{pmatrix} := \text{expfit}(V_{gsp2_int}, I_{dsp2_int}) \quad b_{p2} := \frac{b_{p2}}{V} \quad V_{T2} = 6.633 \text{ mV}$$

The slope factor and the zero-gate-to-source current is found as:

$$S_{p77} := \frac{\ln(10)}{b_{p2}} \quad S_{p77} = 43.143 \frac{\text{mV}}{\text{decade}} \quad I_{dsp2} := I_{dsp2} \cdot A \quad I_{dsp2_0} = 29.74 \text{ pA}$$

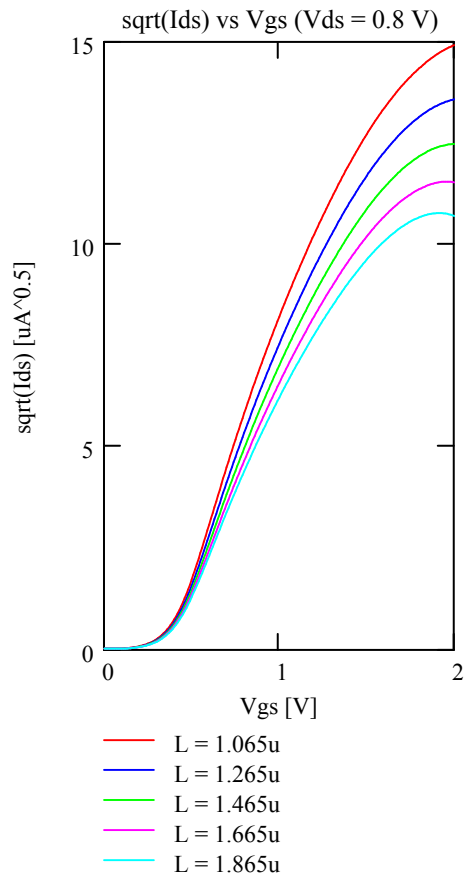
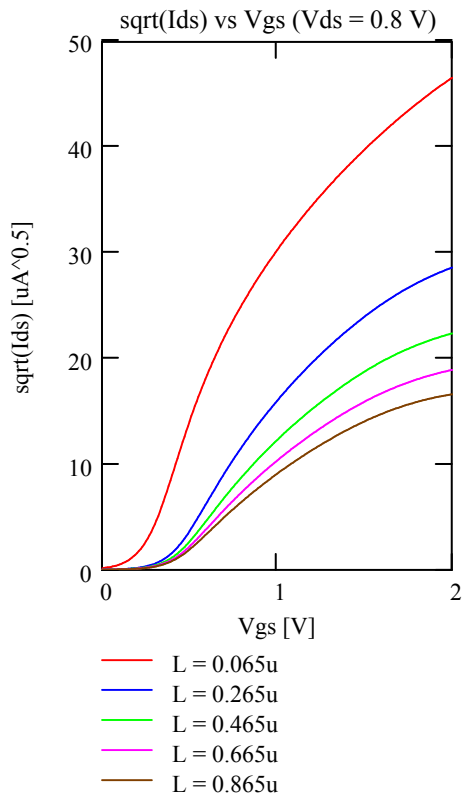
$I_{ds_08v_0} := \text{READPRN}(\text{"vgs_id_l=0.065u_T=300k_vds=0.8v.txt"}) \langle 1 \rangle$
 $I_{ds_08v_1} := \text{READPRN}(\text{"vgs_id_l=0.265u_T=300k_vds=0.8v.txt"}) \langle 1 \rangle$
 $I_{ds_08v_2} := \text{READPRN}(\text{"vgs_id_l=0.465u_T=300k_vds=0.8v.txt"}) \langle 1 \rangle$
 $I_{ds_08v_3} := \text{READPRN}(\text{"vgs_id_l=0.665u_T=300k_vds=0.8v.txt"}) \langle 1 \rangle$
 $I_{ds_08v_4} := \text{READPRN}(\text{"vgs_id_l=0.865u_T=300k_vds=0.8v.txt"}) \langle 1 \rangle$
 $I_{ds_08v_5} := \text{READPRN}(\text{"vgs_id_l=1.065u_T=300k_vds=0.8v.txt"}) \langle 1 \rangle$
 $I_{ds_08v_6} := \text{READPRN}(\text{"vgs_id_l=1.265u_T=300k_vds=0.8v.txt"}) \langle 1 \rangle$
 $I_{ds_08v_7} := \text{READPRN}(\text{"vgs_id_l=1.465u_T=300k_vds=0.8v.txt"}) \langle 1 \rangle$
 $I_{ds_08v_8} := \text{READPRN}(\text{"vgs_id_l=1.665u_T=300k_vds=0.8v.txt"}) \langle 1 \rangle$
 $I_{ds_08v_9} := \text{READPRN}(\text{"vgs_id_l=1.865u_T=300k_vds=0.8v.txt"}) \langle 1 \rangle$

$I_{ds_11v_0} := \text{READPRN}(\text{"vgs_id_l=0.065u_T=300k_vds=1.1v.txt"}) \langle 1 \rangle$
 $I_{ds_11v_1} := \text{READPRN}(\text{"vgs_id_l=0.265u_T=300k_vds=1.1v.txt"}) \langle 1 \rangle$
 $I_{ds_11v_2} := \text{READPRN}(\text{"vgs_id_l=0.465u_T=300k_vds=1.1v.txt"}) \langle 1 \rangle$
 $I_{ds_11v_3} := \text{READPRN}(\text{"vgs_id_l=0.665u_T=300k_vds=1.1v.txt"}) \langle 1 \rangle$
 $I_{ds_11v_4} := \text{READPRN}(\text{"vgs_id_l=0.865u_T=300k_vds=1.1v.txt"}) \langle 1 \rangle$
 $I_{ds_11v_5} := \text{READPRN}(\text{"vgs_id_l=1.065u_T=300k_vds=1.1v.txt"}) \langle 1 \rangle$
 $I_{ds_11v_6} := \text{READPRN}(\text{"vgs_id_l=1.265u_T=300k_vds=1.1v.txt"}) \langle 1 \rangle$
 $I_{ds_11v_7} := \text{READPRN}(\text{"vgs_id_l=1.465u_T=300k_vds=1.1v.txt"}) \langle 1 \rangle$
 $I_{ds_11v_8} := \text{READPRN}(\text{"vgs_id_l=1.665u_T=300k_vds=1.1v.txt"}) \langle 1 \rangle$
 $I_{ds_11v_9} := \text{READPRN}(\text{"vgs_id_l=1.865u_T=300k_vds=1.1v.txt"}) \langle 1 \rangle$

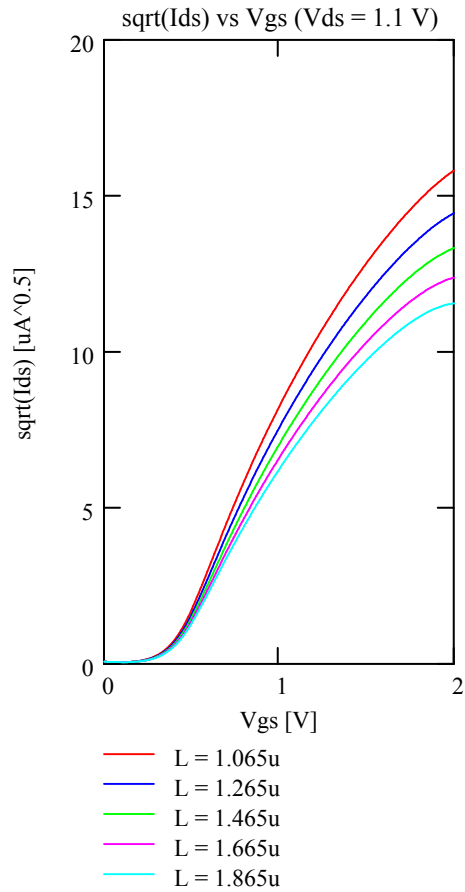
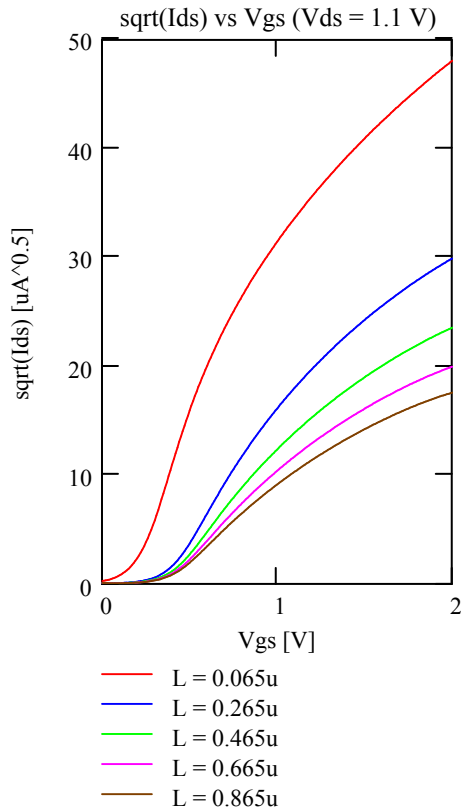
$$\begin{aligned}
I_{\text{dsp_08v}_0} &:= \overrightarrow{\text{READPRN("vgs_id_l=0.065u_T=300k_vds=0.8v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_08v}_1} &:= \overrightarrow{\text{READPRN("vgs_id_l=0.265u_T=300k_vds=0.8v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_08v}_2} &:= \overrightarrow{\text{READPRN("vgs_id_l=0.465u_T=300k_vds=0.8v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_08v}_3} &:= \overrightarrow{\text{READPRN("vgs_id_l=0.665u_T=300k_vds=0.8v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_08v}_4} &:= \overrightarrow{\text{READPRN("vgs_id_l=0.865u_T=300k_vds=0.8v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_08v}_5} &:= \overrightarrow{\text{READPRN("vgs_id_l=1.065u_T=300k_vds=0.8v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_08v}_6} &:= \overrightarrow{\text{READPRN("vgs_id_l=1.265u_T=300k_vds=0.8v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_08v}_7} &:= \overrightarrow{\text{READPRN("vgs_id_l=1.465u_T=300k_vds=0.8v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_08v}_8} &:= \overrightarrow{\text{READPRN("vgs_id_l=1.665u_T=300k_vds=0.8v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_08v}_9} &:= \overrightarrow{\text{READPRN("vgs_id_l=1.865u_T=300k_vds=0.8v.txt")}} \langle 3 \rangle
\end{aligned}$$

$$\begin{aligned}
I_{\text{dsp_11v}_0} &:= \overrightarrow{\text{READPRN("vgs_id_l=0.065u_T=300k_vds=1.1v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_11v}_1} &:= \overrightarrow{\text{READPRN("vgs_id_l=0.265u_T=300k_vds=1.1v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_11v}_2} &:= \overrightarrow{\text{READPRN("vgs_id_l=0.465u_T=300k_vds=1.1v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_11v}_3} &:= \overrightarrow{\text{READPRN("vgs_id_l=0.665u_T=300k_vds=1.1v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_11v}_4} &:= \overrightarrow{\text{READPRN("vgs_id_l=0.865u_T=300k_vds=1.1v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_11v}_5} &:= \overrightarrow{\text{READPRN("vgs_id_l=1.065u_T=300k_vds=1.1v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_11v}_6} &:= \overrightarrow{\text{READPRN("vgs_id_l=1.265u_T=300k_vds=1.1v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_11v}_7} &:= \overrightarrow{\text{READPRN("vgs_id_l=1.465u_T=300k_vds=1.1v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_11v}_8} &:= \overrightarrow{\text{READPRN("vgs_id_l=1.665u_T=300k_vds=1.1v.txt")}} \langle 3 \rangle \\
I_{\text{dsp_11v}_9} &:= \overrightarrow{\text{READPRN("vgs_id_l=1.865u_T=300k_vds=1.1v.txt")}} \langle 3 \rangle
\end{aligned}$$

Part c: To find the effects of the threshold voltage to channel length, we repeat the simulations done in Part a with varying channel lengths, for a V_{DS} of 1.8 volts and 1.2 volts.



```
LengthArray := | x0 ← 0.065μm  
                | for i ∈ 1..9  
                |   xi ← xi-1 + 0.2μm  
                | x
```



Performing the extrapolation for all the curves:

$$V_{th_08v} := \begin{cases} \text{for } i \in 0..9 \\ \begin{pmatrix} x_i \\ y_i \end{pmatrix} \leftarrow \text{line}\left(\sqrt{\text{submatrix}(I_{ds_08v_i}, 50, 60, 0, 0)}, \text{submatrix}(V_{gs_array}, 50, 60, 0, 0)\right) \\ x \end{cases}$$

$$V_{th_11v} := \begin{cases} \text{for } i \in 0..9 \\ \begin{pmatrix} x_i \\ y_i \end{pmatrix} \leftarrow \text{line}\left(\sqrt{\text{submatrix}(I_{ds_11v_i}, 50, 60, 0, 0)}, \text{submatrix}(V_{gs_array}, 50, 60, 0, 0)\right) \\ x \end{cases}$$

And comparing this with the threshold voltage reported by HSPICE:

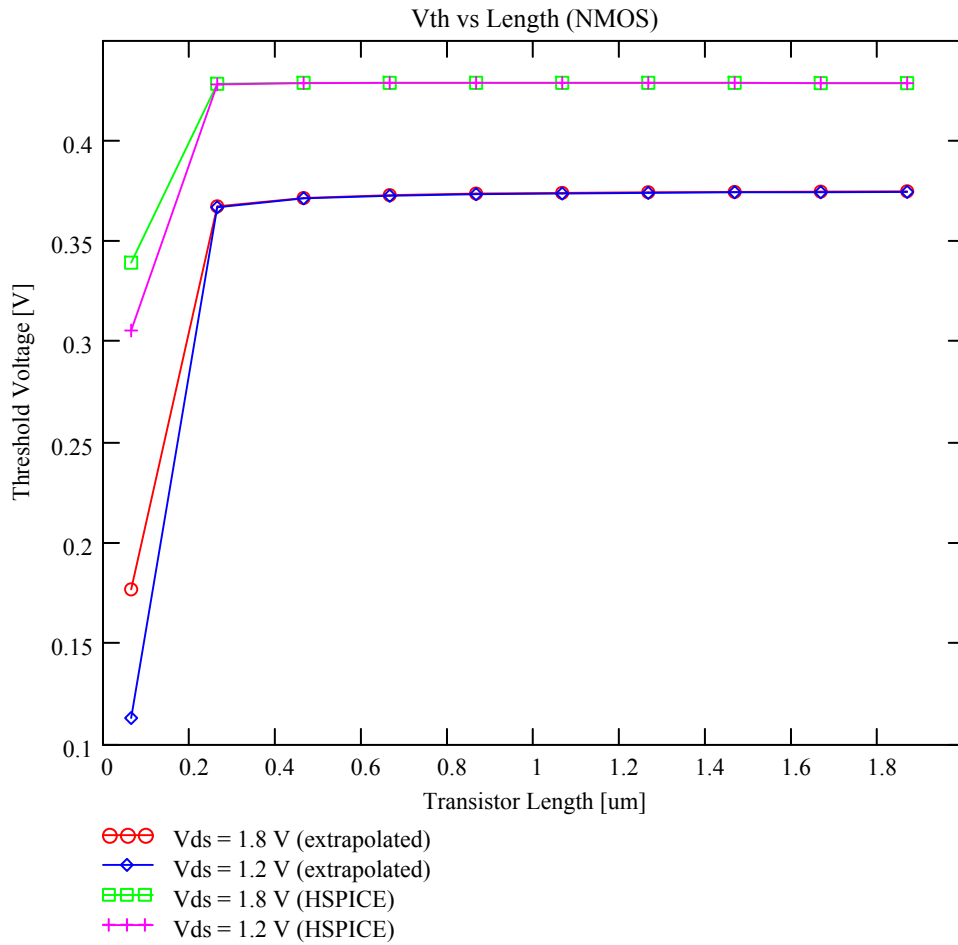
VthHspiceData18v := READPRN("vth_vgs=1.1_vds=0.8v.txt")

VthHspiceData12v := READPRN("vth_vgs=1.1_vds=1.1v.txt")

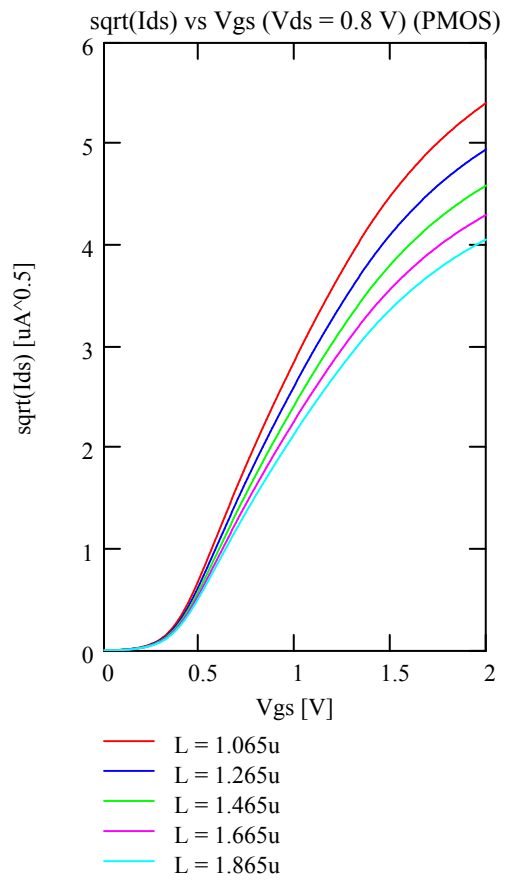
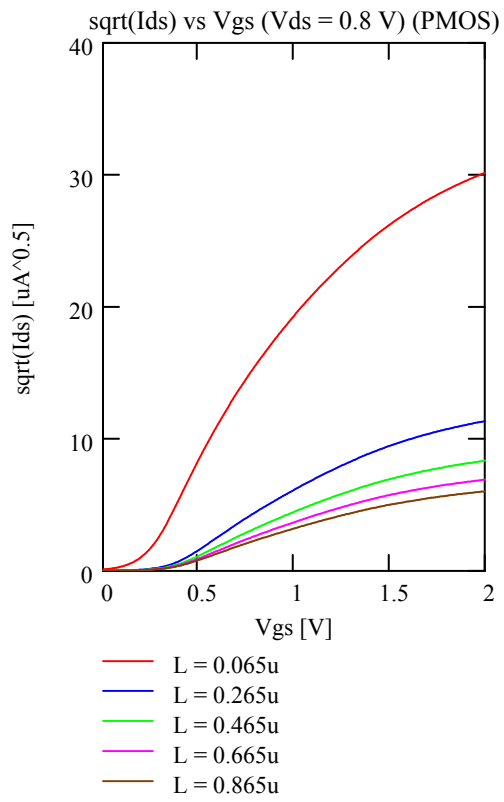
Vth_hspice_18v := VthHspiceData18v^{<1>}

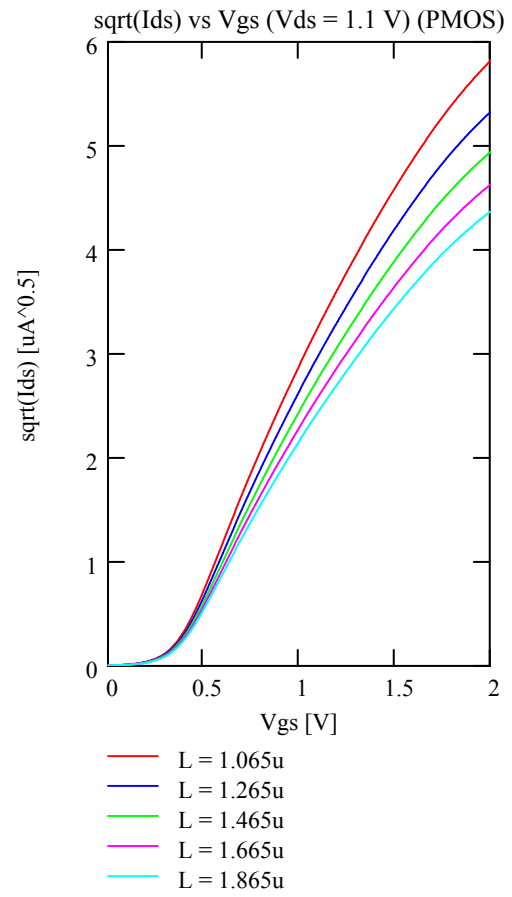
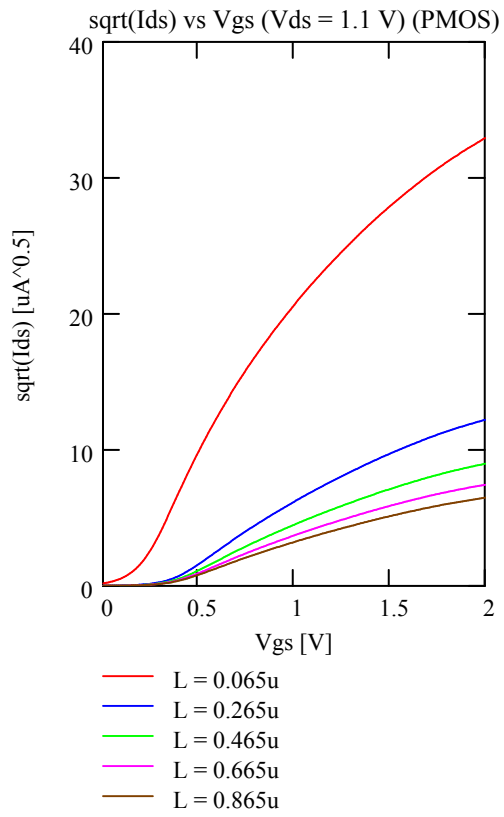
Vth_hspice_12v := VthHspiceData12v^{<1>}

We would get the following graph showing the interpolated values and the values reported by HSPICE obtained by sweeping the transistor channel lengths from 0.18 microns to 2 microns.



Part c: Repeat the procedure for PMOS transistors:





Extrapolating the curves to find the threshold voltages:

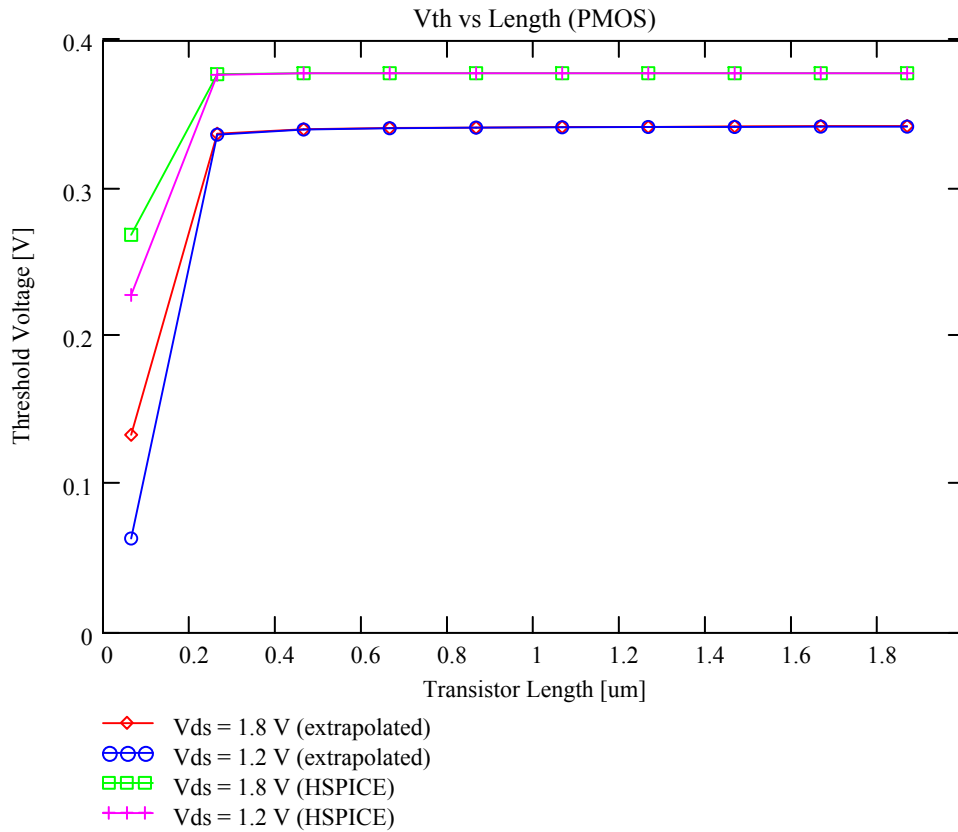
$$V_{thp_18v} := \left| \begin{array}{l} \text{for } i \in 0..9 \\ \left(\begin{array}{l} x_i \\ y_i \end{array} \right) \leftarrow \text{line} \left(\sqrt{\text{submatrix} \left(I_{dsp_08v_1}, 60, 70, 0, 0 \right)}, \text{submatrix} \left(V_{gs_array}, 60, 70, 0, 0 \right) \right) \\ x \end{array} \right.$$

$$V_{thp_12v} := \left| \begin{array}{l} \text{for } i \in 0..9 \\ \left(\begin{array}{l} x_i \\ y_i \end{array} \right) \leftarrow \text{line} \left(\sqrt{\text{submatrix} \left(I_{dsp_11v_1}, 60, 70, 0, 0 \right)}, \text{submatrix} \left(V_{gs_array}, 60, 70, 0, 0 \right) \right) \\ x \end{array} \right.$$

And obtaining the threshold voltage data from HSPICE:

$$V_{thp_hspice_18v} := V_{thHspiceData18v} \langle 3 \rangle$$

$$V_{thp_hspice_12v} := V_{thHspiceData12v} \langle 3 \rangle$$

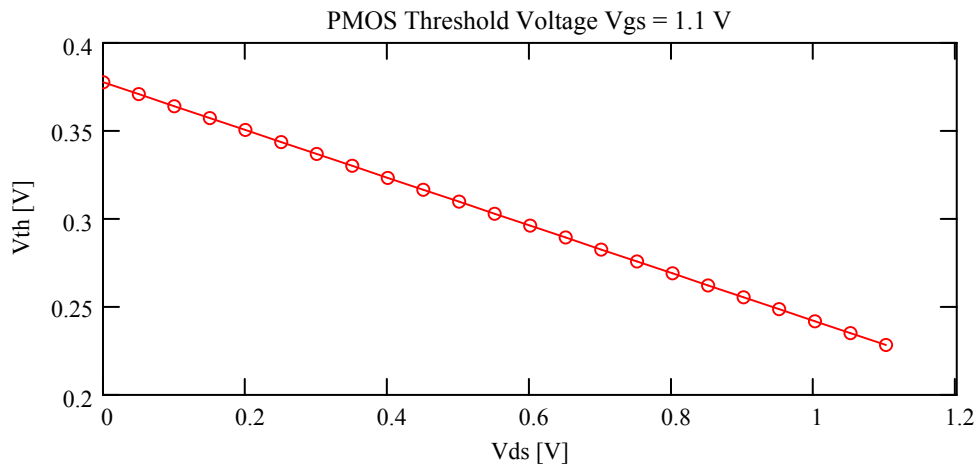
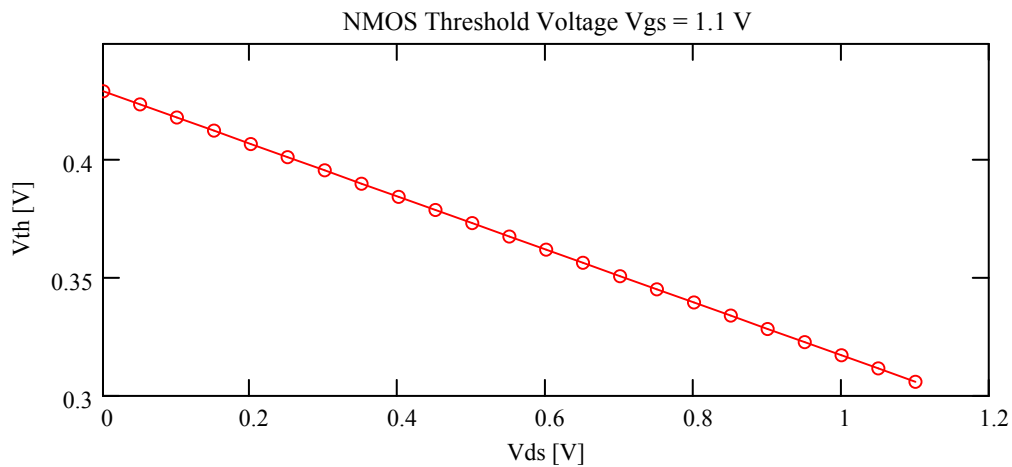


Part d: To determine the effect of the drain-to-source voltage on the threshold voltage, simulations were carried out where the V_{DS} is swept from 0 - 1.1 volts while holding V_{GS} constant at 1.1 volt. Plotted below is the NMOS and PMOS threshold voltage data reported by HSPICE.

```
DIBLData := READPRN("dibl_data.txt")
```

```
VdsArray := DIBLData<0> V      Vthn := DIBLData<1> V      Vthn_body := DIBLData<2> V
```

```
Vthp := DIBLData<3> V      Vthp_body := DIBLData<4> V
```



Computing the slopes to get the DIBL factor yields:

$$\xi_{nmos} := \text{slope}(V_{dsArray}, V_{thn}) \quad \xi_{nmos} = -0.113$$

$$\xi_{pmos} := \text{slope}(V_{dsArray}, V_{thp}) \quad \xi_{pmos} = -0.136$$

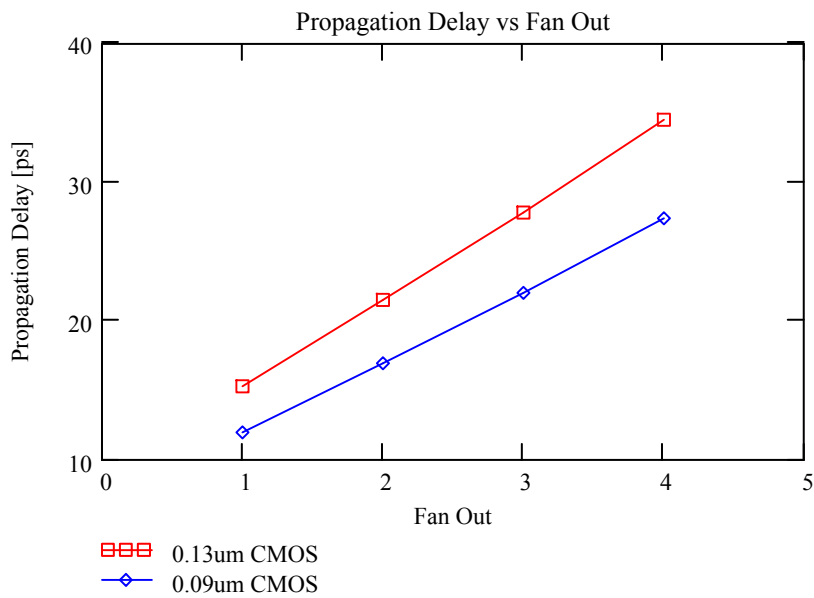
Problem #2:

HSPICE simulations were performed for inverters with fan-outs of 1, 2, 3 and 4. Propagation data is shown below.

FanoutData013 := READPRN("inverter_delay_013.txt")

FanoutData009 := READPRN("inverter_delay_009.txt")

FanOut := FanoutData013^{<0>} t_{p_013} := FanoutData013^{<3>} s t_{p_009} := FanoutData009^{<3>} s



We can use this data to determine the inverter's intrinsic delay as well as their C_{out} to C_{gate} ratio (γ).

$$t_{po_013} := \text{intercept}(\text{FanOut}, t_{p_013}) \qquad t_{po_013} = 8.809 \text{ ps}$$

$$t_{po_009} := \text{intercept}(\text{FanOut}, t_{p_009}) \qquad t_{po_009} = 6.752 \text{ ps}$$

$$\gamma_{013} := \frac{t_{po_013}}{\text{slope}(\text{FanOut}, t_{p_013})} \qquad \gamma_{013} = 1.377$$

$$\gamma_{009} := \frac{t_{po_009}}{\text{slope}(\text{FanOut}, t_{p_009})} \qquad \gamma_{009} = 1.314$$

$$\gamma_0 := \gamma_{013} \qquad \gamma_1 := \gamma_{009} \qquad V_{dd_0} := 1.3V \qquad V_{dd_1} := 1.2V$$

The inverters are then simulated in a 5-stage ring oscillator circuit and their delay, power and oscillation frequency are obtained.:

RingOscData := READPRN("ring_data.txt")

LengthArray := RingOscData^{<0>} m RingDelay := RingOscData^{<1>} s
 InvDelay := RingOscData^{<2>} s OscFreq := RingOscData^{<3>} Hz
 I_{supply_rms} := RingOscData^{<4>} A InvPower := RingOscData^{<5>} W

Comparing the obtained ring oscillator data to the fan-out data:

$$\text{InvDelay} = \begin{pmatrix} 19.807 \\ 24.607 \end{pmatrix} \text{ps} \quad t_{p_009_0} = 11.98 \text{ps} \quad t_{p_013_0} = 15.303 \text{ps}$$

From the obtained HSPICE data, we can also compute the energy needed by each inverter in one cycle:

$$\text{InvPower} = \begin{pmatrix} 29.009 \\ 43.363 \end{pmatrix} \mu\text{W} \quad \text{LengthArray} = \begin{pmatrix} 0.09 \\ 0.13 \end{pmatrix} \mu\text{m} \quad V_{\text{dd}} = \begin{pmatrix} 1.3 \\ 1.2 \end{pmatrix} \text{V}$$

$$\text{OscFreq} = \begin{pmatrix} 10.097 \\ 8.128 \end{pmatrix} \text{GHz} \quad \text{InvEnergyPerCycle} := \overrightarrow{\left(\text{InvPower} \cdot \frac{1}{\text{OscFreq}} \right)}$$

$$\text{InvEnergyPerCycle} = \begin{pmatrix} 2.873 \\ 5.335 \end{pmatrix} \text{fJ}$$

Using the γ data obtained from the fan-out simulations, we can calculate the input (gate) capacitance of the inverter:

$$C_{\text{gate}} := \begin{array}{l} \text{for } i \in 0..1 \\ x_1 \leftarrow \frac{\text{InvPower}_i}{(V_{\text{dd}_i})^2 \cdot \text{OscFreq}_i} \cdot \frac{1}{(1 + \gamma_i)} \\ x \end{array} \quad C_{\text{gate}} = \begin{pmatrix} 0.715 \\ 1.601 \end{pmatrix} \text{fF}$$

Values Predicted by Scaling (General Scaling):

$$S := \frac{0.13 \mu\text{m}}{0.09 \mu\text{m}} \quad U := \frac{1.3 \text{V}}{1.2 \text{V}} \quad S = 1.444 \quad U = 1.083$$

$$C_{\text{predicted}} := \frac{C_{\text{gate}_1}}{S} \quad t_{p_predicted} := \frac{\text{InvDelay}_1}{S} \quad E_{\text{predicted}} := \frac{\text{InvEnergyPerCycle}_1}{S \cdot U^2}$$

Predicted versus simulated values:

$$C_{\text{predicted}} = 1.108 \text{ fF}$$

$$C_{\text{gate}_0} = 0.715 \text{ fF}$$

$$t_{\text{p_predicted}} = 17.036 \text{ ps}$$

$$\text{InvDelay}_0 = 19.807 \text{ ps}$$

$$E_{\text{predicted}} = 3.147 \text{ fJ}$$

$$\text{InvEnergyPerCycle}_0 = 2.873 \text{ fJ}$$

We can see from the results above that the predicted values are somewhat better than the values obtained from the simulations.

$$1 - \frac{C_{\text{predicted}}}{C_{\text{gate}_0}} = -54.997\% \quad 1 - \frac{t_{\text{p_predicted}}}{\text{InvDelay}_0} = 13.992\% \quad 1 - \frac{E_{\text{predicted}}}{\text{InvEnergyPerCycle}_0} = -9.542\%$$

$$t_{\text{ox}_0} := 5.7 \cdot \text{nm} \quad t_{\text{ox}_1} := 7.7 \cdot \text{nm} \quad \frac{t_{\text{ox}_1}}{t_{\text{ox}_0}} = 1.351$$

We can see from the oxide thickness obtained from the device models are not exactly scaled as the feature size. This could account for some of the differences between the predicted and actual values.

Problem #3:

Part a: Motivation for Non-Classical CMOS Structures:

Physical and manufacturing limits are making it more difficult to scale bulk CMOS further in order to meet the projected industry performance increase requirement of 17% per year. Thus, non-classical CMOS structures are being studied as candidates to replace bulk CMOS in order to meet these requirements.

Part b: Non-Classical CMOS Structures:

Transport Enhanced MOSFETs (Strained Channel):

This structure uses mechanically strained channel to enhance carrier mobility and velocity at the expense of higher manufacturing costs.

Fully Depleted SOI:

This structure has a thin body that is fully depleted, allowing strong turn-off, immunity to threshold voltage variations and higher drive currents due to enhanced carrier mobilities at the expense of tighter manufacturing tolerances.

Ultra Thin Channel and Localized BOX:

A localized ultra thin buried oxide isolates the channel from the bulk giving the advantages of SOI (strong turn-off, better threshold voltage variation immunity and higher carrier mobilities) in addition to deep source and drain regions for low parasitic resistances. The deep S/D regions and thin BOX increases capacitive coupling between the bulk and the channel/S/D regions that may potentially decrease speed.

Schottky Source/Drain:

Schottky contacts (metal-semiconductor contacts in place of shallow p-n junctions) reduce the parasitic resistance in the S/D regions. This structure however needs proper materials to form the schottky junction and UTB is needed to control leakage.

Non-overlapped Source/Drain:

By not overlapping the gate with the source and drain regions, this structure minimizes overlap capacitance, and is thus faster. Also, this structure shows less SCE and DIBL effects due to its longer effective channel length at the expense of higher S/D resistance.

N-Gate Structures:

The following structures have multiple gate surfaces effectively creating a 2 or 3 dimensional gate surface for better on and off control of the channel, and also allowing for thicker bodies.

MG Tied Gate Sidewall Conduction:

This structure has thin vertical fins (thinner than the channel length, and therefore could be harder to manufacture) that can provide adequate control of short channel effects. This structure can be implemented in bulk silicon substrates.

MG Tied Gate Planar:

This structure has gate electrodes at the top and bottom of the channel, can be fabricated in a simple process, and uses the same layout as bulk CMOS. In addition, the channel thickness is controlled by epitaxy instead of etching, allowing better control. Limited by widths of less than 1 micron.

MG Double Gate Planar:

This structure has two gates, one gate can be used for on/off control and one gate for threshold voltage adjustment. This can lead to improved short channel effects. The second gate however adds additional capacitance and adds wiring complexity.

MG Double Gate Vertical:

Since the conduction path from S to D is vertical, this structure's channel length depends on epitaxy rather than lithography allowing very short and well controlled (limited to unit-sized) channels.