UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

Jan M. Rabaey **Homework 2** **NTU 6342 / EECS 241**
Spring 2007

Note: This is an individual assignment. For problem 1, please attach zoom-in plots from SPICE simulation, as well as the SPICE input files.
Due: February 16 (Friday) via email or post.

1. Cell Library Design

The AOI4 gate is a complex gate that finds wide use in today's standard cell library. Its functionality is defined by Z = -(AB + CD).

a. Design such a gate in static 65nm CMOS. Device sizes will be Wn/Ln = 0.18μm/65nm,Wp/Lp = 0.36μm/65nm. Measure the energy, delay and energy-delay product. The cell inputs should be driven by unit inverters, the cell output should be loaded with 4 unit inverters to suppress overshoot.
b. Redesign the same gate using DCVSL. Use the Karnaugh map technique to synthesize the complementary pull down networks, for which you will use NMOS devices sized as Wn/Ln = 0.18μm/65nm. Sweep the width of the PMOS cross-coupled load and plot delay, energy and energy-delay. What is the optimal width value from an energy perspective? What about energy-delay?
c. Repeat part 2, but instead of using a cross-coupled load, put an inverter at the end of each chain, followed by a keeper with the gate tied to the inverter output.

2. Pulsed Static CMOS

a. Design a two-input XOR gate using the PS-CMOS logic style
b. Size the gate for optimum performance using logical effort analysis. Assume that each device within a NAND or NOR gate has the same size.

3. Pass Transistor Logic

Consider the circuit shown in Figure 1. Assume $V_{Tn} = |V_{Tp}| = 300mV$.

a. Derive the minimum supply such that the circuit is still operational
b. Determine the critical path, and give an expression for its delay.
c. Discuss power dissipation of this circuit. Is there a problem?
d. Propose two circuit modifications to improve the performance and power dissipation of the circuit, and discuss the pros and cons of each of them.
e. What are the impacts on the performance and power consumption of this circuit if the threshold voltage of this process is lowered?

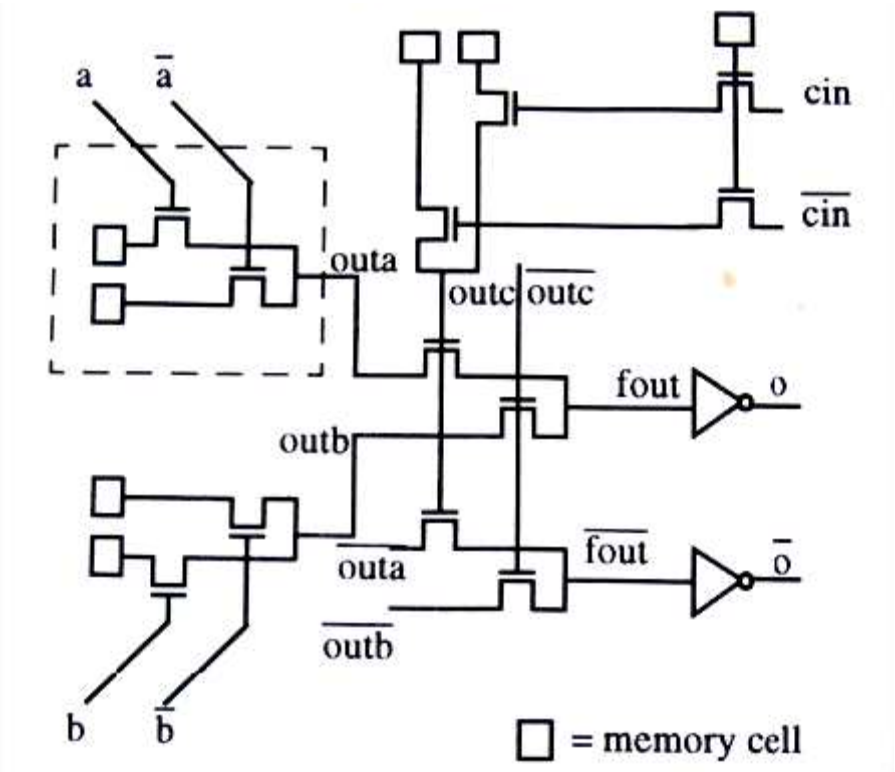

Figure 1: Circuit for problem 3.